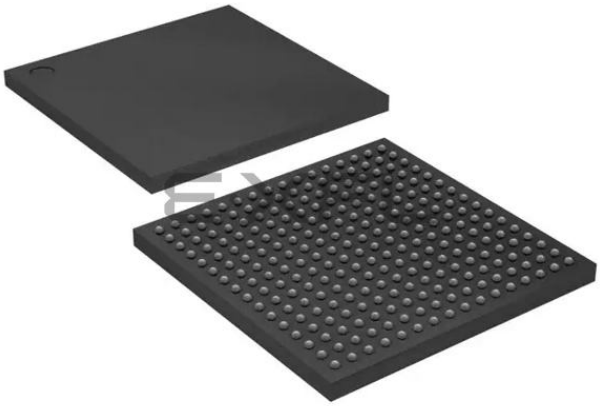

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

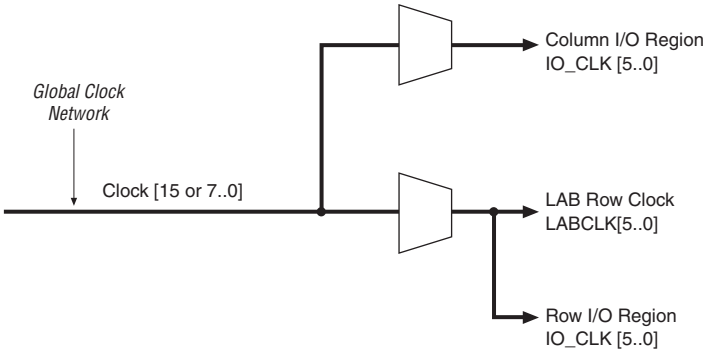
| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1172 |
| Number of Logic Elements/Cells | 18752 |
| Total RAM Bits | 239616 |
| Number of I/O | 152 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2c20f256c6 |

## Chapter 14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

## Global Clock Network Distribution

Cyclone II devices contains 16 global clock networks. The device uses multiplexers with these clocks to form six-bit buses to drive column IOE clocks, LAB row clocks, or row IOE clocks (see Figure 2–14). Another multiplexer at the LAB level selects two of the six LAB row clocks to feed the LE registers within the LAB.

*Figure 2–14. Global Clock Network Multiplexers*

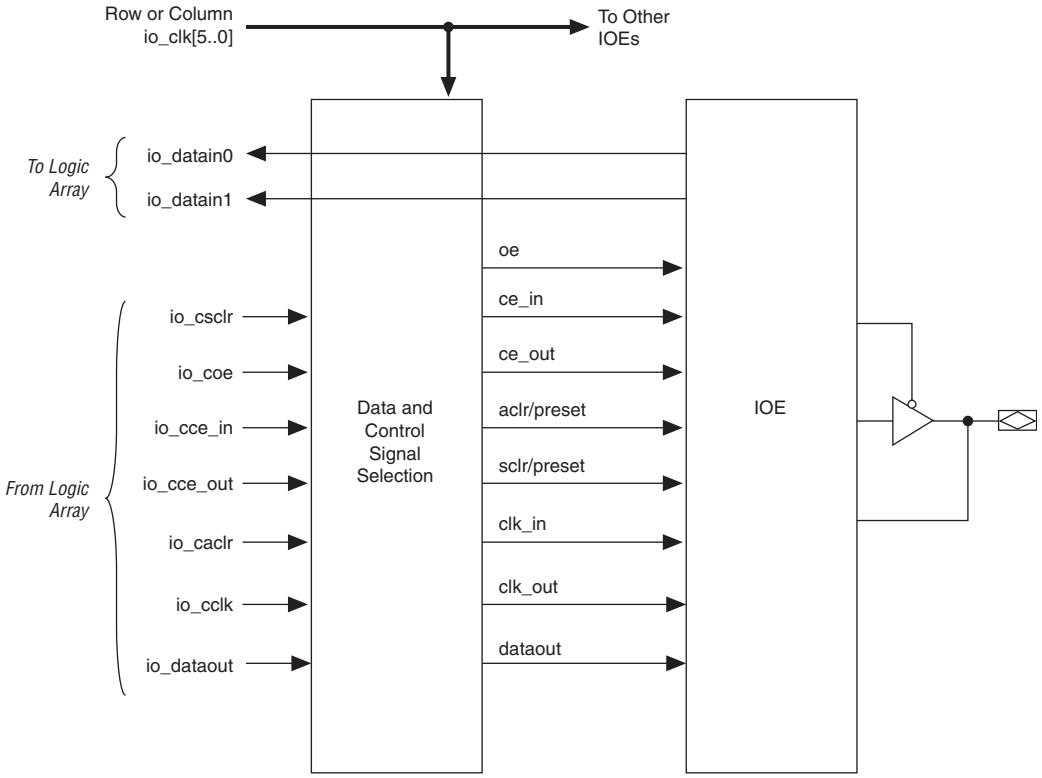



LAB row clocks can feed LEs, M4K memory blocks, and embedded multipliers. The LAB row clocks also extend to the row I/O clock regions.

IOE clocks are associated with row or column block regions. Only six global clock resources feed to these row and column regions. Figure 2–15 shows the I/O clock regions.

The pin's datain signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks, io_clk[5..0], provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions (see "Global Clock Network & Phase-Locked Loops" on page 2–16). Figure 2–23 illustrates the signal paths through the I/O block.

*Figure 2–23. Signal Path Through the I/O Block*




Each IOE contains its own control signal selection for the following control signals: oe, ce_in, ce_out, aclr/preset, sclr/preset, clk_in, and clk_out. Figure 2–24 illustrates the control signal selection.

## Programmable Drive Strength

The output buffer for each Cyclone II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL-2 class I and II, SSTL-18 class I and II, HSTL-18 class I and II, and HSTL-1.5 class I and II standards have several levels of drive strength that you can control. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 2–16 shows the possible settings for the I/O standards with drive strength control.

*Table 2–16. Programmable Drive Strength (Part 1 of 2)* *Note (1)*

| I/O Standard | $I_{OH}/I_{OL}$ Current Strength Setting (mA) | |
|---|---|---|
| | Top & Bottom I/O Pins | Side I/O Pins |
| LVTTL (3.3 V) | 4 | 4 |
| | 8 | 8 |
| | 12 | 12 |
| | 16 | 16 |
| | 20 | 20 |
| | 24 | 24 |
| LVCMOS (3.3 V) | 4 | 4 |
| | 8 | 8 |
| | 12 | 12 |
| | 16 | |
| | 20 | |
| | 24 | |
| LVTTL/LVCMOS (2.5 V) | 4 | 4 |
| | 8 | 8 |
| | 12 | |
| | 16 | |
| LVTTL/LVCMOS (1.8 V) | 2 | 2 |
| | 4 | 4 |
| | 6 | 6 |
| | 8 | 8 |
| | 10 | 10 |
| | 12 | 12 |

# Document Revision History

Table 3–5 shows the revision history for this document.

*Table 3–5. Document Revision History*

| Date & Document Version | Changes Made | Summary of Changes |
|---|---|---|
| February 2007 v2.2 | • Added document revision history.<br>• Added new handpara nore in "IEEE Std. 1149.1 (JTAG) Boundary Scan Support" section.<br>• Updated "Cyclone II Automated Single Event Upset Detection" section. | • Added information about limitation of cascading multi devices in the same JTAG chain.<br>• Corrected information on CRC calculation. |
| July 2005 v2.0 | Updated technical content. | |
| February 2005 v1.2 | Updated information on JTAG chain limitations. | |
| November 2004 v1.1 | Updated Table 3–4. | |
| June 2004 v1.0 | Added document to the Cyclone II Device Handbook. | |

Table 5–11 specifies the bus hold parameters for general I/O pins.

*Table 5–11. Bus Hold Parameters* *Note (1)*

| Parameter | Conditions | $V_{CCIO}$ Level | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | 1.8 V | | 2.5 V | | 3.3 V | | |
| | | Min | Max | Min | Max | Min | Max | |
| Bus-hold low, sustaining current | $V_{IN} > V_{IL}$(maximum) | 30 | — | 50 | — | 70 | — | µA |
| Bus-hold high, sustaining current | $V_{IN} < V_{IL}$(minimum) | –30 | — | –50 | — | –70 | — | µA |
| Bus-hold low, overdrive current | $0 V < V_{IN} < V_{CCIO}$ | — | 200 | — | 300 | — | 500 | µA |
| Bus-hold high, overdrive current | $0 V < V_{IN} < V_{CCIO}$ | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point *(2)* | — | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2.0 | V |

*Notes to Table 5–11:*
(1) There is no specification for bus-hold at $V_{CCIO}$ = 1.5 V for the HSTL I/O standard.
(2) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

## On-Chip Termination Specifications

Table 5–12 defines the specifications for internal termination resistance tolerance when using series or differential on-chip termination.

*Table 5–12. Series On-Chip Termination Specifications*

| Symbol | Description | Conditions | Resistance Tolerance | | | |
|---|---|---|---|---|---|---|
| | | | Commercial Max | Industrial Max | Extended/ Automotive Temp Max | Unit |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.3V | ±30 | ±30 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 2.5V | ±30 | ±30 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8V | ±30 *(1)* | ±40 | ±50 | % |

*Note to Table 5–12:*
(1) For commercial –8 devices, the tolerance is ±40%.

*Table 5–30. EP2C35 Row Pins Global Clock Timing Parameters*

| Parameter | Fast Corner | | –6 Speed Grade | –7 Speed Grade | –8 Speed Grade | Unit |
|---|---|---|---|---|---|---|
| | Industrial | Commercial | | | | |
| $t_{CIN}$ | 1.410 | 1.476 | 2.514 | 2.724 | 2.986 | ns |
| $t_{COUT}$ | 1.412 | 1.478 | 2.530 | 2.737 | 2.994 | ns |
| $t_{PLLCIN}$ | –0.117 | –0.127 | 0.134 | 0.162 | 0.241 | ns |
| $t_{PLLCOUT}$ | –0.115 | –0.125 | 0.15 | 0.175 | 0.249 | ns |

### *EP2C50 Clock Timing Parameters*

Tables 5–31 and 5–32 show the clock timing parameters for EP2C50 devices.

*Table 5–31. EP2C50 Column Pins Global Clock Timing Parameters*

| Parameter | Fast Corner | | –6 Speed Grade | –7 Speed Grade | –8 Speed Grade | Unit |
|---|---|---|---|---|---|---|
| | Industrial | Commercial | | | | |
| $t_{CIN}$ | 1.575 | 1.651 | 2.759 | 2.940 | 3.174 | ns |
| $t_{COUT}$ | 1.589 | 1.666 | 2.793 | 2.972 | 3.203 | ns |
| $t_{PLLCIN}$ | –0.149 | –0.158 | 0.113 | 0.075 | 0.089 | ns |
| $t_{PLLCOUT}$ | –0.135 | –0.143 | 0.147 | 0.107 | 0.118 | ns |

*Table 5–32. EP2C50 Row Pins Global Clock Timing Parameters*

| Parameter | Fast Corner | | –6 Speed Grade | –7 Speed Grade | –8 Speed Grade | Unit |
|---|---|---|---|---|---|---|
| | Industrial | Commercial | | | | |
| $t_{CIN}$ | 1.463 | 1.533 | 2.624 | 2.791 | 3.010 | ns |
| $t_{COUT}$ | 1.465 | 1.535 | 2.640 | 2.804 | 3.018 | ns |
| $t_{PLLCIN}$ | –0.261 | –0.276 | –0.022 | –0.074 | –0.075 | ns |
| $t_{PLLCOUT}$ | –0.259 | –0.274 | –0.006 | –0.061 | –0.067 | ns |

The loop filter converts these up and down signals to a voltage that is used to bias the VCO. If the charge pump receives a logic high on the up signal, current is driven into the loop filter. If the charge pump receives a logic high on the down signal, current is drawn from the loop filter. The loop filter filters out glitches from the charge pump and prevents voltage over-shoot, which minimizes the jitter on the VCO.

The voltage from the charge pump determines how fast the VCO operates. The VCO is implemented as an four-stage differential ring oscillator. A divide counter, *m*, is inserted in the feedback loop to increase the VCO frequency above the input reference frequency, making the VCO frequency $f_{VCO} = m \times f_{REF}$. Therefore, the feedback clock, $f_{FB}$, applied to one input of the PFD, is locked to the input reference clock, $f_{REF}$ ($f_{IN}/n$), applied to the other input of the PFD.

The VCO output can feed up to three post-scale counters (c0, c1, and c2). These post-scale counters allow a number of harmonically related frequencies to be produced by the PLL.

Additionally, Cyclone II PLLs have internal delay elements to compensate for routing on the global clock networks and I/O buffers. These internal delays are fixed and not accessible to the user.

Figure 7–2 shows a simplified block diagram of the major components of a Cyclone II device PLL.

## Document Revision History

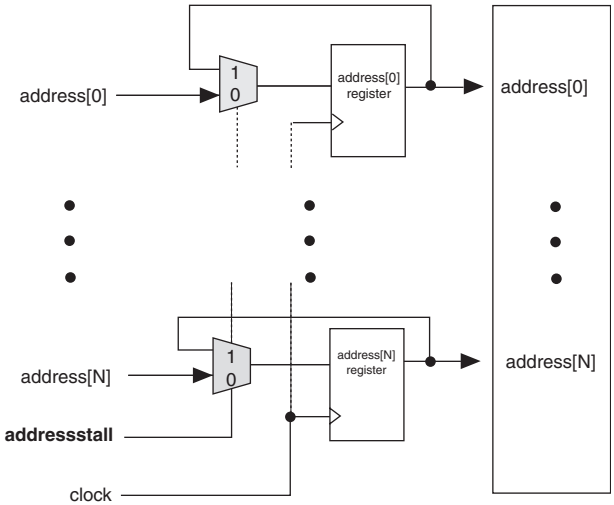
Table 7–10 shows the revision history for this document.

*Table 7–10. Document Revision History*

| Date & Document Version | Changes Made | Summary of Changes |
|---|---|---|
| February 2007 v3.1 | • Added document revision history.<br>• Updated handpara note in "Introduction".<br>• Updated *Note (3)* in Table 7–2.<br>• Updated Figure 7–5.<br>• Updated "Control Signals" section.<br>• Updated "Thick VCCA Trace" section. | • Updated chapter with extended temperature information.<br>• Updated `pllena` information in "Control Signals" section.<br>• Corrected capacitor unit from10-F to 10 µF. |
| December 2005 v2.2 | Updated industrial temperature range | |
| November 2005 v2.1 | • Updated Figure 7–12.<br>• Updated Figure 7–17. | |
| July 2005 v2.0 | • Updated Table 7–6.<br>• Updated "Hardware Features" section.<br>• Updated "areset" section.<br>• Updated Table 7–8.<br>• Added "Board Layout" section. | |
| February 2005 v1.2 | Updated information concerning signals.<br>Added a note to Figures 7-9 through 7-13 regarding violating the setup or hold time on address registers. | |
| November, 2004 v1.1 | Updated "Introduction" section. | |
| June 2004 v1.0 | Added document to the Cyclone II Device Handbook. | |

Figure 8–3 shows an address clock enable block diagram. The address register output is fed back to its input via a multiplexer. The multiplexer output is selected by the address clock enable (`addressstall`) signal. Address latching is enabled when the `addressstall` signal goes high (active high). The output of the address register is then continuously fed into the input of the register until the `addressstall` signal goes low.

***Figure 8–3. Cyclone II Address Clock Enable Block Diagram***




The address clock enable is typically used for cache memory applications to improve efficiency during a cache-miss. The default value for the address clock enable signals is low (disabled). Figures 8–4 and 8–5 show the address clock enable waveforms during the read and write cycles, respectively.

applications require local data storage, traditionally implemented with standard flip-flops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources.

The size of a ($w \times m \times n$) shift register is determined by the input data width ($w$), the length of the taps ($m$), and the number of taps ($n$), and must be less than or equal to the maximum number of memory bits, which is 4,608 bits. In addition, the size of ($w \times n$) must be less than or equal to the maximum width of the block, which is 36 bits. If a larger shift register is required, the memory blocks can be cascaded.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 8–12 shows the Cyclone II memory block in the shift register mode.

*Figure 8–12. Cyclone II Shift Register Mode Configuration*

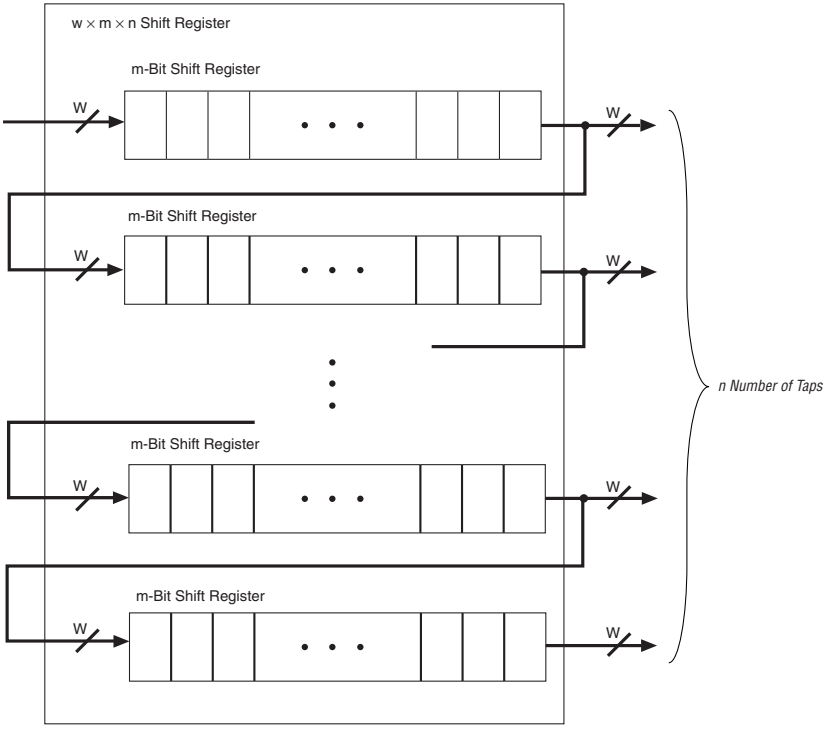
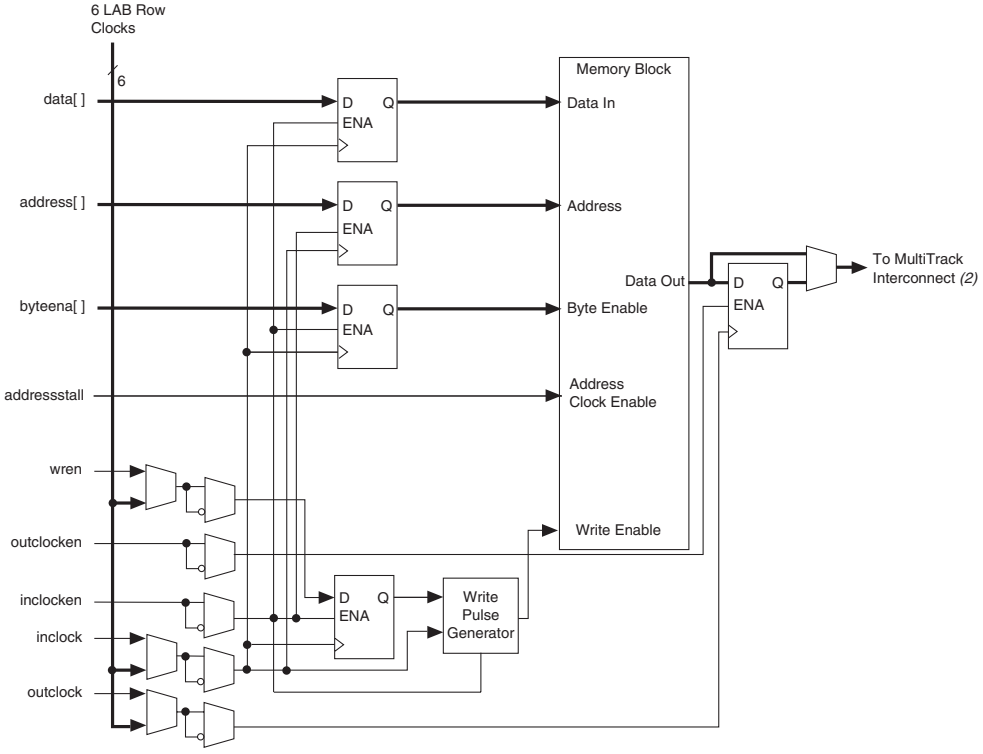


*Figure 8–16. Cyclone II Input/Output Clock Mode in Single-Port Mode* *Notes (1), (2)*




*Notes to Figure 8–16:*

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) For more information about the MultiTrack interconnect, refer to *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

## Read/Write Clock Mode

Cyclone II memory blocks can implement read/write clock mode for simple dual-port memory. The write clock controls the blocks' data inputs, write address, and write enable signals. The read clock controls the data output, read address, and read enable signals. The memory blocks support independent clock enables for each clock for the read- and write-side registers. This mode does not support asynchronous clear signals for the registers. Figure 8–17 shows a memory block in read/write clock mode.

*Figure 10–3. SSTL-2 Class I Differential Termination*

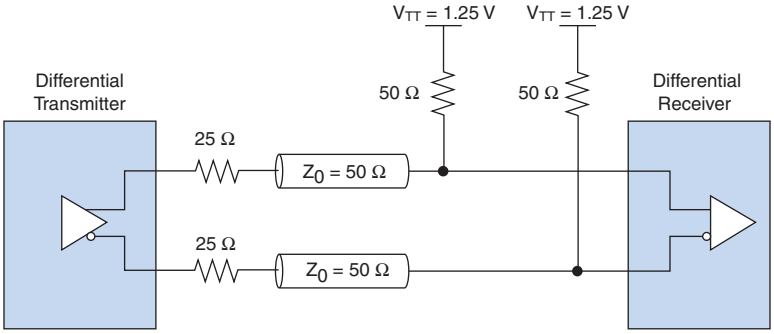
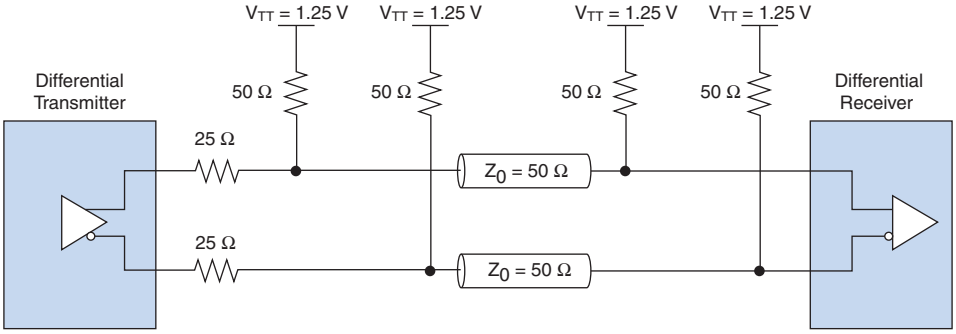



*Figure 10–4. SSTL-2 Class II Differential Termination*




## 1.8-V LVTTL (EIA/JEDEC Standard EIA/JESD8-7)

The 1.8-V I/O standard is used for 1.8-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts.

The 1.8-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.8-V LVTTL.

## Programmable Current Drive Strength

The Cyclone II device I/O standards support various output current drive settings as shown in Table 10–6. These programmable drive-strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for $I_{OH}$ and $I_{OL}$ of the corresponding I/O standard.

*Table 10–6. Programmable Drive Strength (Part 1 of 2)*

| I/O Standard | $I_{OH}/I_{OL}$ Current Strength Setting (mA) | |
|---|---|---|
| | Top and Bottom I/O Pins | Side I/O Pins |
| LVTTL (3.3 V) | 4 | 4 |
| | 8 | 8 |
| | 12 | 12 |
| | 16 | 16 |
| | 20 | 20 |
| | 24 | 24 |
| LVCMOS (3.3 V) | 4 | 4 |
| | 8 | 8 |
| | 12 | 12 |
| | 16 | — |
| | 20 | — |
| | 24 | — |
| LVTTL and LVCMOS (2.5 V) | 4 | 4 |
| | 8 | 8 |
| | 12 | — |
| | 16 | — |
| LVTTL and LVCMOS (1.8 V) | 2 | 2 |
| | 4 | 4 |
| | 6 | 6 |
| | 8 | 8 |
| | 10 | 10 |
| | 12 | 12 |
| LVCMOS (1.5 V) | 2 | 2 |
| | 4 | 4 |
| | 6 | 6 |
| | 8 | — |

## Configuration File Format

Table 13–3 shows the approximate uncompressed configuration file sizes for Cyclone II devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

*Table 13–3. Cyclone II Raw Binary File (.rbf) Sizes* *Note (1)*

| Device | Data Size (Bits) | Data Size (Bytes) |
|---|---|---|
| EP2C5 | 1,265,792 | 152,998 |
| EP2C8 | 1,983,536 | 247,974 |
| EP2C15 | 3,892,496 | 486,562 |
| EP2C20 | 3,892,496 | 486,562 |
| EP2C35 | 6,858,656 | 857,332 |
| EP2C50 | 9,963,392 | 1,245,424 |
| EP2C70 | 14,319,216 | 1,789,902 |

*Note to Table 13–3:*
(1) These values are preliminary.

Use the data in Table 13–3 only to estimate the file size before design compilation. Different configuration file formats, such as a Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) format, have different file sizes. However, for any specific version of the Quartus® II software, any design targeted for the same device has the same uncompressed configuration file size. If compression is used, the file size can vary after each compilation since the compression ratio is dependent on the design.

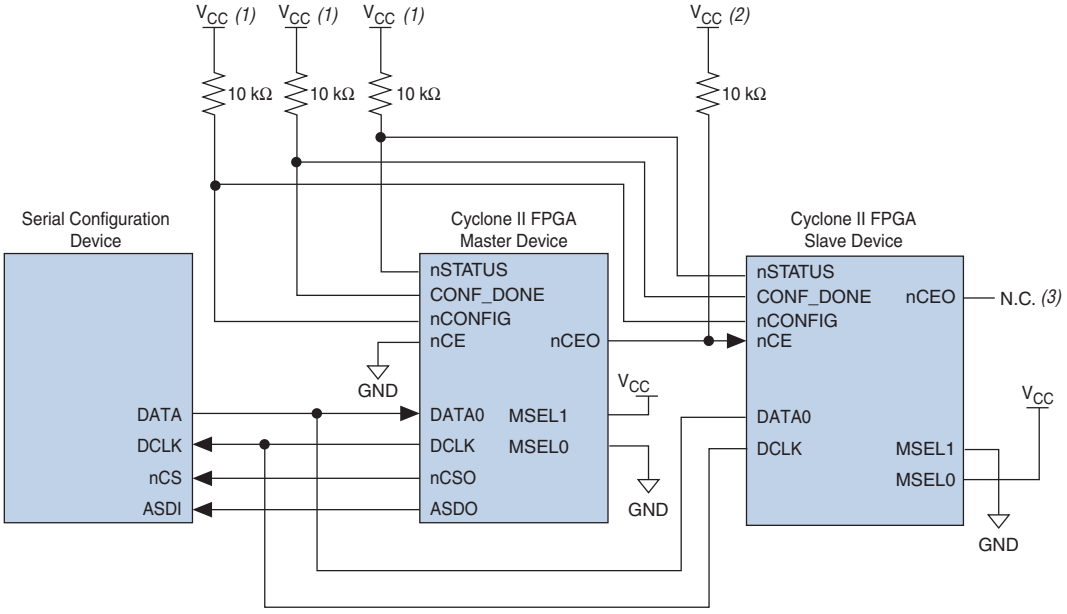
## Configuration Data Compression

Cyclone II devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Cyclone II devices. During configuration, the Cyclone II device decompresses the bitstream in real time and programs its SRAM cells.

Preliminary data indicates that compression reduces configuration bitstream size by 35 to 55%.

Cyclone II devices support decompression in the AS and PS configuration schemes. Decompression is not supported in JTAG-based configuration.

*Figure 13–4. Multiple Device AS Configuration*




*Notes to Figure 13–4:*

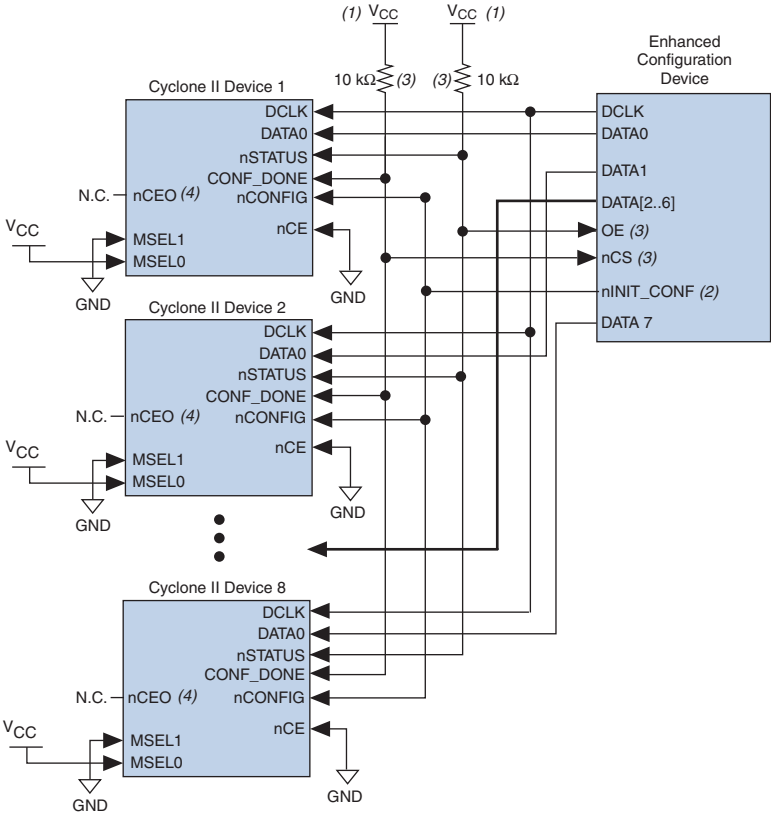
(1) Connect the pull-up resistors to a 3.3-V supply.

(2) Connect the pull-up resistor to the $V_{CCIO}$ supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

As shown in Figure 13–4, the nSTATUS and CONF_DONE pins on all target FPGAs are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the FPGAs. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep the CONF_DONE signal low until they receive their configuration data. When all the target FPGAs in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor pulls this signal high, and all devices simultaneously enter initialization mode.

*Figure 13–15. Concurrent PS Configuration of Multiple Devices Using an Enhanced Configuration Device*




*Notes to Table 13–15:*

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to $V_{CC}$ either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

The Quartus II software only allows you to set *n* to 1, 2, 4, or 8. However, you can use these modes to configure any number of devices from 1 to 8. For example, if you configure three FPGAs, you would use the 4-bit PS mode. For the DATA0, DATA1, and DATA2 lines, the corresponding SOF data is transmitted from the configuration device to the FPGA. For

# 14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

CII51014-2.1

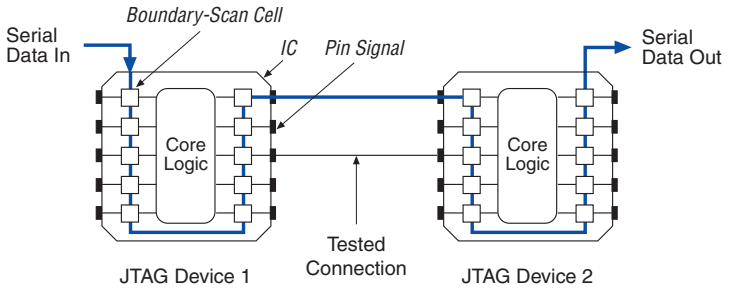
## Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (e.g., external test probes and "bed-of-nails" test fixtures) harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

This BST architecture tests pin connections without using physical test probes and captures functional data while a device is operating normally. Boundary-scan cells in a device force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared with expected results. Figure 14–1 shows the concept of boundary-scan testing.

*Figure 14–1. IEEE Std. 1149.1 Boundary-Scan Testing*



to external device data via the PIN_IN signal, while the update registers connect to external data through the PIN_OUT and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 14–4 shows the Cyclone II device's user I/O boundary-scan cell.

*Figure 14–4. Cyclone II Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry*