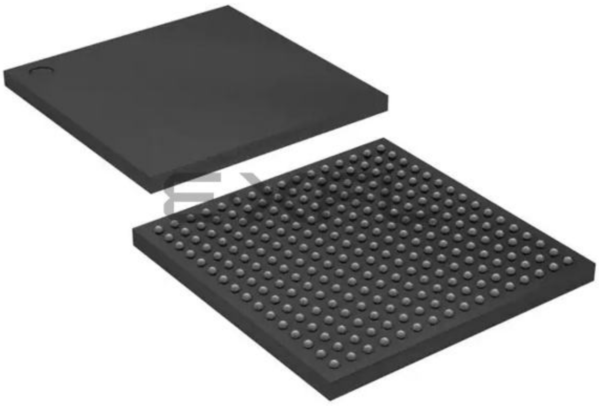

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1172
Number of Logic Elements/Cells	18752
Total RAM Bits	239616
Number of I/O	152
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c20f256c8

Table 1–1. Cyclone II FPGA Family Features (Part 2 of 2)

Feature	EP2C5 *(2)*	EP2C8 *(2)*	EP2C15 *(1)*	EP2C20 *(2)*	EP2C35	EP2C50	EP2C70
Maximum user I/O pins	158	182	315	315	475	450	622

Notes to Table 1–1:

(1) The EP2C15A is only available with the Fast On feature, which offers a faster POR time. This device is available in both commercial and industrial grade.

(2) The EP2C5, EP2C8, and EP2C20 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. The EP2C8A and EP2C20A devices are only available in industrial grade.

(3) This is the total number of 18 × 18 multipliers. For the total number of 9 × 9 multipliers per device, multiply the total number of 18 × 18 multipliers by 2.

Cyclone II devices are available in up to three speed grades: –6, –7, and –8, with –6 being the fastest. Table 1–4 shows the Cyclone II device speed-grade offerings.

Table 1–4. Cyclone II Device Speed Grades

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA	896-Pin FineLine BGA
EP2C5 *(1)*	–6, –7, –8	–7, –8	—	–6, –7, –8	—	—	—	—
EP2C8	–6, –7, –8	–7, –8	—	–6, –7, –8	—	—	—	—
EP2C8A *(2)*	—	—	—	–8	—	—	—	—
EP2C15A	—	—	—	–6, –7, –8	–6, –7, –8	—	—	—
EP2C20	—	—	–8	–6, –7, –8	–6, –7, –8	—	—	—
EP2C20A *(2)*	—	—	—	–8	–8	—	—	—
EP2C35	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	—
EP2C50	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	—
EP2C70	—	—	—	—	—	—	–6, –7, –8	–6, –7, –8

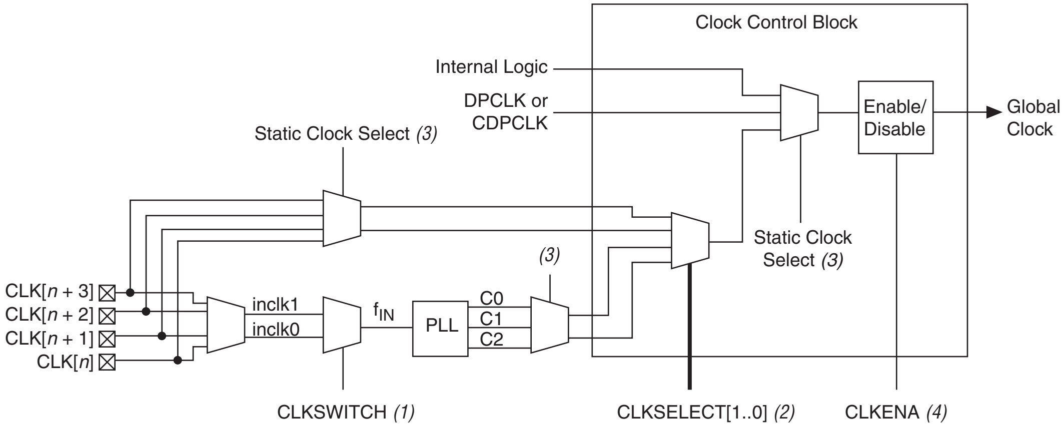
Notes to Table 1–4:

(1) The EP2C5 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. Refer to the Cyclone II section in the *Automotive-Grade Device Handbook* for detailed information.

(2) EP2C8A and EP2C20A are only available in industrial grade.

Of the sources listed, only two clock pins, two PLL clock outputs, one DPCLK pin, and one internally-generated signal are chosen to drive into a clock control block. Figure 2–13 shows a more detailed diagram of the clock control block. Out of these six inputs, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of DPCLK and the signal from internal logic.

Figure 2–13. Clock Control Block



Notes to Figure 2–13:

(1) The CLKSWITCH signal can either be set through the configuration file or it can be dynamically set when using the manual PLL switchover feature. The output of the multiplexer is the input reference clock (f_{IN}) for the PLL.

(2) The CLKSELECT[1..0] signals are fed by internal logic and can be used to dynamically select the clock source for the global clock network when the device is in user mode.

(3) The static clock select signals are set in the configuration file and cannot be dynamically controlled when the device is in user mode.

(4) Internal logic can be used to enabled or disabled the global clock network in user mode.

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL_18_CLASS_II	0	pF
1.5V_HSTL_CLASS_I	0	pF
1.5V_HSTL_CLASS_II	0	pF
1.8V_HSTL_CLASS_I	0	pF
1.8V_HSTL_CLASS_II	0	pF
DIFFERENTIAL_SSTL_2_CLASS_I	0	pF
DIFFERENTIAL_SSTL_2_CLASS_II	0	pF
DIFFERENTIAL_SSTL_18_CLASS_I	0	pF
DIFFERENTIAL_SSTL_18_CLASS_II	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
LVDS	0	pF
1.2V_HSTL	0	pF
1.2V_DIFFERENTIAL_HSTL	0	pF

Row I/O Output Standard	C6	C7	C8	Unit
Differential SSTL-2 Class I	60	90	90	ps
Differential SSTL-2 Class II	65	75	75	ps
Differential SSTL-18 Class I	90	165	165	ps
Differential HSTL-18 Class I	85	155	155	ps
Differential HSTL-15 Class I	145	145	205	ps
LVDS	60	60	60	ps
Simple RSDS	60	60	60	ps
Mini LVDS	60	60	60	ps
PCI	195	255	255	ps
PCI-X	195	255	255	ps

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins Notes (1), (2) (Part 2 of 2)

Notes to Table 5–55:
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Here is an example for calculating the DCD as a percentage for an SDR output on a row I/O on a –6 device:

If the SDR output I/O standard is SSTL-2 Class II, the maximum DCD is 65 ps (refer to Table 5–55). If the clock frequency is 167 MHz, the clock period T is:

$$T = 1/ f = 1 / 167 \text{ MHz} = 6 \text{ ns} = 6000 \text{ ps}$$

To calculate the DCD as a percentage:

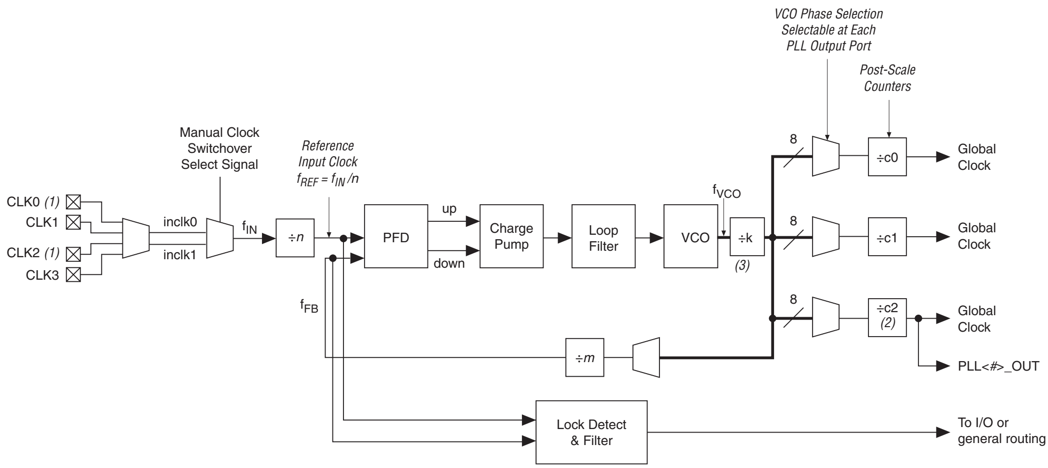
$$(T/2 – DCD) / T = (6000 \text{ ps}/2 – 65 \text{ ps}) / 6000 \text{ ps} = 48.91\%$$ (for low boundary)

$$(T/2 + DCD) / T = (6000 \text{ ps}/2 + 65 \text{ ps}) / 6000\text{ps} = 51.08\%$$ (for high boundary

Table 5–56. Maximum DCD for SDR Output on Column I/O Notes (1), (2) (Part 1 of 2)

Column I/O Output Standard	C6	C7	C8	Unit
LVCMOS	195	285	285	ps
LVTTL	210	305	305	ps

Figure 7–2. Cyclone II PLL Block Diagram



Notes to Figure 7–2:

(1) This input can be single-ended or differential. If you are using a differential I/O standard, then the design uses two clock pins. LVDS input is supported via the secondary function of the dedicated clock pins. For example, the `CLK0` pin's secondary function is `LVDSCLK1p` and the `CLK1` pin's secondary function is `LVDSCLK1n`. Figure 7–2 shows the possible clock input connections to PLL 1.

(2) This counter output is shared between a dedicated external clock output (`PLL<#>_OUT`) and the global clock network.

(3) If the VCO post scale counter = 2, a 300- to 500-MHz internal VCO frequency is available.

The Cyclone II PLL supports up to three global clock outputs and one dedicated external clock output. The output frequency to the global clock network or dedicated external clock output is determined by using the following equation:

$$f_{global/external} = f_{IN} \frac{m}{n \times C}$$

f_{IN} is the clock input to the PLL and C is the setting on the c0, c1, or c2 counter.

The VCO frequency is determined in all cases by using the following equation:

$$f_{VCO} = f_{IN} \frac{m}{n}$$

Table 7–5. PLL Output signals

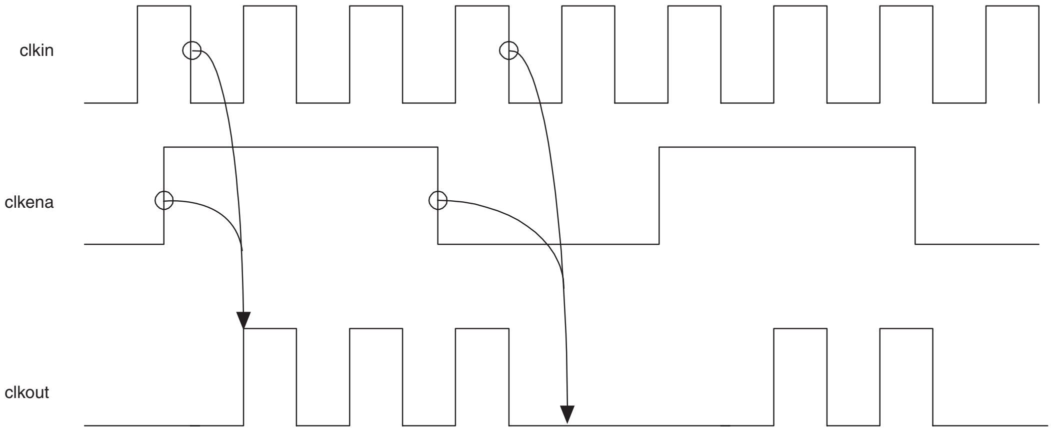
Port	Description	Source	Destination
`c[2..0]`	PLL clock outputs driving the internal global clock network or external clock output pin (`PLL<#>_OUT`)	PLL post-scale counter	Global clock network or external I/O pin
Locked	Gives the status of the PLL lock. When the PLL is locked, this port drives V_{CC}. When the PLL is out of lock, this port drives GND. The locked port may pulse high and low during the PLL lock process.	PLL lock detect circuit	Logic array or output pin

Table 7–6 shows a list of I/O standards supported in Cyclone II device PLLs.

Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 1 of 2)

I/O Standard	Input	Output	
	inclk	lock	pll_out
LVTTL (3.3, 2.5, and 1.8 V)	✓	✓	✓
LVCMOS (3.3, 2.5, 1.8, and 1.5 V)	✓	✓	✓
3.3-V PCI	✓	✓	✓
3.3-V PCI-X *(1)*	✓	✓	✓
LVPECL	✓		
LVDS	✓	✓	✓
1.5 and 1.8 V differential HSTL class I and class II	✓		✓ *(2)*
1.8 and 2.5 V differential SSTL class I and class II	✓		✓ *(2)*
1.5-V HSTL class I	✓	✓	✓
1.5-V HSTL class II *(3)*	✓	✓	✓
1.8-V HSTL class I	✓	✓	✓
1.8-V HSTL class II *(3)*	✓	✓	✓
SSTL-18 class I	✓	✓	✓
SSTL-18 class II *(3)*	✓	✓	✓
SSTL-25 class I	✓	✓	✓

Figure 7–15. clkena Implementation



The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during PLL resynchronization.

Altera recommends using the `clkena` signals when switching the clock source to the PLLs or the global clock network. The recommended sequence to be followed is:

1. Disable the primary output clock by de-asserting the `clkena` signal.
2. Switch to the secondary clock using the dynamic select signals of the clock control block.
3. Allow some clock cycles of the secondary clock to pass before re-asserting the `clkena` signal. The exact number of clock cycles you need to wait before enabling the secondary clock is design dependent. You can build custom logic to ensure glitch-free transition when switching between different clock sources.

Board Layout

The PLL circuits in Cyclone II devices contain analog components embedded in a digital device. These analog components have separate power and ground pins to minimize noise generated by the digital components.

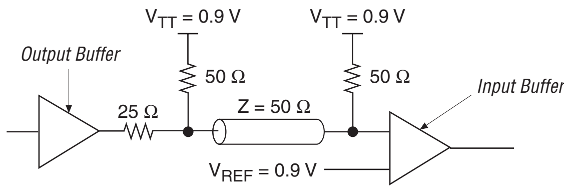
Document Revision History

Table 7–10 shows the revision history for this document.

Table 7–10. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	• Added document revision history. • Updated handpara note in "Introduction". • Updated *Note (3)* in Table 7–2. • Updated Figure 7–5. • Updated "Control Signals" section. • Updated "Thick VCCA Trace" section.	• Updated chapter with extended temperature information. • Updated `pllena` information in "Control Signals" section. • Corrected capacitor unit from10-F to 10 µF.
December 2005 v2.2	Updated industrial temperature range	
November 2005 v2.1	• Updated Figure 7–12. • Updated Figure 7–17.	
July 2005 v2.0	• Updated Table 7–6. • Updated "Hardware Features" section. • Updated "areset" section. • Updated Table 7–8. • Added "Board Layout" section.	
February 2005 v1.2	Updated information concerning signals. Added a note to Figures 7-9 through 7-13 regarding violating the setup or hold time on address registers.	
November, 2004 v1.1	Updated "Introduction" section.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Figure 10–6. 1.8-V SSTL Class II Termination



1.8-V HSTL Class I and II

The HSTL standard is a technology independent I/O standard developed by JEDEC to provide voltage scalability. It is used for applications designed to operate in the 0.0- to 1.8-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces.

Although JEDEC specifies a maximum V_{CCIO} value of 1.6 V, there are various memory chip vendors with HSTL standards that require a V_{CCIO} of 1.8 V. Cyclone II devices support interfaces with V_{CCIO} of 1.8 V for HSTL. Figures 10–7 and 10–8 show the nominal V_{REF} and V_{TT} required to track the higher value of V_{CCIO}. The value of V_{REF} is selected to provide optimum noise margin in the system. Cyclone II devices support both input and output levels of operation.

Figure 10–7. 1.8-V HSTL Class I Termination

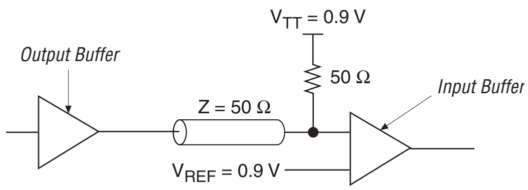
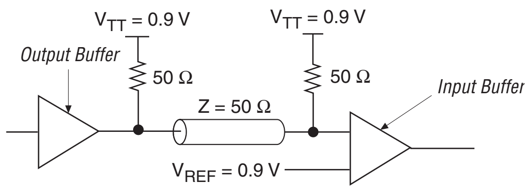


Figure 10–8. 1.8-V HSTL Class II Termination



V_{REF} Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply and to prevent output switching noise from shifting the V_{REF} rail, there are restrictions on the placement of single-ended voltage referenced I/Os with respect to V_{REF} pads and VCCIO and ground pairs. Use the following guidelines for placing single-ended pads in Cyclone II devices.

The Quartus II software automatically does all the calculations in this section.

Input Pads

Each V_{REF} pad supports up to 15 input pads on each side of the V_{REF} pad for FineLine BGA devices. Each V_{REF} pad supports up to 10 input pads on each side of the V_{REF} pad for quad flat pack (QFP) devices. This is irrespective of VCCIO and ground pairs, and is guaranteed by the Cyclone II architecture.

Output Pads

When a voltage referenced input or bidirectional pad does not exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each VCCIO and ground pair supports 9 output pins for Fineline BGA packages (not more than 9 output pins per 12 consecutive row I/O pins) or 5 output pins for QFP packages (not more than 5 output pins per 12 consecutive row I/O pins or 8 consecutive column I/O pins). Any non-SSTL and non-HSTL output can be no closer than two pads away from a V_{REF} pad. Altera recommends that any SSTL or HSTL output, except for pintable defined DQ and DQS outputs, to be no closer than two pads away from a V_{REF} pad to maintain acceptable noise levels.

Quartus II software will not check for the SSTL and HSTL output pads placement rule.

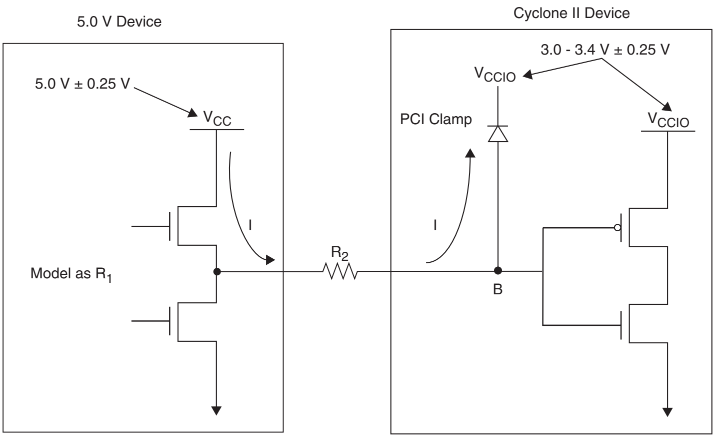
Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

Bidirectional Pads

Bidirectional pads must satisfy input and output guidelines simultaneously.

Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

Figure 10–21. Driving a Cyclone II Device with a 5.0-Volt Device



If V_{CCIO} is between 3.0 V and 3.6 V and the PCI clamping diode is enabled, the voltage at point B in Figure 10–21 is 4.3 V or less. To limit large current draw from the 5.0-V device, R_2 should be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (I_{OH}) specifications of the devices driving the trace. The PCI clamping diode in the Cyclone II device can support 25 mA of current.

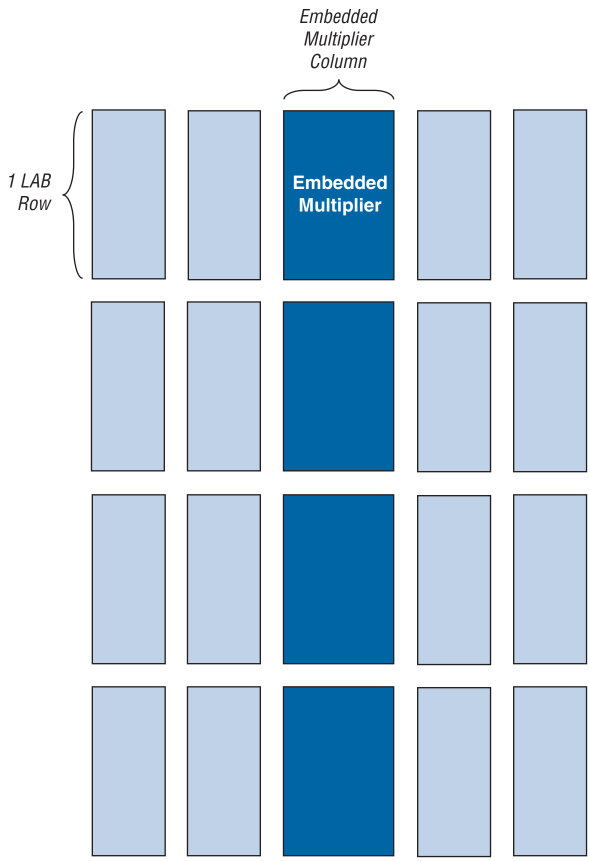
To compute the required value of R_2, first calculate the model of the pull-up transistors on the 5.0-V device. This output resistor (R_1) can be modeled by dividing the 5.0-V device supply voltage (V_{CC}) by the I_{OH}: $R_1 = V_{CC}/I_{OH}$.

Figure 10–22 shows an example of typical output drive characteristics of a 5.0-V device.

Embedded Multiplier Block Overview

Each Cyclone II device has one to three columns of embedded multipliers that implement multiplication functions. Figure 12–1 shows one of the embedded multiplier columns with the surrounding LABs. Each embedded multiplier can be configured to support one 18 × 18 multiplier or two 9 × 9 multipliers.

Figure 12–1. Embedded Multipliers Arranged in Columns with Adjacent LABs



configuration device. The configuration device then provides data on its serial data output (DATA) pin, which connects to the DATA0 input of the Cyclone II device.

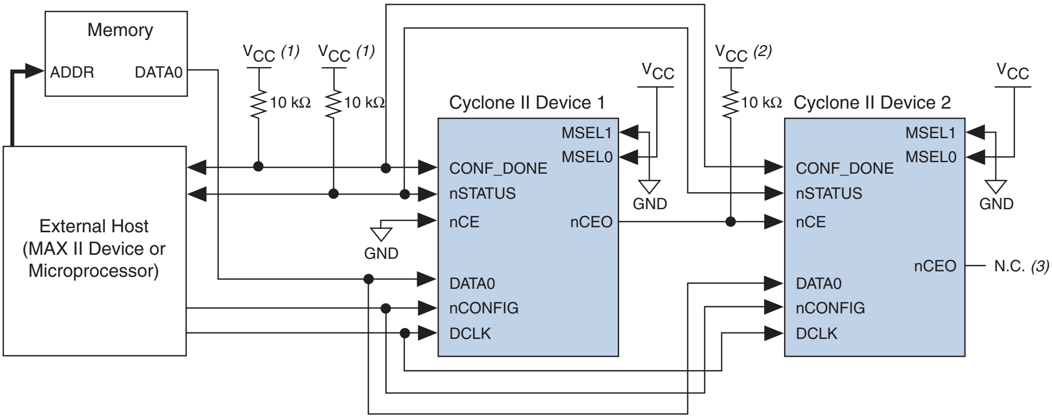
After the Cyclone II device receives all the configuration bits, it releases the open-drain CONF_DONE pin, which is then pulled high by an external 10-kΩ resistor. Also, the Cyclone II device stops driving the DCLK signal. Initialization begins only after the CONF_DONE signal reaches a logic high level. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. All AS configuration pins (DATA0, DCLK, nCSO, and ASDO) have weak internal pull-up resistors which are always active. After configuration, these pins are set as input tri-stated and are pulled high by the internal weak pull-up resistors.

Initialization Stage

In Cyclone II devices, the initialization clock source is either the Cyclone II 10-MHz (typical) internal oscillator (separate from the AS internal oscillator) or the optional CLKUSR pin. The internal oscillator is the default clock source for initialization. If the internal oscillator is used, the Cyclone II device provides itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. Additionally, you can use the CLKUSR pin as a user I/O pin.

If you want to delay the initialization of the device, you can use the CLKUSR pin option. Using the CLKUSR pin allows you to control when your device enters user mode. The device can be delayed from entering user mode for an indefinite amount of time. When you enable the **User Supplied Start-Up Clock** option, the CLKUSR pin is the initialization clock source. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data has been accepted and CONF_DONE goes high, Cyclone II devices require 299 clock cycles to initialize properly and support a CLKUSR f_{MAX} of 100 MHz.

Figure 13–10. Multiple Device PS Configuration Using an External Host



Notes to Figure 13–10:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

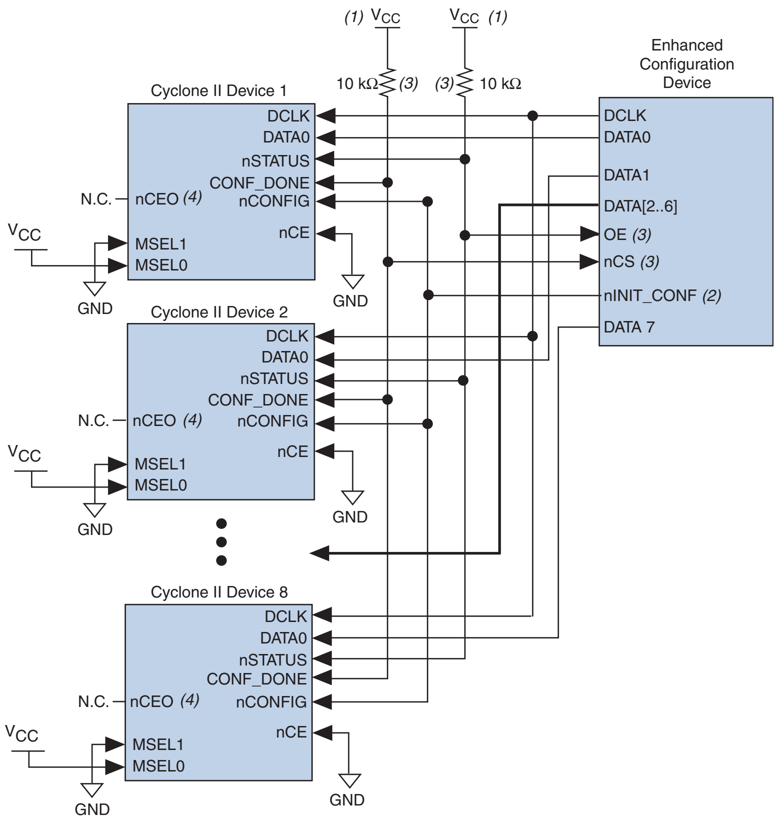
(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the `nCEO` pin resides in.

(3) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed another device's `nCE` pin.

In multiple device PS configuration, connect the first Cyclone II device's `nCE` pin to GND and connect the `nCEO` pin to the `nCE` pin of the next Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's `nCEO` pin high to its V_{CCIO} level to help the internal weak pull-up resistor when the `nCEO` pin feeds next Cyclone II device's `nCE` pin. The input to the `nCE` pin of the last Cyclone II device in the chain comes from the previous Cyclone II device. After the first device completes configuration in a multiple device configuration chain, its `nCEO` pin transitions low to activate the second device's `nCE` pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle. Therefore, the MAX II device begins to transfer data to the next Cyclone II device without interruption. The `nCEO` pin is a dual-purpose pin in Cyclone II devices. You can leave the `nCEO` pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in chain is a Cyclone II device.

☞ The Quartus II software sets the Cyclone II device `nCEO` pin as a dedicated output by default. If the `nCEO` pin feeds the next device's `nCE` pin, you must make sure that the `nCEO` pin is not used as a user I/O after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

Figure 13–15. Concurrent PS Configuration of Multiple Devices Using an Enhanced Configuration Device



Notes to Table 13–15:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The `nINIT_CONF` pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the `nINIT_CONF` to `nCONFIG` line. The `nINIT_CONF` pin does not need to be connected if its functionality is not used. If `nINIT_CONF` is not used, `nCONFIG` must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' `OE` and `nCS` pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

The Quartus II software only allows you to set *n* to 1, 2, 4, or 8. However, you can use these modes to configure any number of devices from 1 to 8. For example, if you configure three FPGAs, you would use the 4-bit PS mode. For the `DATA0`, `DATA1`, and `DATA2` lines, the corresponding SOF data is transmitted from the configuration device to the FPGA. For feature. To use this feature successfully, set the MSEL[1..0] pins of the master Cyclone II device to select the AS configuration scheme or fast AS configuration scheme (see Table 13–1).

☞ The Quartus II software version 4.1 and higher supports serial configuration device ISP through an FPGA JTAG interface using a JIC file.

The serial configuration device in-system programming through the Cyclone II JTAG interface has three stages, which are described in the following sections.

Loading the Serial Flash Loader Design

The serial flash loader design is a design inside the Cyclone II device that bridges the JTAG interface and AS interface inside the Cyclone II device using glue logic.

The intelligent host uses the JTAG interface to configure the master Cyclone II device with a serial flash loader design. The serial flash loader design allows the master Cyclone II device to control the access of four serial configuration device pins, also known as the Active Serial Memory Interface (ASMI) pins, through the JTAG interface. The ASMI pins are the serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS) pins.

If you configure a master Cyclone II device with a serial flash loader design, the master Cyclone II device can enter user mode even though the slave devices in the multiple device chain are not being configured. The master Cyclone II device can enter user mode with a serial flash loader design even though the CONF_DONE signal is externally held low by the other slave devices in chain. Figure 13–25 shows the JTAG configuration of a single Cyclone II device with a serial flash loader design.

15. Package Information for Cyclone II Devices

CII51015-2.3

Introduction

This chapter provides package information for Altera® Cyclone® II devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Table 15–1 shows Cyclone II device package options.

Table 15–1. Cyclone II Device Package Options

Device	Package	Pins
EP2C5	Plastic Thin Quad Flat Pack (TQFP) – Wirebond	144
	Plastic Quad Flat Pack (PQFP) – Wirebond	208
	Low profile FineLine BGA® – Wirebond	256
EP2C8	TQFP – Wirebond	144
	PQFP – Wirebond	208
	Low profile FineLine BGA – Wirebond	256
EP2C15	Low profile FineLine BGA, Option 2 – Wirebond	256
	FineLine BGA, Option 3– Wirebond	484
EP2C20	PQFP – Wirebond	240
	Low profile FineLine BGA, Option 2 – Wirebond	256
	FineLine BGA, Option 3– Wirebond	484
EP2C35	FineLine BGA, Option 3 – Wirebond	484
	Ultra FineLine BGA – Wirebond	484
	FineLine BGA, Option 3 – Wirebond	672
EP2C50	FineLine BGA, Option 3 – Wirebond	484
	Ultra FineLine BGA – Wirebond	484
	FineLine BGA, Option 3 – Wirebond	672
EP2C70	FineLine BGA, Option 3 – Wirebond	672
	FineLine BGA – Wirebond	896

Figure 15–4 shows a 256-pin FineLine BGA package outline.

Figure 15–4. 256-Pin FineLine BGA Package Outline