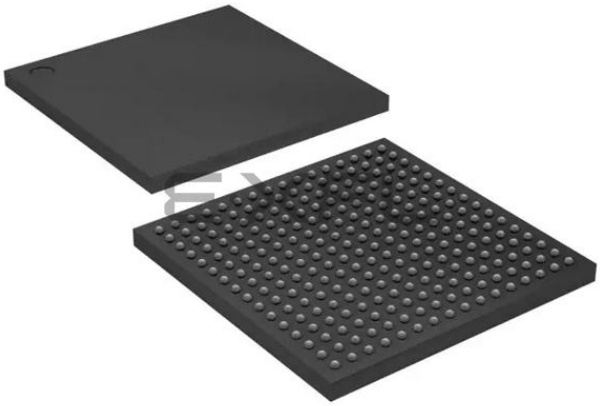

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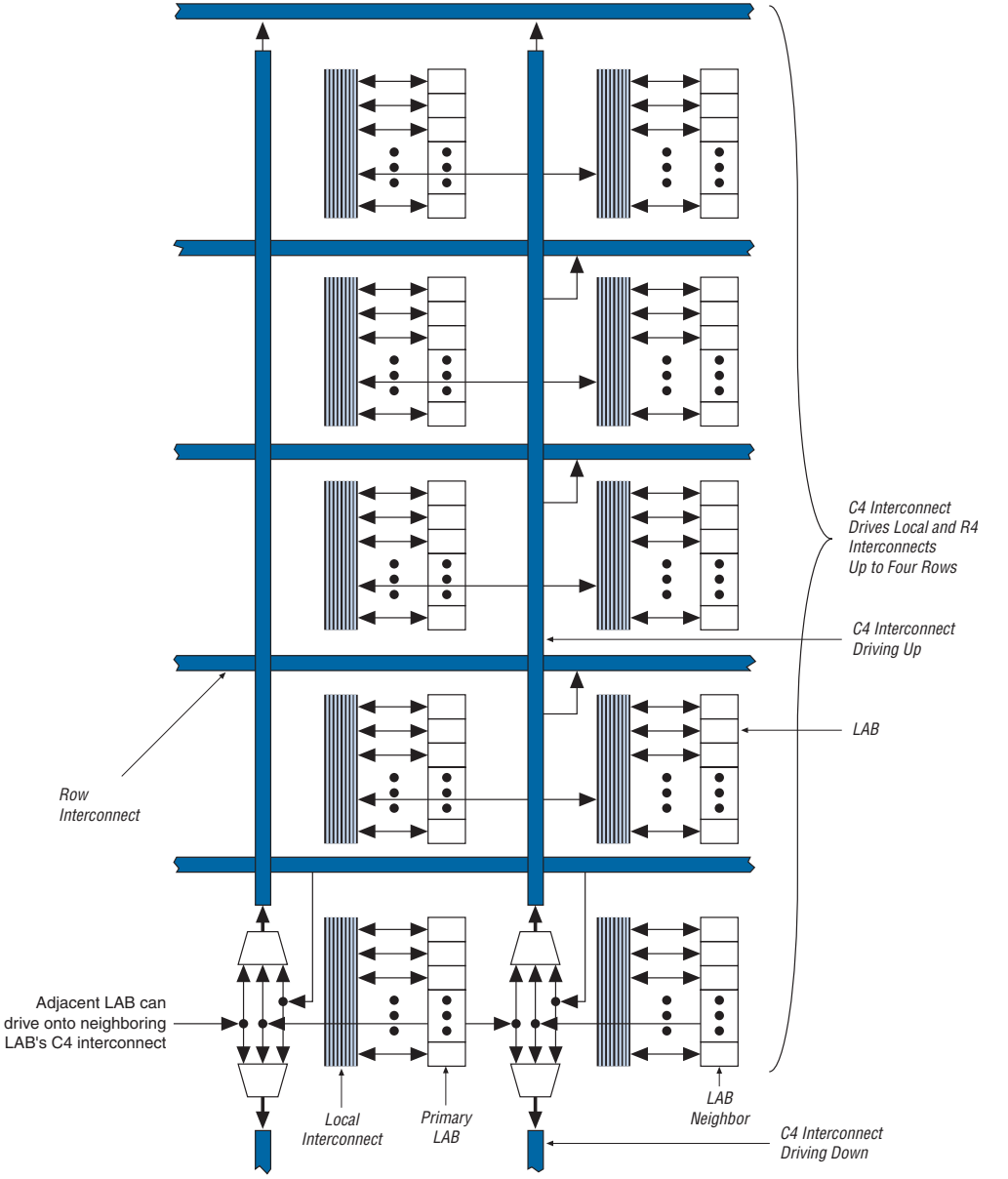
Details	
Product Status	Active
Number of LABs/CLBs	1172
Number of Logic Elements/Cells	18752
Total RAM Bits	239616
Number of I/O	152
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c20f256c8n

Figure 2–10. C4 Interconnect Connections *Note (1)*



Note to Figure 2–10:
(1) Each C4 interconnect can drive either up or down four rows.

3. Configuration & Testing

CII51003-2.2

IEEE Std. 1149.1 (JTAG) Boundary Scan Support

All Cyclone® II devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Cyclone II devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Cyclone II devices support IOE I/O standard reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the `CONFIG_IO` instruction. You can use this capability for JTAG testing before configuration when some of the Cyclone II pins drive or receive from other devices on the board using voltage-referenced standards. Since the Cyclone II device might not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming the I/O standards via JTAG allows you to fully test I/O connections to other devices.

For information on I/O reconfiguration, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*.

A device operating in JTAG mode uses four required pins: `TDI`, `TDO`, `TMS`, and `TCK`. The `TCK` pin has an internal weak pull-down resister, while the `TDI` and `TMS` pins have weak internal pull-up resistors. The `TDO` output pin and all JTAG input pin voltage is determined by the V_{CCIO} of the bank where it resides. The bank V_{CCIO} selects whether the JTAG inputs are 1.5-, 1.8-, 2.5-, or 3.3-V compatible.

Stratix® II, Stratix, Cyclone II and Cyclone devices must be within the first 8 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II, Stratix, Cyclone II or Cyclone devices are in the 9th of further position, they fail configuration. This does not affect Signal Tap II.

The Cyclone II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Cyclone II devices.

Table 3–2. Cyclone II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2C5	498
EP2C8	597
EP2C15	969
EP2C20	969
EP2C35	1,449
EP2C50	1,374
EP2C70	1,890

Table 3–3. 32-Bit Cyclone II Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP2C5	0000	0010 0000 1011 0001	000 0110 1110	1
EP2C8	0000	0010 0000 1011 0010	000 0110 1110	1
EP2C15	0000	0010 0000 1011 0011	000 0110 1110	1
EP2C20	0000	0010 0000 1011 0011	000 0110 1110	1
EP2C35	0000	0010 0000 1011 0100	000 0110 1110	1
EP2C50	0000	0010 0000 1011 0101	000 0110 1110	1
EP2C70	0000	0010 0000 1011 0110	000 0110 1110	1

Notes to Table 3–3:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

For more information on the Cyclone II JTAG specifications, refer to the *DC Characteristics & Timing Specifications* chapter in the *Cyclone II Device Handbook, Volume 1*.

Document Revision History

Table 3–5 shows the revision history for this document.

Table 3–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	• Added document revision history. • Added new handpara nore in "IEEE Std. 1149.1 (JTAG) Boundary Scan Support" section. • Updated "Cyclone II Automated Single Event Upset Detection" section.	• Added information about limitation of cascading multi devices in the same JTAG chain. • Corrected information on CRC calculation.
July 2005 v2.0	Updated technical content.	
February 2005 v1.2	Updated information on JTAG chain limitations.	
November 2004 v1.1	Updated Table 3–4.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Table 5–11 specifies the bus hold parameters for general I/O pins.

Table 5–11. Bus Hold Parameters *Note (1)*

Parameter	Conditions	V_{CCIO} Level						Unit
		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$(maximum)	30	—	50	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IL}$(minimum)	–30	—	–50	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	200	—	300	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–200	—	–300	—	–500	µA
Bus-hold trip point *(2)*	—	0.68	1.07	0.7	1.7	0.8	2.0	V

Notes to Table 5–11:
(1) There is no specification for bus-hold at V_{CCIO} = 1.5 V for the HSTL I/O standard.
(2) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination Specifications

Table 5–12 defines the specifications for internal termination resistance tolerance when using series or differential on-chip termination.

Table 5–12. Series On-Chip Termination Specifications

Symbol	Description	Conditions	Resistance Tolerance			
			Commercial Max	Industrial Max	Extended/ Automotive Temp Max	Unit
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3V	±30	±30	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 2.5V	±30	±30	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8V	±30 *(1)*	±40	±50	%

Note to Table 5–12:
(1) For commercial –8 devices, the tolerance is ±40%.

Table 5–18. DSP Block Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TPIPE2OUTREG	47	104	45	142	45	185	ps
	—	—	47	—	47	—	ps
TPD9	529	2470	505	3353	505	4370	ps
	—	—	529	—	529	—	ps
TPD18	425	2903	406	3941	406	5136	ps
	—	—	425	—	425	—	ps
TCLR	2686	—	3572	—	3572	—	ps
	—	—	3129	—	3572	—	ps
TCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

Notes to Table 5–18:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–19. M4K Block Internal Timing Microparameters (Part 1 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KRC	2387	3764	2275	4248	2275	4736	ps
	—	—	2387	—	2387	—	ps
TM4KWERESU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KWEREH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KBESU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps

EP2C70 Clock Timing Parameters

Tables 5–33 and 5–34 show the clock timing parameters for EP2C70 devices.

Table 5–33. EP2C70 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.914	3.105	3.174	ns
t_{COUT}	1.589	1.666	2.948	3.137	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.27	0.268	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.304	0.3	0.118	ns

Table 5–34. EP2C70 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.753	2.927	3.010	ns
t_{COUT}	1.465	1.535	2.769	2.940	3.018	ns
t_{PLLCIN}	–0.261	–0.276	0.109	0.09	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	0.125	0.103	–0.067	ns

Clock Network Skew Adders

Table 5–35 shows the clock network specifications.

Table 5–35. Clock Network Specifications

Name	Description	Max	Unit
Clock skew adder EP2C5/A, EP2C8/A *(1)*	Inter-clock network, same bank	±88	ps
	Inter-clock network, same side and entire chip	±88	ps
Clock skew adder EP2C15A, EP2C20/A, EP2C35, EP2C50, EP2C70 *(1)*	Inter-clock network, same bank	±118	ps
	Inter-clock network, same side and entire chip	±138	ps

Note to Table 5–35:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 3 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
SSTL_2_ CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
SSTL_2_ CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps
SSTL_18_ CLASS_I	6 mA	t_{OP}	1472	1544	3140	3345	3542	3549	ps
		t_{DIP}	1604	1683	3310	3539	3768	3768	ps
	8 mA	t_{OP}	1469	1541	3086	3287	3482	3489	ps
		t_{DIP}	1601	1680	3256	3481	3708	3708	ps
	10 mA	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
	12 mA (1)	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
SSTL_18_ CLASS_II	16 mA	t_{OP}	1454	1525	2905	3088	3263	3270	ps
		t_{DIP}	1586	1664	3075	3282	3489	3489	ps
	18 mA (1)	t_{OP}	1453	1524	2900	3082	3257	3264	ps
		t_{DIP}	1585	1663	3070	3276	3483	3483	ps
1.8V_HSTL_ CLASS_I	8 mA	t_{OP}	1460	1531	3222	3424	3618	3625	ps
		t_{DIP}	1592	1670	3392	3618	3844	3844	ps
	10 mA	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
	12 mA (1)	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps

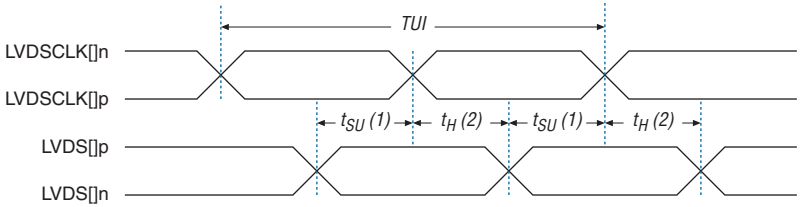
Table 5–49. Mini-LVDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Device operation in Mbps	×10	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	311	20	—	311	20	—	311	Mbps
	×1	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%	—	—	500	—	—	500	—	—	500	ps
t_{FALL}	80–20%	—	—	500	—	—	500	—	—	500	ps
t_{LOCK}		—	—	100	—	—	100	—	—	100	µs

In order to determine the transmitter timing requirements, mini-LVDS receiver timing requirements on the other end of the link must be taken into consideration. The mini-LVDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for mini-LVDS are shown in Figure 5–6.

Figure 5–6. mini-LVDS Transmitter AC Timing Specification



Notes to Figure 5–6:
(1) The data setup time, t_{SU}, is 0.225 × TUI.
(2) The data hold time, t_H, is 0.225 × TUI.

Table 5–54. PLL Specifications Note (1) (Part 2 of 2)

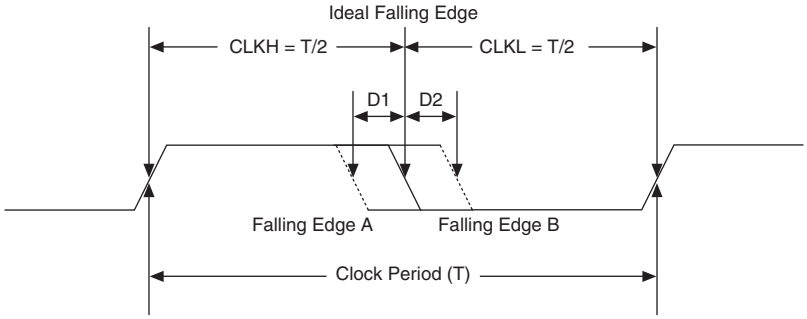
Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO} (3)	PLL internal VCO operating range	300	—	1,000	MHz
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns

Notes to Table 5–54:
(1) These numbers are preliminary and pending silicon characterization.
(2) The t_{JITTER} specification for the PLL[4..1]_OUT pins are dependent on the I/O pins in its VCCIO bank, how many of them are switching outputs, how much they toggle, and whether or not they use programmable current strength.
(3) If the VCO post-scale counter = 2, a 300- to 500-MHz internal VCO frequency is available.
(4) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
(5) Cyclone II PLLs can track a spread-spectrum input clock that has an input jitter within ±200 ps.
(6) For extended temperature devices, the maximum lock time is 500 us.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 5–8. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (Figure 5–8). The maximum DCD for a clock is the larger value of D1 and D2.

Figure 5–8. Duty Cycle Distortion



DCD expressed in absolution derivation, for example, D1 or D2 in Figure 5–8, is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as:

The VCO frequency is a critical parameter that must be between 300 and 1,000 MHz to ensure proper operation of the PLL. The Quartus II software automatically sets the VCO frequency within the recommended range based on the clock output and phase-shift requirements in your design.

PLL Reference Clock Generation

In Cyclone II devices, up to four clock pins can drive the PLL, as shown in Figure 7–11 on page 7–26. The multiplexer output feeds the PLL reference clock input. The PLL has internal delay elements that compensate for the clock delay from the input pin to the clock input port of the PLL.

Table 7–3 shows the clock input pin connections to the PLLs in the Cyclone II device.

Table 7–3. PLL Clock Input Pin Connections

Device	PLL 1		PLL 2		PLL 3		PLL 4	
	CLK0 CLK1	CLK2 CLK3	CLK4 CLK5	CLK6 CLK7	CLK8 CLK9	CLK10 CLK11	CLK12 CLK13	CLK14 CLK15
EP2C5	✓	✓	✓	✓				
EP2C8	✓	✓	✓	✓				
EP2C15	✓	✓	✓	✓	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓	✓	✓	✓	✓

Each PLL can be fed by one of four single-ended or two differential clock input pins. For example, PLL 1 can be fed by `CLK[3..0]` when using a single-ended I/O standard. When your design uses a differential I/O standard, these same clock pins have a secondary function as `LVDSCLK[2..1]p` and `LVDSCLK[2..1]n` pins. When using differential clocks, the `CLK0` pin's secondary function is `LVDSCLK1p`, the `CLK1` pin's secondary function is `LVDSCLK1n`, etc.

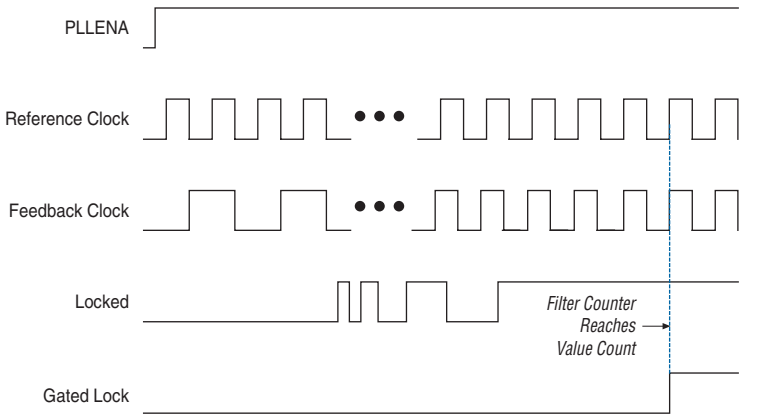
locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals



VCCA & GNDA

Each Cyclone II PLL uses separate VCC and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called VCCA_PLL<*PLL number*> and GNDA_ PLL<*PLL number*>. Connect the VCCA power pin to a 1.2-V power supply, even if you do not use the PLL. Isolate the power connected to VCCA from the power to the rest of the Cyclone II device or any other digital device on the board. You can use one of three different methods of isolating the VCCA pin:

- Use separate VCCA power planes
- Use a partitioned VCCA island within the VCCINT plane
- Use thick VCCA traces

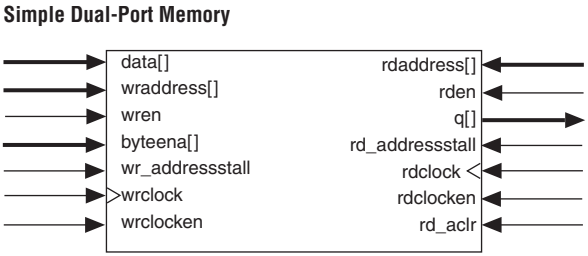
Separate VCCA Power Plane

A mixed signal system is already partitioned into analog and digital sections, each with its own power planes on the board. To isolate the VCCA pin using a separate VCCA power plane, connect the VCCA pin to the analog 1.2-V power plane.

Partitioned VCCA Island Within the VCCINT Plane

Fully digital systems do not have a separate analog power plane on the board. Since it is expensive to add new planes to the board, you can create islands for VCCA_PLL. Figure 7–16 shows an example board layout with an analog power island. The dielectric boundary that creates the island should be 25 mils thick. Figure 7–16 shows a partitioned plane within V_{CCINT} for VCCA.

Figure 8–8. Cyclone II Simple Dual-Port Mode *Note (1)*



Note to Figure 8–8:
(1) Simple dual-port RAM supports input and output clock mode in addition to the read and write clock mode shown.

Cyclone II memory blocks support mixed-width configurations, allowing different read and write port widths. Tables 8–5 and 8–6 show the mixed-width configurations.

Table 8–5. Cyclone II Memory Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

In simple dual-port mode, the memory blocks have one write enable and one read enable signal. They do not support a clear port on the write enable and read enable registers. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is the old data stored at the memory

Independent Clock Mode

Cyclone II memory blocks can implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables for port A and B registers. However, ports do not support asynchronous clear signals for the registers.

Figure 8–13 shows a memory block in independent clock mode.

Document Revision History

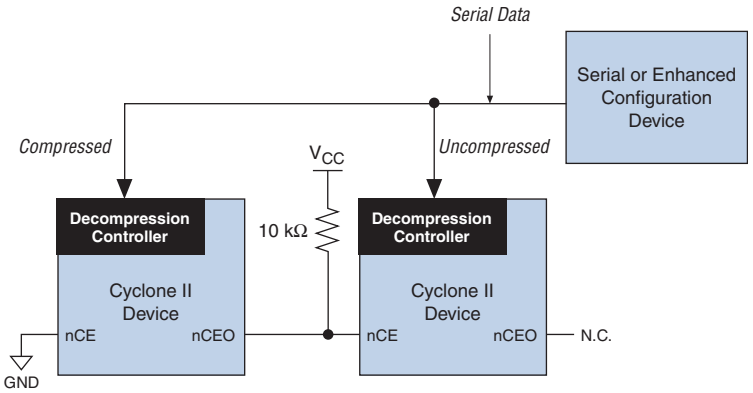
Table 11–6 shows the revision history for this document.

Table 11–6. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	• Added document revision history. • Added *Note (1)* to Table 11–1. • Updated Figure 11–5 and added *Note (1)* • Added *Note (1)* to Table 11–2. • Updated Figure 11–6 and added *Note (1)* • Added *Note (1)* to Table 11–3. • Added *Note (1)* to Figure 11–9.	• Added information stating LVDS/RSDS/mini-LVDS I/O standards specifications apply at the external resistors network output.
November 2005 v2.1	• Updated Table 11–2. • Updated Figures 11–7 through 11–9. • Added Resistor Network Solution for RSDS. • Updated note for mini-LVDS Resistor Network table.	
July 2005 v2.0	• Updated "I/O Standards Support" section. • Updated Tables 11–1 through 11–3.	
November 2004 v1.1	• Updated Table 11–1. • Updated Figures 11–4, 11–5, 11–7, and 11–9.	
June 2004, v1.0	Added document to the Cyclone II Device Handbook.	

When multiple Cyclone II devices are cascaded, the compression feature can be selectively enabled for each device in the chain. Figure 13–2 depicts a chain of two Cyclone II devices. The first Cyclone II device has compression enabled and therefore receives a compressed bitstream from the configuration device. The second Cyclone II device has the compression feature disabled and receives uncompressed data.

Figure 13–2. Compressed & Uncompressed Configuration Data in a Programming File



You can generate programming files (for example, POF files) for this setup in the Quartus II software.

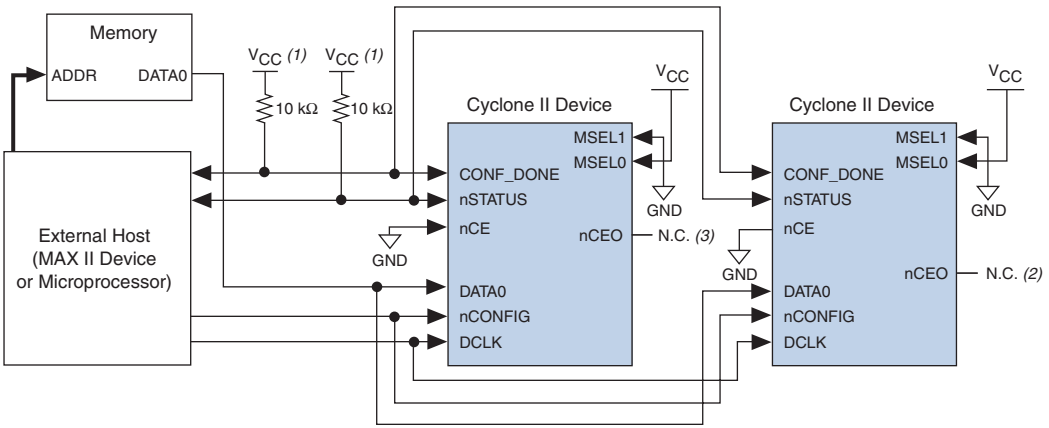
Active Serial Configuration (Serial Configuration Devices)

In the AS configuration scheme, Cyclone II devices are configured using a serial configuration device. These configuration devices are low-cost devices with non-volatile memory that feature a simple, four-pin interface and a small form factor. These features make serial configuration devices an ideal low-cost configuration solution.

For more information on serial configuration devices, see the *Serial Configuration Devices Data Sheet* in the Configuration Handbook.

If your system has multiple Cyclone II devices (in the same density and package) with the same configuration data, you can configure them in one configuration cycle by connecting all device's nCE pins to ground and connecting all the Cyclone II device's configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) together. You can also use the nCEO pin as a user I/O pin after configuration. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Make sure the DCLK and DATA lines are buffered for every fourth device. All devices start and complete configuration at the same time. Figure 13–11 shows multiple device PS configuration when both Cyclone II devices are receiving the same configuration data.

Figure 13–11. Multiple Device PS Configuration When Both FPGAs Receive the Same Data



Notes to Figure 13–11:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

(2) The nCEO pins of both devices can be left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

You can use a single configuration chain to configure Cyclone II devices with other Altera devices. Connect all the Cyclone II device's and all other Altera device's CONF_DONE and nSTATUS pins together so all devices in the chain complete configuration at the same time or that an error reported by one device initiates reconfiguration in all devices.

For more information on configuring multiple Altera devices in the same configuration chain, see *Configuring Mixed Altera FPGA Chains* in the *Configuration Handbook*.

operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

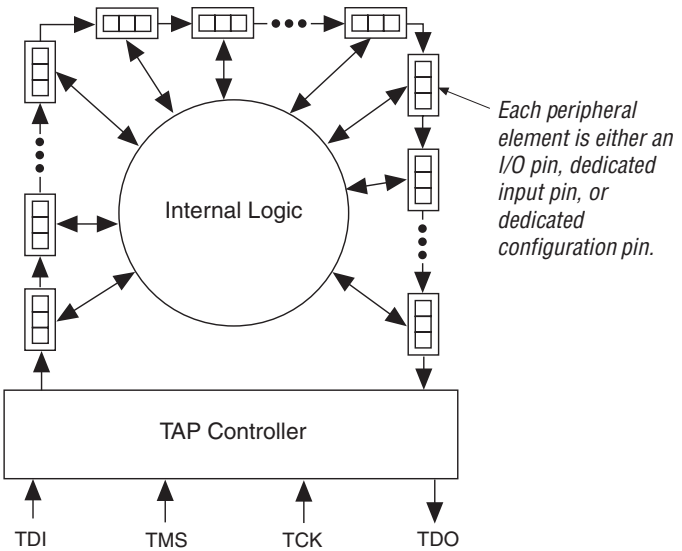
IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are associated with Cyclone II I/O pins. You can use the boundary-scan register to test external pin connections or to capture internal data.

See the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook* for the Cyclone II device boundary-scan register lengths.

Figure 14–3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 14–3. Boundary-Scan Register



Boundary-Scan Cells of a Cyclone II Device I/O Pin

The Cyclone II device 3-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data via the OUTJ and OEJ signals, and connect

15. Package Information for Cyclone II Devices

CII51015-2.3

Introduction

This chapter provides package information for Altera® Cyclone® II devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Table 15–1 shows Cyclone II device package options.

Table 15–1. Cyclone II Device Package Options

Device	Package	Pins
EP2C5	Plastic Thin Quad Flat Pack (TQFP) – Wirebond	144
	Plastic Quad Flat Pack (PQFP) – Wirebond	208
	Low profile FineLine BGA® – Wirebond	256
EP2C8	TQFP – Wirebond	144
	PQFP – Wirebond	208
	Low profile FineLine BGA – Wirebond	256
EP2C15	Low profile FineLine BGA, Option 2 – Wirebond	256
	FineLine BGA, Option 3– Wirebond	484
EP2C20	PQFP – Wirebond	240
	Low profile FineLine BGA, Option 2 – Wirebond	256
	FineLine BGA, Option 3– Wirebond	484
EP2C35	FineLine BGA, Option 3 – Wirebond	484
	Ultra FineLine BGA – Wirebond	484
	FineLine BGA, Option 3 – Wirebond	672
EP2C50	FineLine BGA, Option 3 – Wirebond	484
	Ultra FineLine BGA – Wirebond	484
	FineLine BGA, Option 3 – Wirebond	672
EP2C70	FineLine BGA, Option 3 – Wirebond	672
	FineLine BGA – Wirebond	896