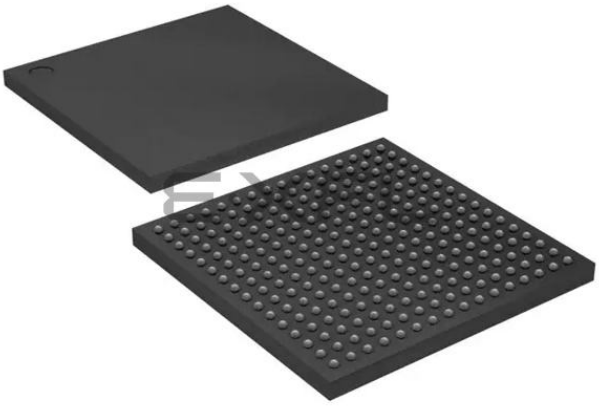

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1172
Number of Logic Elements/Cells	18752
Total RAM Bits	239616
Number of I/O	152
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c20f256i8

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes	
Clock Mode	**Description**
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`.
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

Table 2–9. Cyclone II M4K Memory Clock Modes			
Clocking Modes	**True Dual-Port Mode**	**Simple Dual-Port Mode**	**Single-Port Mode**
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Table 5–19. M4K Block Internal Timing Microparameters (Part 2 of 3)

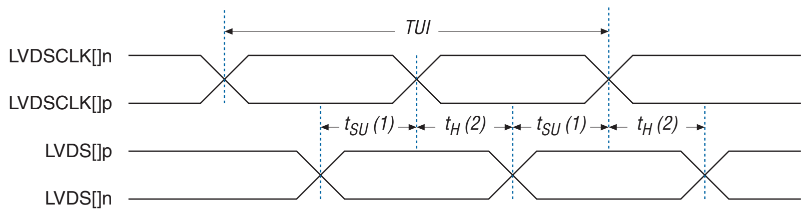
Parameter	–6 Speed Grade *(1)*		–7 Speed Grade *(2)*		–8 Speed Grade *(3)*		Unit
	Min	Max	Min	Max	Min	Max	
TM4KBEH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATAASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATAAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KADDRASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KADDRAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATABSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATABH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KRADDRBSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KRADDRBH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATACO1	466	724	445	826	445	930	ps
	—	—	466	—	466	—	ps
TM4KDATACO2	2345	3680	2234	4157	2234	4636	ps
	—	—	2345	—	2345	—	ps
TM4KCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TM4KCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

Table 5–49. Mini-LVDS Transmitter Timing Specification (Part 2 of 2)											
Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Device operation in Mbps	×10	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	311	20	—	311	20	—	311	Mbps
	×1	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%	—	—	500	—	—	500	—	—	500	ps
t_{FALL}	80–20%	—	—	500	—	—	500	—	—	500	ps
t_{LOCK}		—	—	100	—	—	100	—	—	100	µs

In order to determine the transmitter timing requirements, mini-LVDS receiver timing requirements on the other end of the link must be taken into consideration. The mini-LVDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for mini-LVDS are shown in Figure 5–6.

Figure 5–6. mini-LVDS Transmitter AC Timing Specification

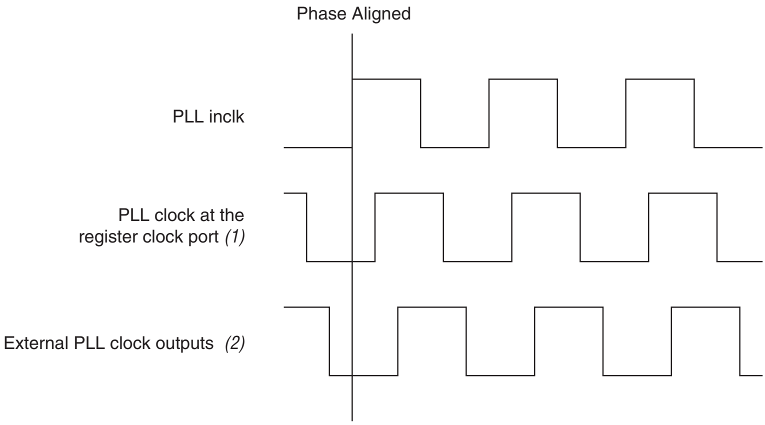


Notes to Figure 5–6:

(1) The data setup time, t_{SU}, is 0.225 × TUI.

(2) The data hold time, t_H, is 0.225 × TUI.

Figure 7–6. Phase Relationship between Cyclone II PLL Clocks in No Compensation Mode



Notes to Figure 7–6:
(1) Internal clocks fed by the PLL are in phase with each other.
(2) The external clock outputs can lead or lag the PLL internal clocks.

Source-Synchronous Mode

If data and clock arrive at the same time at the input pins, they are guaranteed to keep the same phase relationship at the clock and data ports of any IOE input register. Figure 7–7 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfer. Data and clock signals at the IOE experience similar buffer delays as long as the same I/O standard is used.

Table 7–8 shows the clock sources connectivity to the global clock networks.

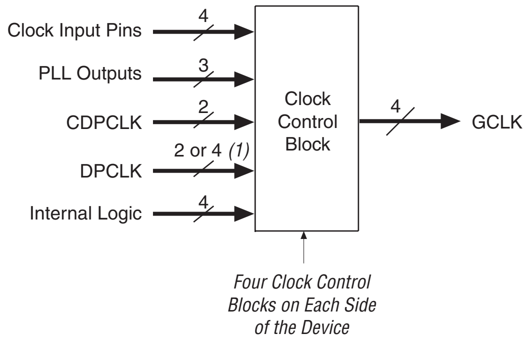
Table 7–8. Global Clock Network Connections (Part 1 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CLK0/LVDSCLK0p	✓		✓													
CLK1/LVDSCLK0n		✓	✓													
CLK2/LVDSCLK1p	✓			✓												
CLK3/LVDSCLK1n		✓		✓												
CLK4/LVDSCLK2p					✓		✓									
CLK5/LVDSCLK2n						✓	✓									
CLK6/LVDSCLK3p					✓			✓								
CLK7/LVDSCLK3n						✓		✓								
CLK8/LVDSCLK4n									✓		✓					
CLK9/LVDSCLK4p										✓	✓					
CLK10/LVDSCLK5n									✓			✓				
CLK11/LVDSCLK5p										✓		✓				
CLK12/LVDSCLK6n													✓		✓	
CLK13/LVDSCLK6p														✓	✓	
CLK14/LVDSCLK7n													✓			✓
CLK15/LVDSCLK7p														✓		✓
PLL1_c0	✓	✓		✓												
PLL1_c1	✓		✓	✓												
PLL1_c2		✓	✓													
PLL2_c0					✓	✓		✓								
PLL2_c1					✓		✓	✓								
PLL2_c2						✓	✓									
PLL3_c0									✓	✓		✓				
PLL3_c1									✓		✓	✓				
PLL3_c2										✓	✓					

From the clock sources listed above, only two clock input pins, two PLL clock outputs, one DPCLK or CDPCLK pin, and one source from internal logic can drive into any given clock control blocks, as shown in Figure 7–11. Out of these six inputs to any clock control block, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of the DPCLK or CDPCLK pin and the signal from internal logic.

Figure 7–13 shows the simplified version of the four clock control blocks on each side of the Cyclone II device periphery. The Cyclone II devices support up to 16 of these clock control blocks and this allows for up to a maximum of 16 global clocks in Cyclone II devices.

Figure 7–13. Clock Control Blocks on Each Side of the Cyclone II Device



Note to Figure 7–13:

(1) The left and right sides of the device have two DPCLK pins, and the top and bottom of the device have four DPCLK pins.

Global Clock Network Power Down

The Cyclone II global clock network can be disabled (powered down) by both static and dynamic approaches. When a clock network is powered down, all the logic fed by the clock network is in an off-state, thereby reducing the overall power consumption of the device.

The global clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable or disable feature allows internal logic to synchronously control power up or down on the global clock networks in the Cyclone II device. This function is independent of the PLL and is applied directly on the clock network, as shown in Figure 7–11. The input

In addition, the clock networks in the Cyclone II device support dynamic selection of the clock source and also support a power-down mode where clock networks that are not being used can easily be turned off, reducing the overall power consumption of the device.

Table 8–2. Number of M4K Blocks in Cyclone II Devices (Part 2 of 2)

Device	M4K Blocks	Total RAM Bits
EP2C50	129	594,432
EP2C70	250	1,152,000

Control Signals

Figure 8–1 shows how the register clocks, clears, and control signals are implemented in the Cyclone II memory block.

The clock enable control signal controls the clock entering the entire memory block, not just the input and output registers. The signal disables the clock so that the memory block does not see any clock edges and will not perform any operations.

Cyclone II devices do not support asynchronous clear signals to input registers. Only output registers support asynchronous clears. There are three ways to reset the registers in the M4K blocks: power up the device, use the `aclr` signal for output register only, or assert the device-wide reset signal using the `DEV_CLRn` option.

☞ When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

1.8-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-7)

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts.

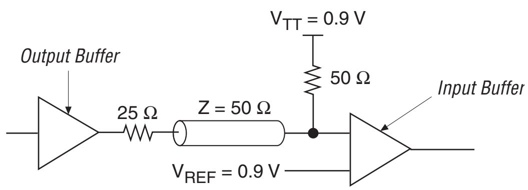
The 1.8-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.8-V LVCMOS.

SSTL-18 Class I and II

The 1.8-V SSTL-18 standard is formulated under JEDEC Standard, JESD815: Stub Series Terminated Logic for 1.8V (SSTL-18).

The SSTL-18 I/O standard is a 1.8-V memory bus standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V V_{REF} and a 0.9-V V_{TT}, with the termination resistors connected to both. There are no class definitions for the SSTL-18 standard in the JEDEC specification. The specification of this I/O standard is based on an environment that consists of both series and parallel terminating resistors. Altera provides solutions to two derived applications in JEDEC specification and names them class I and class II to be consistent with other SSTL standards. Figures 10–5 and 10–6 show SSTL-18 class I and II termination, respectively. Cyclone II devices support both input and output levels.

Figure 10–5. 1.8-V SSTL Class I Termination



After applying the equation above, apply one of the equations in Table 10–11, depending on the package type.

Table 10–11. Bidirectional Pad Limitation Formulas (Multiple V_{REF} Inputs and Outputs)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of output pads) ≤9 (per VCCIO/GND pair)
QFP	Total number of bidirectional pads + Total number of output pads ≤5 (per VCCIO/GND pair)

Each I/O bank can only be set to a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible V_{CCIO} values (refer to Table 10–4 for more details) and compatible V_{REF} voltage levels.

DDR and QDR Pads

For dedicated DQ and DQS pads on a DDR interface, DQ pads have to be on the same power bank as DQS pads. With the DDR and DDR2 memory interfaces, a `VCCIO` and ground pair can have a maximum of five DQ pads.

For a QDR interface, D is the QDR output and Q is the QDR input. D pads and Q pads have to be on the same power bank as CQ. With the QDR and QDRII memory interfaces, a `VCCIO` and ground pair can have a maximum of five D and Q pads.

By default, the Quartus II software assigns D and Q pads as regular I/O pins. If you do not specify the function of a D or Q pad in the Quartus II software, the software sets them as regular I/O pins. If this occurs, Cyclone II QDR and QDRII performance is not guaranteed.

DC Guidelines

There is a current limit of 240 mA per eight consecutive output top and bottom pins per power pair, as shown by the following equation:

$$\sum_{pin}^{pin+7} I_{PIN} < 240mA \text{ per power pair}$$

There is a current limit of 240 mA per 12 consecutive output side (left and right) pins per power pair, as shown by the following equation:

Referenced Documents

This chapter references the following documents:

- *Altera Reliability Report*
- *AN 75: High-Speed Board Designs*
- *Cyclone II Architecture* chapter in volume 1 of the *Cyclone II Device Handbook*
- *Cyclone II Device Family Data Sheet, section 1* of the *Cyclone II Device Handbook*
- *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*
- *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*
- *High Speed Differential Interfaces in Cyclone II Devices* chapter in volume 1 of the *Cyclone II Device Handbook*
- *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*
- *I/O Management* chapter in volume 2 of the *Quartus II Handbook*

Document Revision History

Table 10–13 shows the revision history for this document.

Table 10–13. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2008 v2.4	• Added "Referenced Documents" section. • Updated "Differential Pad Placement Guidelines" section.	—
February 2007 v2.3	• Added document revision history. • Updated "Introduction" and its feetpara note. • Updated *Note (2)* in Table 10–4. • Updated "Differential LVPECL" section. • Updated "Differential Pad Placement Guidelines" section. • Updated "Output Pads" section. • Added new section "5.0-V Device Compatibility" with two new figures.	• Added reference detail for ESD specifications. • Added information about differential placement restrictions applying only to pins in the same bank. • Added information that Cyclone II device supports LVDS on clock inputs at 3.3V V_{CCIO}. • Added more information on DC placement guidelines. • Added information stating SSTL and HSTL outputs can be closer than 2 pads from V_{REF}. • Added 5.0 Device tolerence solution.

Table 13–1. Cyclone II Configuration Schemes

Configuration Scheme	MSEL1	MSEL0
AS (20 MHz)	0	0
PS	0	1
Fast AS (40 MHz) *(1)*	1	0
JTAG-based Configuration *(2)*	*(3)*	*(3)*

Notes to Table 13–1:

(1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

(2) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

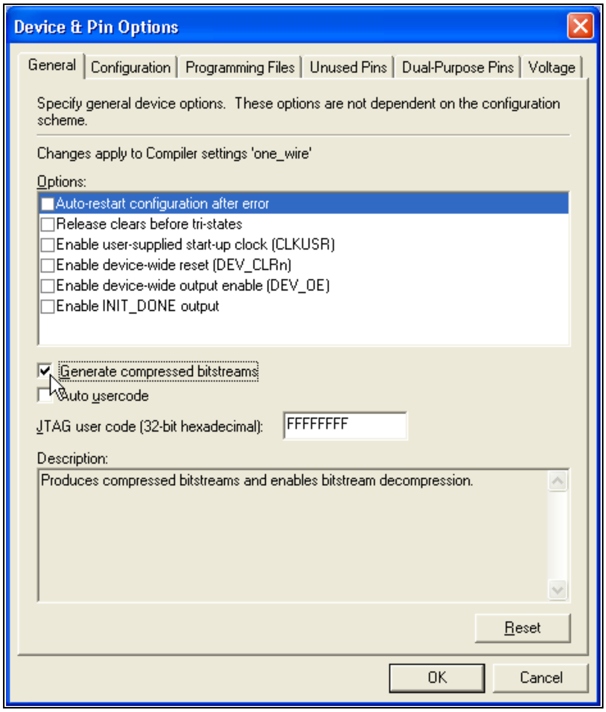
(3) Do not leave the MSEL pins floating; connect them to V_{CCIO} or ground. These pins support the non-JTAG configuration scheme used in production. If you are only using JTAG configuration, you should connect the MSEL pins to ground.

You can download configuration data to Cyclone II FPGAs with the AS, PS, or JTAG interfaces using the options in Table 13–2.

Table 13–2. Cyclone II Device Configuration Schemes

Configuration Scheme	Description
AS configuration	Configuration using serial configuration devices (EPCS1, EPCS4, EPCS16 or EPCS64 devices)
PS configuration	Configuration using enhanced configuration devices (EPC4, EPC8, and EPC16 devices), EPC2 and EPC1 configuration devices, an intelligent host (microprocessor), or a download cable
JTAG-based configuration	Configuration via JTAG pins using a download cable, an intelligent host (microprocessor), or the Jam™ Standard Test and Programming Language (STAPL)

Figure 13–1. Enabling Compression for Cyclone II Bitstreams in Compiler Settings



You can also use the following steps to enable compression when creating programming files from the Convert Programming Files window.

1. Click **Convert Programming Files** (File menu).

2. Select the Programming File type. Only Programmer Object Files (**.pof**), SRAM HEXOUT, RBF, or TTF files support compression.

3. For POFs, select a configuration device.

4. Select **Add File** and add a Cyclone II SRAM Object File(s) (**.sof**).

5. Select the name of the file you added to the SOF Data area and click on **Properties**.

6. Check the **Compression** check box.

Reset Stage

When nCONFIG or nSTATUS are low, the device is in reset. After POR, the Cyclone II device releases nSTATUS. An external 10-kΩ pull-up resistor pulls the nSTATUS signal high, and the Cyclone II device enters configuration mode.

☞ V_{CCINT} and V_{CCIO} of the banks where the configuration and JTAG pins reside need to be fully powered to the appropriate voltage levels in order to begin the configuration process.

Configuration Stage

The serial clock (DCLK) generated by the Cyclone II device controls the entire configuration cycle and provides the timing for the serial interface. Cyclone II devices use an internal oscillator to generate DCLK. Using the MSEL[] pins, you can select either a 20- or 40-MHz oscillator. Although you can select either 20- or 40-MHz oscillator when designing with serial configuration devices, the 40-MHz oscillator provides faster configuration times. There is some variation in the internal oscillator frequency because of the process, temperature, and voltage conditions in Cyclone II devices. The internal oscillator is designed such that its maximum frequency is guaranteed to meet EPCS device specifications.

Table 13–5 shows the AS DCLK output frequencies.

Table 13–5. AS DCLK Output Frequency *Note (1)*

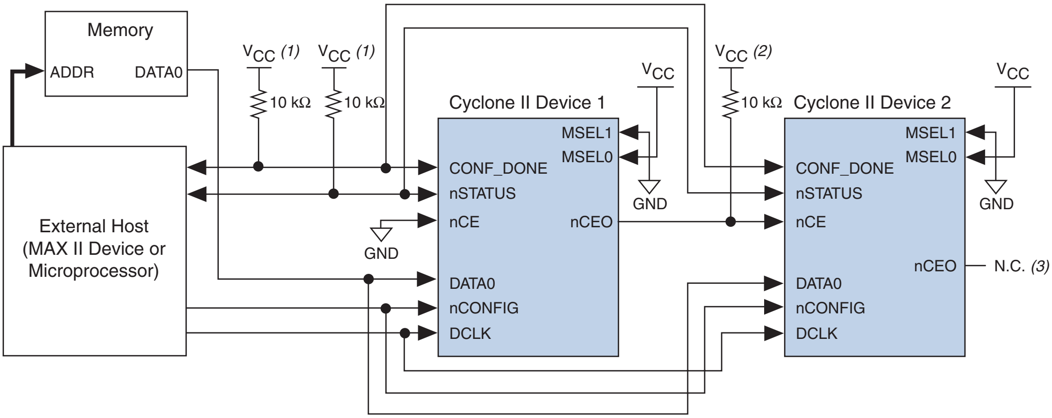
Oscillator Selected	Minimum	Typical	Maximum	Units
40 MHz	20	26	40	MHz
20 MHz	10	13	20	MHz

Note to Table 13–5:
(1) These values are preliminary.

In both AS and Fast AS configuration schemes, the serial configuration device latches input and control signals on the rising edge of DCLK and drives out configuration data on the falling edge. Cyclone II devices drive out control signals on the falling edge of DCLK and latch configuration data on the falling edge of DCLK.

In configuration mode, the Cyclone II device enables the serial configuration device by driving its nCSO output pin low, which connects to the chip select (nCS) pin of the configuration device. The Cyclone II device uses the serial clock (DCLK) and serial data output (ASDO) pins to send operation commands and/or read address signals to the serial

Figure 13–10. Multiple Device PS Configuration Using an External Host



Notes to Figure 13–10:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

In multiple device PS configuration, connect the first Cyclone II device's nCE pin to GND and connect the nCEO pin to the nCE pin of the next Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's nCEO pin high to its V_{CCIO} level to help the internal weak pull-up resistor when the nCEO pin feeds next Cyclone II device's nCE pin. The input to the nCE pin of the last Cyclone II device in the chain comes from the previous Cyclone II device. After the first device completes configuration in a multiple device configuration chain, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle. Therefore, the MAX II device begins to transfer data to the next Cyclone II device without interruption. The nCEO pin is a dual-purpose pin in Cyclone II devices. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in chain is a Cyclone II device.

☞ The Quartus II software sets the Cyclone II device nCEO pin as a dedicated output by default. If the nCEO pin feeds the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

The Quartus II software sets the Cyclone II device `nCEO` pin as an output pin driving to ground by default. If the `nCEO` pin inputs to the next device's `nCE` pin, make sure that the `nCEO` pin is not used as a user I/O pin after configuration.

Other Altera devices that have JTAG support can be placed in the same JTAG chain for device programming and configuration.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP). Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information on JTAG and Jam STAPL in embedded environments, see *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*. To download the Jam player, go to the Altera web site (**www.altera.com**).

Configuring Cyclone II FPGAs with JRunner

JRunner is a software driver that allows you to configure Cyclone II devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in **.rbf** format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

The RBF file used by the JRunner software driver can not be a compressed RBF file because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

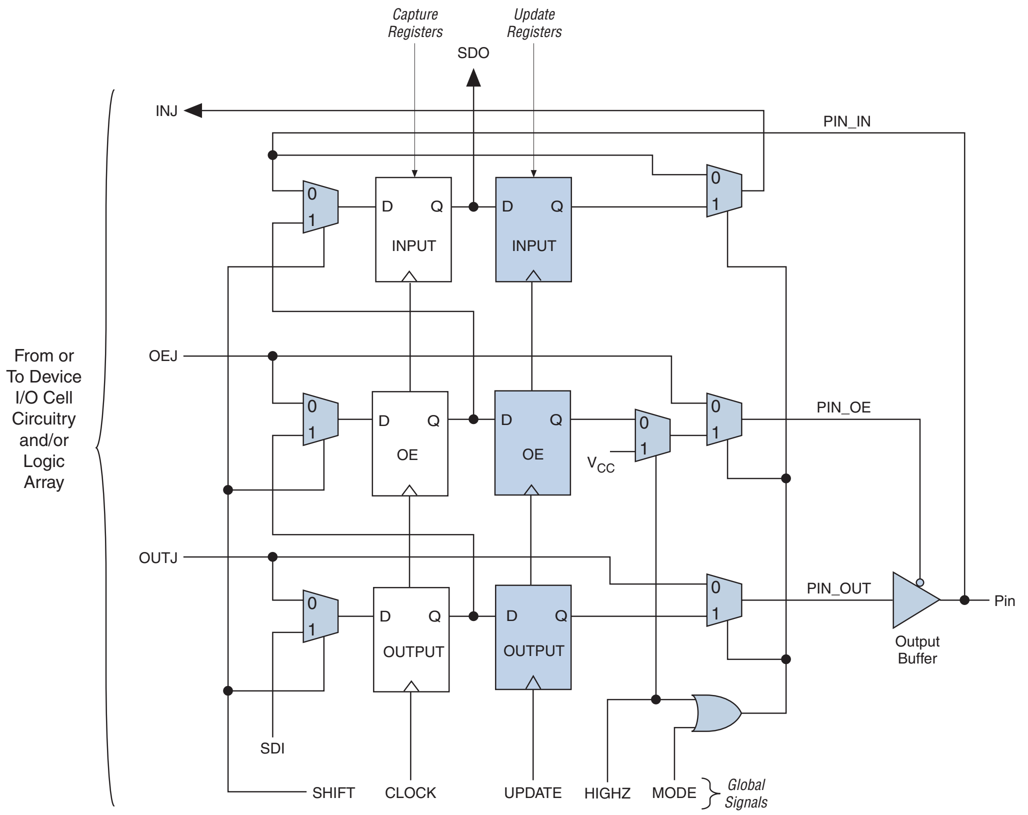
For more information on the JRunner software driver, see *JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site.

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)				
Pin Name	**User Mode**	**Configuration Scheme**	**Pin Type**	**Description**
nCEO	N/A if option is on. I/O if option is off.	All	Output	This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration. If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. Use the Quartus II software to make this pin a user I/O pin.
ASDO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data. In AS mode, ASDO has an internal pull-up that is always active.
nCSO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

to external device data via the PIN_IN signal, while the update registers connect to external data through the PIN_OUT and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 14–4 shows the Cyclone II device's user I/O boundary-scan cell.

Figure 14–4. Cyclone II Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry



256-Pin FineLine Ball-Grid Array, Option 2 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

☞ This POD is applicable to the F256 package of the Cyclone II product only.

Tables 15–11 and 15–12 show the package information and package outline figure references, respectively, for the 256-pin FineLine BGA package.

Table 15–11. 256-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MO-192 Variation: AAF-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	1.9 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–12. 256-Pin FineLine BGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	1.55
A1	0.25	–	–
A2	1.05 REF		
A3	–	–	0.80
D	17.00 BSC		
E	17.00 BSC		
b	0.40	0.50	0.55
e	1.00 BSC		

Figure 15–4 shows a 256-pin FineLine BGA package outline.

Figure 15–4. 256-Pin FineLine BGA Package Outline