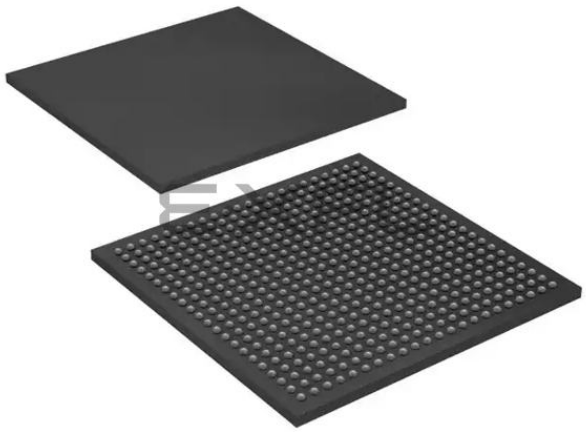

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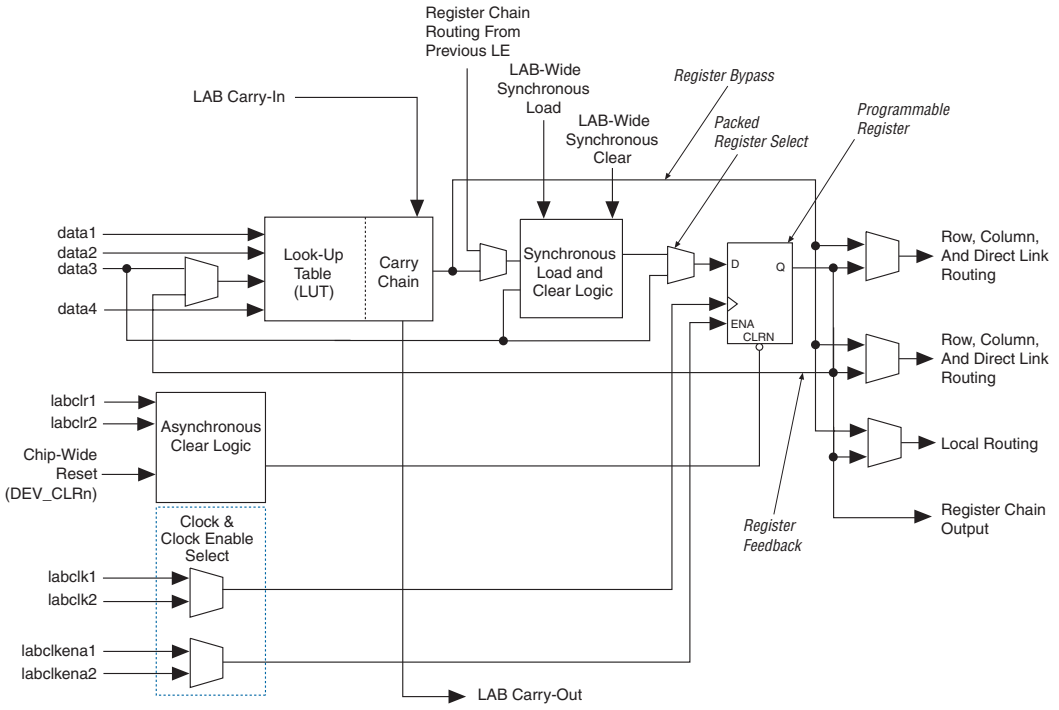
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1172
Number of Logic Elements/Cells	18752
Total RAM Bits	239616
Number of I/O	315
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c20f484c7

Figure 2–2 shows a Cyclone II LE.

Figure 2–2. Cyclone II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, clock, clock enable, and clear inputs. Signals that use the global clock network, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources, allowing the LUT to drive one output while the register drives another output. This feature, register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. When using register packing, the LAB-wide synchronous load control signal is not available. See "LAB Control Signals" on page 2–8 for more information.

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{CONF} *(5) (6)*	Value of I/O pin pull-up resistor before and during configuration	V_{IN} = 0 V; V_{CCIO} = 3.3 V	10	25	50	kΩ
		V_{IN} = 0 V; V_{CCIO} = 2.5 V	15	35	70	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.8 V	30	50	100	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.5 V	40	75	150	kΩ
		V_{IN} = 0 V; V_{CCIO} = 1.2 V	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	*(7)*	—	1	2	kΩ

Notes to Table 5–3:

(1) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltages shown in Table 5–4, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(3) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(4) Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (www.altera.com) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to "Power Consumption" on page 5–13 for more information.

(5) R_{CONF} values are based on characterization. $R_{CONF} = V_{CCIO}/I_{RCONF}$. R_{CONF} values may be different if V_{IN} value is not 0 V. Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

(6) Minimum condition at –40°C and high V_{CC}, typical condition at 25°C and nominal V_{CC} and maximum condition at 125°C and low V_{CC} for R_{CONF} values.

(7) These values apply to all V_{CCIO} settings.

Table 5–4 shows the maximum V_{IN} overshoot voltage and the dependency on the duty cycle of the input signal. Refer to Table 5–3 for more information.

Table 5–4. V_{IN} Overshoot Voltage for All Input Buffers

Maximum V_{IN} (V)	Input Signal Duty Cycle
4.0	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

I/O Delays

Refer to Tables 5–39 through 5–43 for I/O delays.

Table 5–39. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 1 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
LVTTL	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
2.5V	t_{PI}	624	654	1192	1238	1283	1283	ps
	t_{PCOUT}	410	430	730	793	855	855	ps
1.8V	t_{PI}	725	760	1372	1428	1484	1484	ps
	t_{PCOUT}	511	536	910	983	1056	1056	ps
1.5V	t_{PI}	790	828	1439	1497	1556	1556	ps
	t_{PCOUT}	576	604	977	1052	1128	1128	ps
LVCMOS	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
SSTL_2_CLASS_I	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_2_CLASS_II	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_18_CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
SSTL_18_CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 5 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
DIFFERENTIAL_ SSTL_18_CLASS_I	6 mA	t_{OP}	1472	1544	3140	3345	3542	3549	ps
		t_{DIP}	1604	1683	3310	3539	3768	3768	ps
	8 mA	t_{OP}	1469	1541	3086	3287	3482	3489	ps
		t_{DIP}	1601	1680	3256	3481	3708	3708	ps
	10 mA	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
	12 mA (1)	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
DIFFERENTIAL_ SSTL_18_CLASS_II	16 mA	t_{OP}	1454	1525	2905	3088	3263	3270	ps
		t_{DIP}	1586	1664	3075	3282	3489	3489	ps
	18 mA (1)	t_{OP}	1453	1524	2900	3082	3257	3264	ps
		t_{DIP}	1585	1663	3070	3276	3483	3483	ps
1.8V_DIFFERENTIAL _HSTL_CLASS_I	8 mA	t_{OP}	1460	1531	3222	3424	3618	3625	ps
		t_{DIP}	1592	1670	3392	3618	3844	3844	ps
	10 mA	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
	12 mA (1)	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
1.8V_DIFFERENTIAL _HSTL_CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_DIFFERENTIAL _HSTL_CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 4 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
LVDS	—	t_{OP}	1216	1275	2089	2184	2272	2278	ps
		t_{DIP}	1340	1407	2297	2421	2545	2545	ps
RSDS	—	t_{OP}	1216	1275	2089	2184	2272	2278	ps
		t_{DIP}	1340	1407	2297	2421	2545	2545	ps
MINI_LVDS	—	t_{OP}	1216	1275	2089	2184	2272	2278	ps
		t_{DIP}	1340	1407	2297	2421	2545	2545	ps
PCI	—	t_{OP}	989	1036	2070	2214	2352	2358	ps
		t_{DIP}	1113	1168	2278	2451	2625	2625	ps
PCI-X	—	t_{OP}	989	1036	2070	2214	2352	2358	ps
		t_{DIP}	1113	1168	2278	2451	2625	2625	ps

Notes to Table 5–43:
(1) This is the default setting in the Quartus II software.
(2) These numbers are for commercial devices.
(3) These numbers are for automotive devices.

Maximum Input and Output Clock Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 5–44 specifies the maximum input clock toggle rates. Table 5–45 specifies the maximum output clock toggle rates at default load. Table 5–46 specifies the derating factors for the output clock toggle rate for non-default load.

To calculate the output toggle rate for a non-default load, use this formula:

The toggle rate for a non-default load

Tables 5–50 and 5–51 show the LVDS timing budget for Cyclone II devices. Cyclone II devices support LVDS receivers at data rates up to 805 Mbps, and LVDS transmitters at data rates up to 640 Mbps.

Table 5–50. LVDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
		Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	
f_{HSCLK} (input clock frequency)	×10	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×8	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×7	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×4	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×2	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (8)	402.5 (8)	MHz
HSIODR	×10	100	—	640	640	100	—	550	640	100	—	311 (5)	550 (7)	Mbps
	×8	80	—	640	640	80	—	550	640	80	—	311 (5)	550 (7)	Mbps
	×7	70	—	640	640	70	—	550	640	70	—	311 (5)	550 (7)	Mbps
	×4	40	—	640	640	40	—	550	640	40	—	311 (5)	550 (7)	Mbps
	×2	20	—	640	640	20	—	550	640	20	—	311 (5)	550 (7)	Mbps
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (9)	402.5 (9)	Mbps
t_{DUTY}	—	45	—	55	—	45	—	55	—	45	—	55	—	%
	—	—	—	—	160	—	—	—	312.5	—	—	—	363.6	ps
TCCS (3)	—	—	—	200		—	—	200		—	—	200		ps
Output jitter (peak to peak)	—	—	—	500		—	—	500		—	—	550 (10)		ps
t_{RISE}	20–80%	150	200	250		150	200	250		150	200	250 (11)		ps

Table 5–54. PLL Specifications Note (1) (Part 2 of 2)

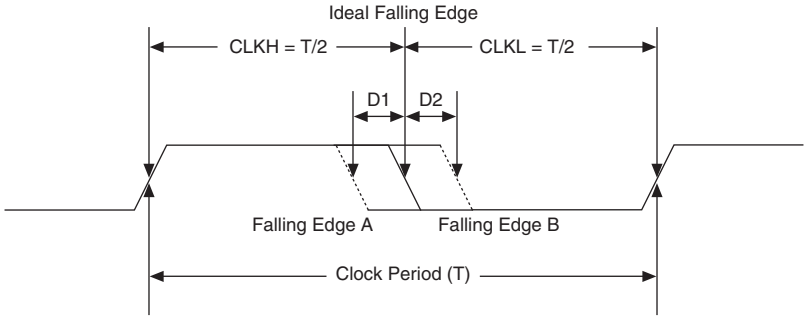
Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO} (3)	PLL internal VCO operating range	300	—	1,000	MHz
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns

Notes to Table 5–54:
(1) These numbers are preliminary and pending silicon characterization.
(2) The t_{JITTER} specification for the PLL[4..1]_OUT pins are dependent on the I/O pins in its VCCIO bank, how many of them are switching outputs, how much they toggle, and whether or not they use programmable current strength.
(3) If the VCO post-scale counter = 2, a 300- to 500-MHz internal VCO frequency is available.
(4) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
(5) Cyclone II PLLs can track a spread-spectrum input clock that has an input jitter within ±200 ps.
(6) For extended temperature devices, the maximum lock time is 500 us.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 5–8. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (Figure 5–8). The maximum DCD for a clock is the larger value of D1 and D2.

Figure 5–8. Duty Cycle Distortion



DCD expressed in absolution derivation, for example, D1 or D2 in Figure 5–8, is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as:

Figure 8–4. Cyclone II Address Clock Enable During Read Cycle Waveform

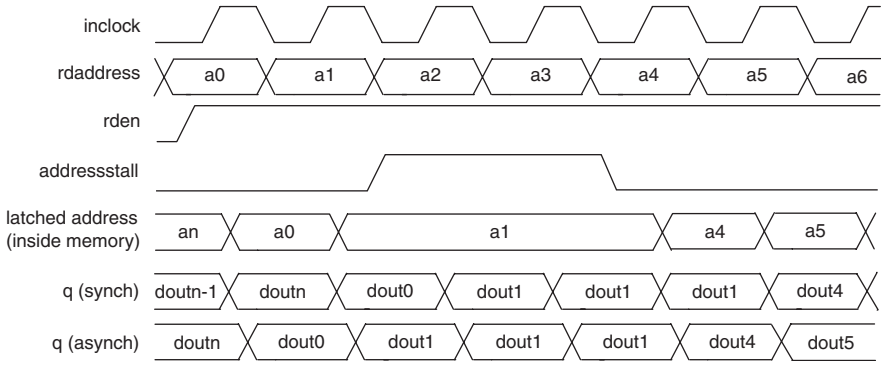
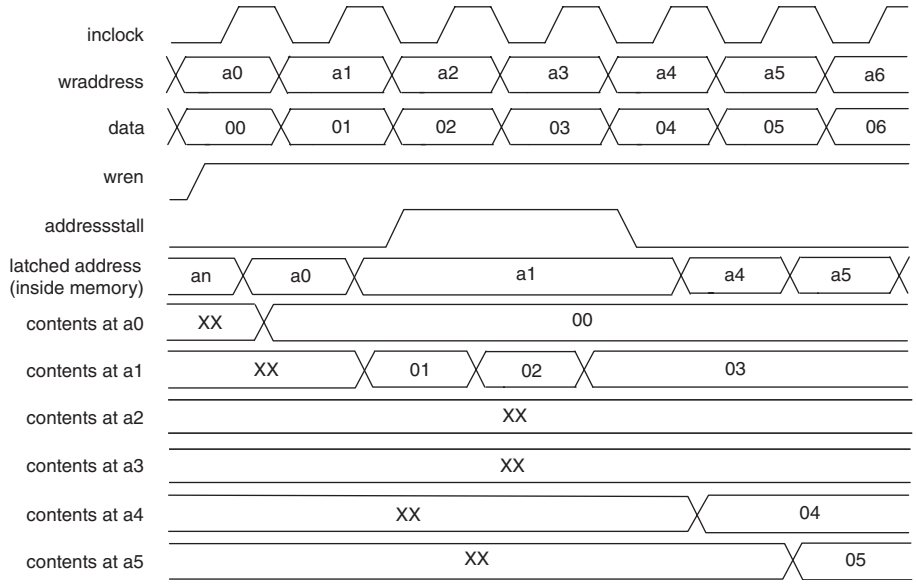


Figure 8–5. Cyclone II Address Clock Enable During Write Cycle Waveform



Memory Modes

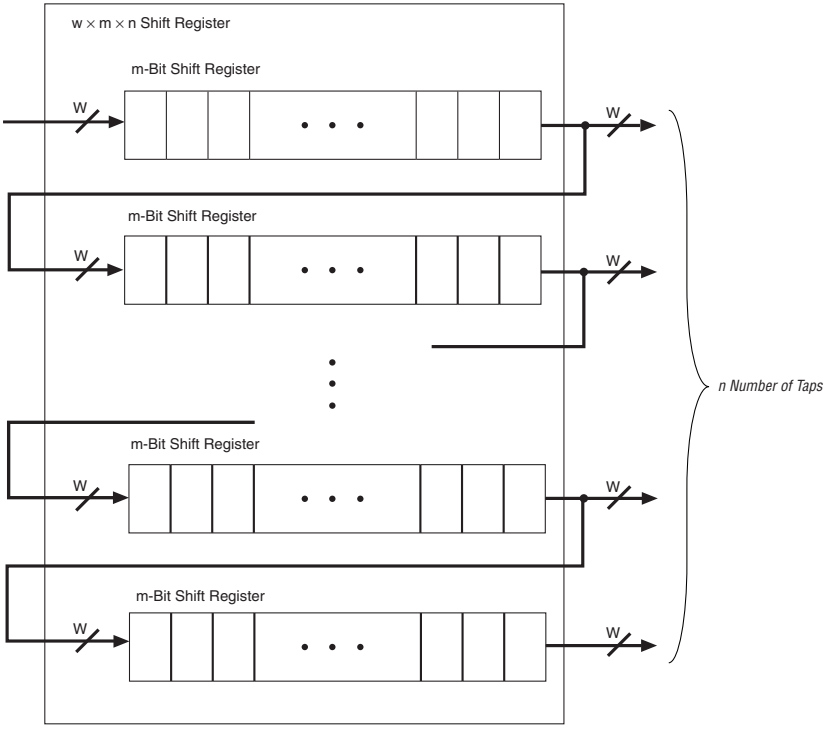
Cyclone II M4K memory blocks include input registers that synchronize writes and output registers to pipeline data, thereby improving system performance. All M4K memory blocks are fully synchronous, meaning that you must send all inputs through a register, but you can either send outputs through a register (pipelined) or bypass the register (flow-through).

applications require local data storage, traditionally implemented with standard flip-flops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources.

The size of a ($w \times m \times n$) shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n), and must be less than or equal to the maximum number of memory bits, which is 4,608 bits. In addition, the size of ($w \times n$) must be less than or equal to the maximum width of the block, which is 36 bits. If a larger shift register is required, the memory blocks can be cascaded.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 8–12 shows the Cyclone II memory block in the shift register mode.

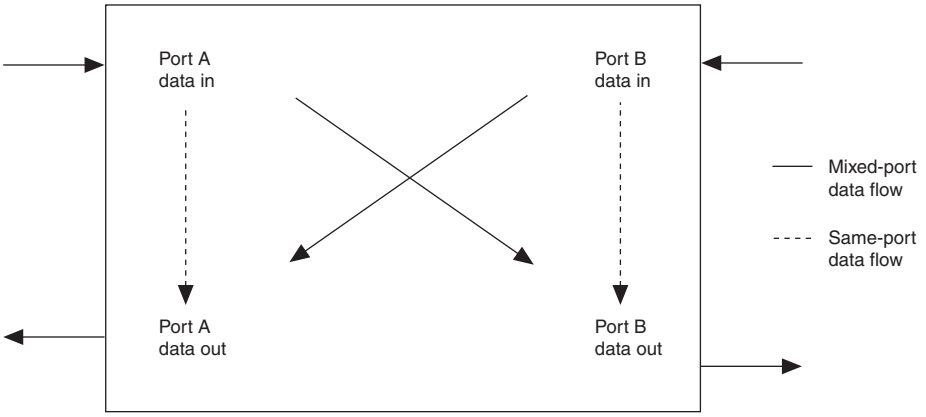
Figure 8–12. Cyclone II Shift Register Mode Configuration



Read-During-Write Operation at the Same Address

The "Same-Port Read-During-Write Mode" and "Mixed-Port Read-During-Write Mode" sections describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two read-during-write data flows: same-port and mixed-port. Figure 8–21 shows the difference between these flows.

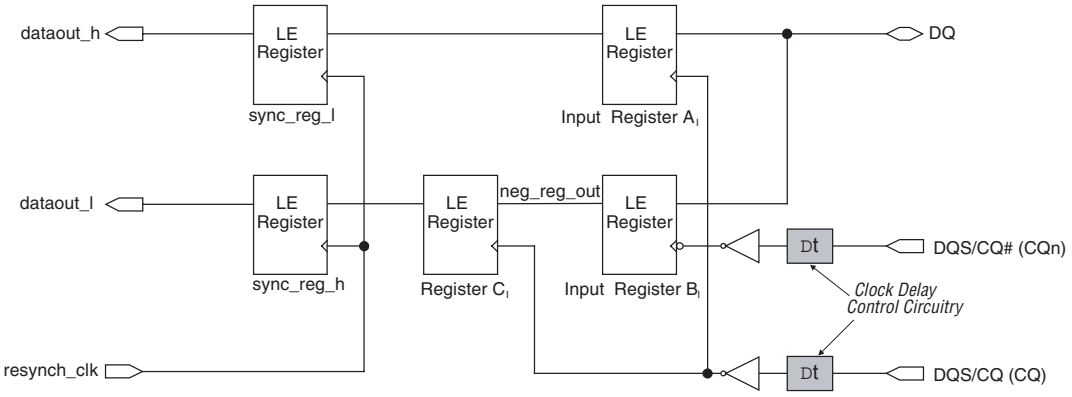
Figure 8–21. Cyclone II Read-During-Write Data Flow



Same-Port Read-During-Write Mode

For read-during-write operation of a single-port RAM or the same port of a true dual-port RAM, the new data is available on the rising edge of the same clock cycle on which it was written. Figure 8–22 shows a sample functional waveform. When using byte enables in true dual-port RAM mode, the outputs for the masked bytes on the same port are unknown (see Figure 8–2 on page 8–6). The non-masked bytes are read out as shown in Figure 8–22.

Figure 9–4. CQ & CQn Connection for QDRII SRAM Read



Read & Write Operation

Figure 9–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDRII SRAM devices send data within t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQn clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Cyclone II devices.

Table 10–6. Programmable Drive Strength (Part 2 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Side I/O Pins
SSTL-2 class I	8	8
	12	12
SSTL-2 class II	16	16
	20	—
	24	—
SSTL-18 class I	6	6
	8	8
	10	10
	12	—
SSTL-18 class II	16	—
	18	—
HSTL-18 class I	8	8
	10	10
	12	12
HSTL-18 class II	16	N/A
	18	—
	20	—
HSTL-15 class I	8	8
	10	—
	12	—
HSTL-15 class II	16	N/A

These drive-strength settings are programmable on a per-pin basis using the Quartus II software.

V_{REF} Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply and to prevent output switching noise from shifting the V_{REF} rail, there are restrictions on the placement of single-ended voltage referenced I/Os with respect to V_{REF} pads and VCCIO and ground pairs. Use the following guidelines for placing single-ended pads in Cyclone II devices.

The Quartus II software automatically does all the calculations in this section.

Input Pads

Each V_{REF} pad supports up to 15 input pads on each side of the V_{REF} pad for FineLine BGA devices. Each V_{REF} pad supports up to 10 input pads on each side of the V_{REF} pad for quad flat pack (QFP) devices. This is irrespective of VCCIO and ground pairs, and is guaranteed by the Cyclone II architecture.

Output Pads

When a voltage referenced input or bidirectional pad does not exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each VCCIO and ground pair supports 9 output pins for Fineline BGA packages (not more than 9 output pins per 12 consecutive row I/O pins) or 5 output pins for QFP packages (not more than 5 output pins per 12 consecutive row I/O pins or 8 consecutive column I/O pins). Any non-SSTL and non-HSTL output can be no closer than two pads away from a V_{REF} pad. Altera recommends that any SSTL or HSTL output, except for pintable defined DQ and DQS outputs, to be no closer than two pads away from a V_{REF} pad to maintain acceptable noise levels.

Quartus II software will not check for the SSTL and HSTL output pads placement rule.

Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

Bidirectional Pads

Bidirectional pads must satisfy input and output guidelines simultaneously.

Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

pin+11
$\Sigma I_{PIN} < 240mA$ per power pair
pin

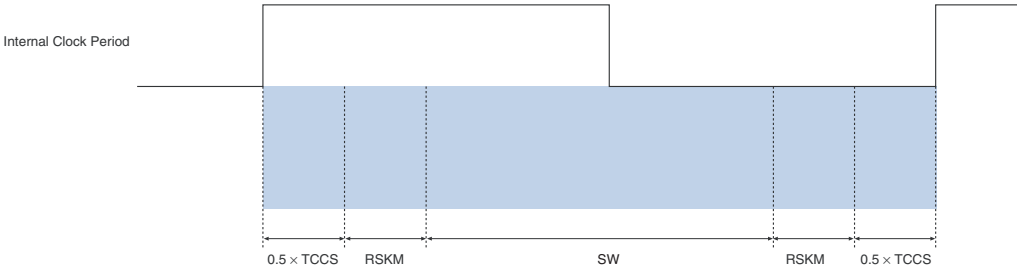
In all cases listed above, the Quartus II software generates an error message for illegally placed pads.

Table 10–12 shows the I/O standard DC current specification.

Table 10–12. Cyclone II I/O Standard DC Current Specification (Preliminary) (Part 1 of 2)

I/O Standard	I_{PIN} (mA)	
	Top and Bottom Banks	Side Banks
LVTTL	*(1)*	*(1)*
LVCMOS	*(1)*	*(1)*
2.5 V	*(1)*	*(1)*
1.8 V	*(1)*	*(1)*
1.5 V	*(1)*	*(1)*
3.3-V PCI	Not supported	1.5
3.3-V PCI-X	Not supported	1.5
SSTL-2 class I	12 *(2)*	12 *(2)*
SSTL-2 class II	24 *(2)*	20 *(2)*
SSTL-18 class I	12 *(2)*	12 *(2)*
SSTL-18 class II	8 *(2)*	Not supported
1.8-V HSTL class I	12 *(2)*	12 *(2)*
1.8-V HSTL class II	20 *(2)*	Not supported
1.5-V HSTL class I	12 *(2)*	10 *(2)*
1.5-V HSTL class II	18 *(2)*	Not supported
Differential SSTL-2 class I *(3)*	8.1 *(4)*	
Differential SSTL-2 class II *(3)*	16.4 *(4)*	
Differential SSTL-18 class I *(3)*	6.7 *(4)*	
Differential SSTL-18 class II *(3)*	13.4 *(4)*	
1.8-V differential HSTL class I *(3)*	8 *(4)*	
1.8-V differential HSTL class II *(3)*	16 *(4)*	
1.5-V differential HSTL class I *(3)*	8 *(4)*	

Figure 11–17. Cyclone II High-Speed I/O Timing Budget *Note (1)*



Note to Figure 11–17:
(1) The equation for the high-speed I/O timing budget is: Period = 0.5/TCCS + RSKM + SW + RSKM + 0.5/TCCS.

Design Guidelines

This section provides guidelines for designing with Cyclone II devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pins in relation to differential pads.

See the guidelines in the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook* for placing single-ended pads with respect to differential pads in Cyclone II devices.

Board Design Considerations

This section explains how to get the optimal performance from the Cyclone II I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. The critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques must be considered to get the best performance from the IC. The Cyclone II device generates signals that travel over the media at frequencies as high as 805 Mbps. Use the following general guidelines for improved signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.

Document Revision History

Table 12–4 shows the revision history for this document.

Table 12–4. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v1.2	• Added document revision history. • Updated "Software Support" section.	• Removed reference to third-party synthesis tool: LeonardoSpectrum and Synplify.
November 2005 v2.1	Updated Introduction.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Although they both use the same compression algorithm, the decompression feature supported by Cyclone II devices is different from the decompression feature in enhanced configuration devices (EPC16, EPC8, and EPC4 devices). The data decompression feature in the enhanced configuration devices allows them to store compressed data and decompress the bitstream before transmitting it to the target devices.

In PS mode, you should use the Cyclone II decompression feature since sending compressed configuration data reduces configuration time. You should not use both the Cyclone II device and the enhanced configuration device decompression features simultaneously. The compression algorithm is not intended to be recursive and could expand the configuration file instead of compressing it further.

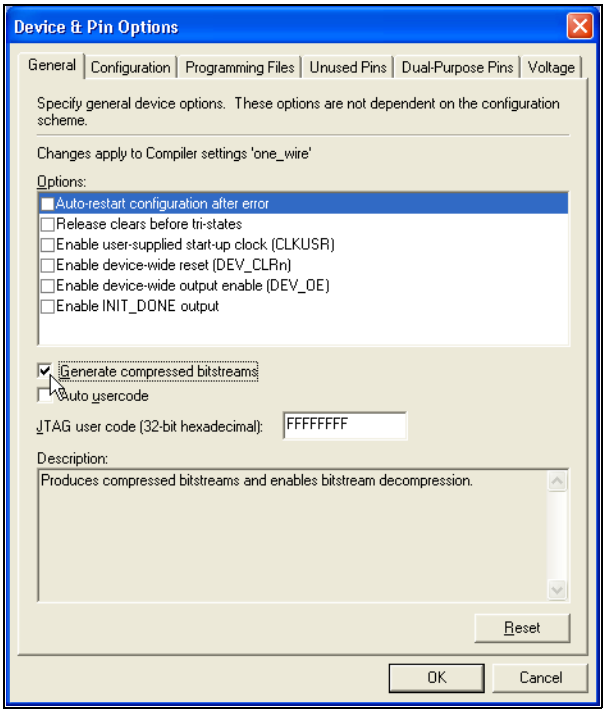
You should use the Cyclone II decompression feature during AS configuration if you need to save configuration memory space in the serial configuration device.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash, and decreases the time needed to transmit the bitstream to the Cyclone II device. The time required by a Cyclone II device to decompress a configuration file is less than the time needed to transmit the configuration data to the FPGA.

There are two methods to enable compression for Cyclone II bitstreams: before design compilation (in the Compiler Settings menu) and after design compilation (in the **Convert Programming Files** window).

To enable compression in the project's compiler settings, select **Device** under the Assignments menu to bring up the settings window. After selecting your Cyclone II device open the **Device & Pin Options** window, and in the **General settings** tab enable the check box for **Generate compressed bitstreams** (see Figure 13–1).

Figure 13–1. Enabling Compression for Cyclone II Bitstreams in Compiler Settings



You can also use the following steps to enable compression when creating programming files from the Convert Programming Files window.

1. Click **Convert Programming Files** (File menu).
2. Select the Programming File type. Only Programmer Object Files (**.pof**), SRAM HEXOUT, RBF, or TTF files support compression.
3. For POFs, select a configuration device.
4. Select **Add File** and add a Cyclone II SRAM Object File(s) (**.sof**).
5. Select the name of the file you added to the SOF Data area and click on **Properties**.
6. Check the **Compression** check box.

Disabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Cyclone II devices is enabled upon device power-up. Because this circuitry may be used for BST or in-circuit reconfiguration, this circuitry must be enabled only at specific times as mentioned in "Using IEEE Std. 1149.1 BST Circuitry" on page 14–16.

If the IEEE Std. 1149.1 circuitry will not be utilized at any time, the circuitry should be permanently disabled. Table 14–3 shows the pin connections necessary for disabling the IEEE Std. 1149.1 circuitry in Cyclone II devices to ensure that the circuitry is not inadvertently enabled when it is not needed.

Table 14–3. Disabling IEEE Std. 1149.1 Circuitry

JTAG Pins *(1)*	Connection for Disabling
TMS	V_{CC}
TCK	GND
TDI	V_{CC}
TDO	Leave open

Note to Table 14–3:
(1) There is no software option to disable JTAG in Cyclone II devices. The JTAG pins are dedicated.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If the 10-bit checkerboard pattern "1010101010" does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the TAP controller has not reached the proper state. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and send the code 01100 to the TMS pin.
  - Check the connections to the V_{CC}, GND, JTAG, and dedicated configuration pins on the device.

484-Pin Ultra FineLine BGA – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 15–15 and 15–16 show the package information and package outline figure references, respectively, for the 484-pin Ultra FineLine BGA package.

Table 15–15. 484-Pin Ultra FineLine BGA Package Information

Description	Specification
Ordering Code Reference	U
Package Acronym	UBGA
Substrate Material	BT
Solder Ball Composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MO-216 Variation: BAP-2
Maximum Lead Coplanarity	0.005 inches (0.12mm)
Weight	1.8 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Table 15–16. 484-Pin Ultra FineLine BGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	2.20
A1	0.20	–	–
A2	0.65	–	–
A3	0.80 TYP		
D	19.00 BSC		
E	19.00 BSC		
b	0.40	0.50	0.60
e	0.80 BSC		