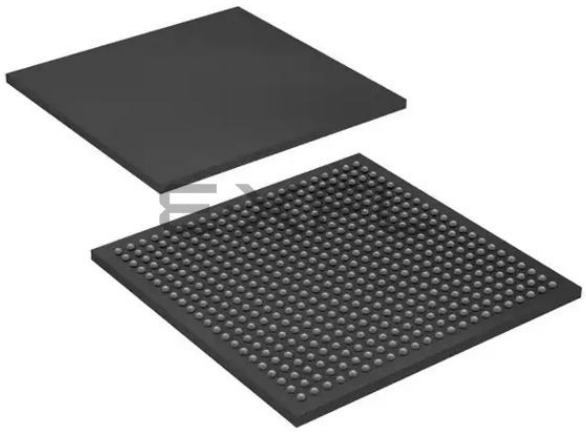

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1172
Number of Logic Elements/Cells	18752
Total RAM Bits	239616
Number of I/O	315
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c20f484c8

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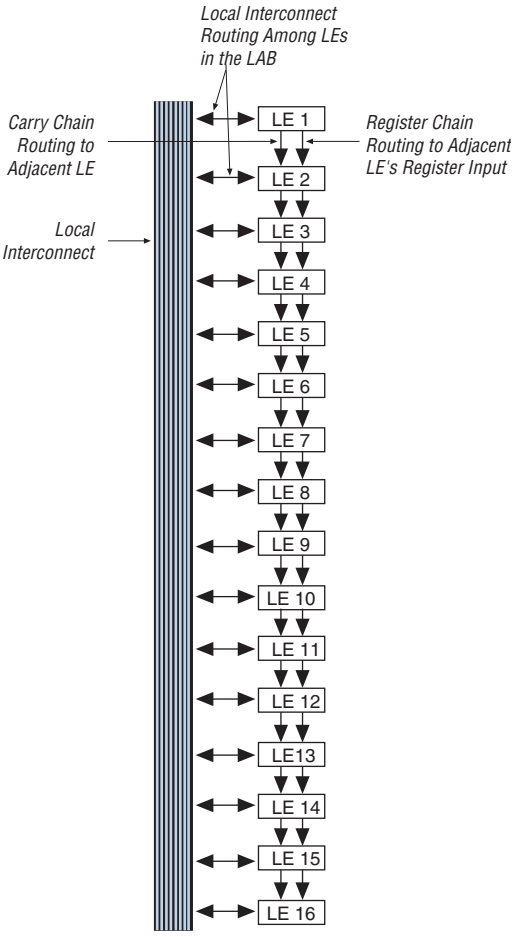
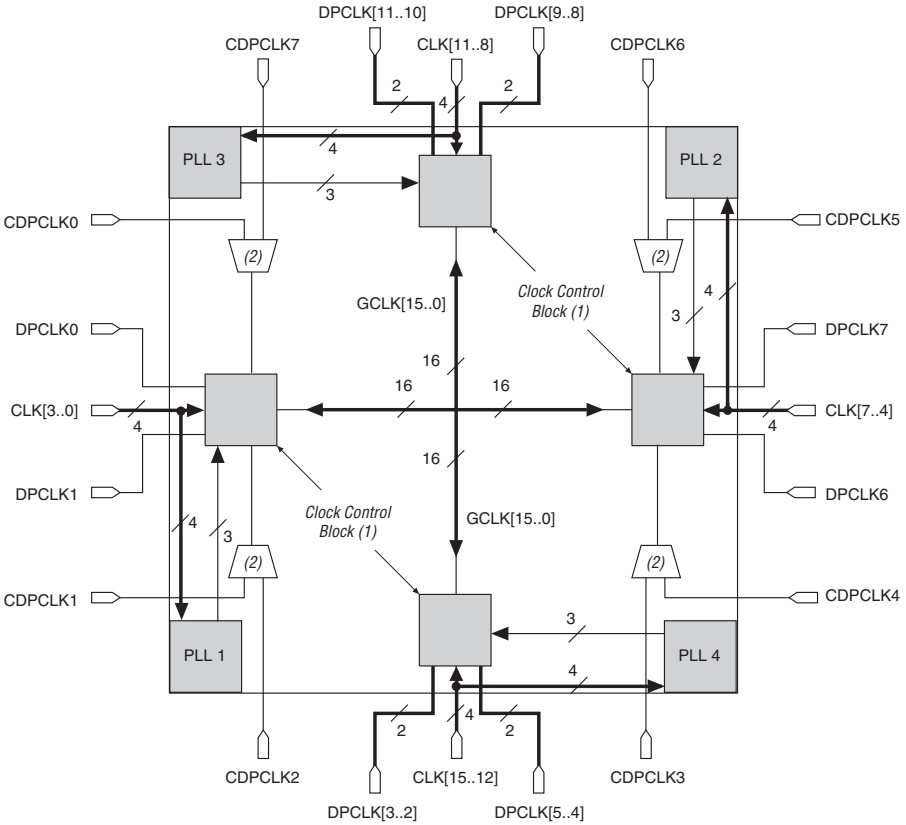
Figure 2–9. Register Chain Interconnects



The C4 interconnects span four LABs, M4K blocks, or embedded multipliers up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–10 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including PLLs, M4K memory blocks, embedded multiplier blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor (see Figure 2–10) can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–12. EP2C15 & Larger PLL, CLK[], DPCLK[] & Clock Control Block Locations



Notes to Figure 2–12:

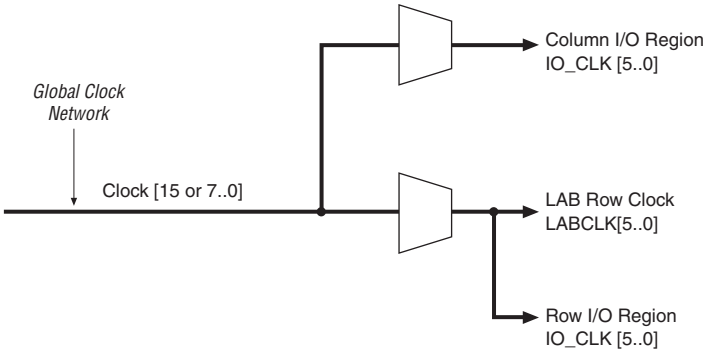
(1) There are four clock control blocks on each side.

(2) Only one of the corner CDPCLK pins in each corner can feed the clock control block at a time. The other CDPCLK pins can be used as general-purpose I/O pins.

Global Clock Network Distribution

Cyclone II devices contains 16 global clock networks. The device uses multiplexers with these clocks to form six-bit buses to drive column IOE clocks, LAB row clocks, or row IOE clocks (see Figure 2–14). Another multiplexer at the LAB level selects two of the six LAB row clocks to feed the LE registers within the LAB.

Figure 2–14. Global Clock Network Multiplexers



LAB row clocks can feed LEs, M4K memory blocks, and embedded multipliers. The LAB row clocks also extend to the row I/O clock regions.

IOE clocks are associated with row or column block regions. Only six global clock resources feed to these row and column regions. Figure 2–15 shows the I/O clock regions.

Cyclone II devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Cyclone II devices support the JTAG instructions shown in Table 3–1.

Table 3–1. Cyclone II JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Cyclone II device via the JTAG port with a USB Blaster™, ByteBlaster™ II, MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or JBC File via an embedded processor.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.

the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

Altera has ensured by design of the I/O buffers and hot-socketing circuitry, that Cyclone II devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone II Devices

The hot-socketing feature turns off the output buffer during power up (either V_{CCINT} or V_{CCIO} supplies) or power down. The hot-socket circuit generates an internal HOTSCKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. Designs cannot use the HOTSCKT signal for other purposes. The HOTSCKT signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When V_{CC} ramps up slowly, V_{CC} is still relatively low even after the internal POR signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tristated at this low V_{CC} voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are able to operate during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 4–1.

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 1 of 2)

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Unit
V_{IN}	Input voltage	*(1)*, *(2)*		–0.5	—	4.0	V
I_i	Input pin leakage current	$V_{IN} = V_{CCIOmax}$ to 0 V *(3)*		–10	—	10	µA
V_{OUT}	Output voltage	—		0	—	V_{CCIO}	V
I_{OZ}	Tri-stated I/O pin leakage current	$V_{OUT} = V_{CCIOmax}$ to 0 V *(3)*		–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_{IN} = ground, no load, no toggling inputs T_J = 25° C Nominal V_{CCINT}	EP2C5/A	—	0.010	*(4)*	A
			EP2C8/A	—	0.017	*(4)*	A
			EP2C15A	—	0.037	*(4)*	A
			EP2C20/A	—	0.037	*(4)*	A
			EP2C35	—	0.066	*(4)*	A
			EP2C50	—	0.101	*(4)*	A
			EP2C70	—	0.141	*(4)*	A
I_{CCIO0}	V_{CCIO} supply current (standby)	V_{IN} = ground, no load, no toggling inputs T_J = 25° C V_{CCIO} = 2.5 V	EP2C5/A	—	0.7	*(4)*	mA
			EP2C8/A	—	0.8	*(4)*	mA
			EP2C15A	—	0.9	*(4)*	mA
			EP2C20/A	—	0.9	*(4)*	mA
			EP2C35	—	1.3	*(4)*	mA
			EP2C50	—	1.3	*(4)*	mA
			EP2C70	—	1.7	*(4)*	mA

Table 5–6. Recommended Operating Conditions for User I/O Pins Using Single-Ended I/O Standards *Note (1)* ***(Part 2 of 2)***

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{IL} (V)	V_{IH} (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
SSTL-18 class II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.125 (DC) V_{REF} – 0.25 (AC)	V_{REF} + 0.125 (DC) V_{REF} + 0.25 (AC)
1.8-V HSTL class I	1.71	1.8	1.89	0.85	0.9	0.95	V_{REF} – 0.1 (DC) V_{REF} – 0.2 (AC)	V_{REF} + 0.1 (DC) V_{REF} + 0.2 (AC)
1.8-V HSTL class II	1.71	1.8	1.89	0.85	0.9	0.95	V_{REF} – 0.1 (DC) V_{REF} – 0.2 (AC)	V_{REF} + 0.1 (DC) V_{REF} + 0.2 (AC)
1.5-V HSTL class I	1.425	1.5	1.575	0.71	0.75	0.79	V_{REF} – 0.1 (DC) V_{REF} – 0.2 (AC)	V_{REF} + 0.1 (DC) V_{REF} + 0.2 (AC)
1.5-V HSTL class II	1.425	1.5	1.575	0.71	0.75	0.79	V_{REF} – 0.1 (DC) V_{REF} – 0.2 (AC)	V_{REF} + 0.1 (DC) V_{REF} + 0.2 (AC)

Note to Table 5–6:
(1) Nominal values (Nom) are for T_A = 25° C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5, 1.8, 2.5, and 3.3 V.

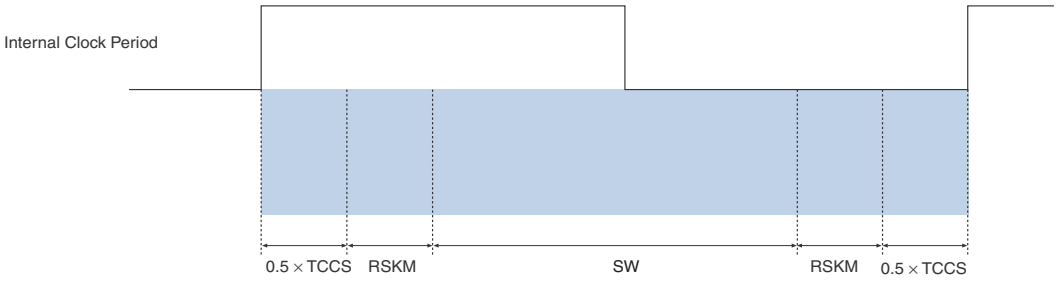
Table 5–7. DC Characteristics of User I/O Pins Using Single-Ended Standards *Notes (1), (2)* ***(Part 1 of 2)***

I/O Standard	Test Conditions		Voltage Thresholds	
	I_{OL} (mA)	I_{OH} (mA)	Maximum V_{OL} (V)	Minimum V_{OH} (V)
3.3-V LVTTL	4	–4	0.45	2.4
3.3-V LVCMOS	0.1	–0.1	0.2	V_{CCIO} – 0.2
2.5-V LVTTL and LVCMOS	1	–1	0.4	2.0
1.8-V LVTTL and LVCMOS	2	–2	0.45	V_{CCIO} – 0.45
1.5-V LVTTL and LVCMOS	2	–2	0.25 × V_{CCIO}	0.75 × V_{CCIO}
PCI and PCI-X	1.5	–0.5	0.1 × V_{CCIO}	0.9 × V_{CCIO}
SSTL-2 class I	8.1	–8.1	V_{TT} – 0.57	V_{TT} + 0.57
SSTL-2 class II	16.4	–16.4	V_{TT} – 0.76	V_{TT} + 0.76
SSTL-18 class I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL-18 class II	13.4	–13.4	0.28	V_{CCIO} – 0.28
1.8-V HSTL class I	8	–8	0.4	V_{CCIO} – 0.4
1.8-V HSTL class II	16	–16	0.4	V_{CCIO} – 0.4

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 3 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
1.8V_HSTL_ CLASS_I	8 mA	t_{OP}	1364	1430	2853	3017	3178	3184	ps
		t_{DIP}	1488	1562	3061	3254	3451	3451	ps
	10 mA	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
	12 mA (1)	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
1.5V_HSTL_ CLASS_I	8 mA (1)	t_{OP}	1657	1738	3642	3917	4185	4191	ps
		t_{DIP}	1781	1870	3850	4154	4458	4458	ps
DIFFERENTIAL_ SSTL_2_ CLASS_I	8 mA	t_{OP}	1090	1142	2152	2268	2376	2382	ps
		t_{DIP}	1214	1274	2360	2505	2649	2649	ps
	12 mA (1)	t_{OP}	1097	1150	2131	2246	2354	2360	ps
		t_{DIP}	1221	1282	2339	2483	2627	2627	ps
DIFFERENTIAL_ SSTL_2_ CLASS_II	16 mA (1)	t_{OP}	1068	1119	2067	2177	2281	2287	ps
		t_{DIP}	1192	1251	2275	2414	2554	2554	ps
DIFFERENTIAL_ SSTL_18_ CLASS_I	6 mA	t_{OP}	1371	1437	2828	3018	3200	3206	ps
		t_{DIP}	1495	1569	3036	3255	3473	3473	ps
	8 mA	t_{OP}	1365	1431	2832	3024	3209	3215	ps
		t_{DIP}	1489	1563	3040	3261	3482	3482	ps
	10 mA (1)	t_{OP}	1374	1440	2806	2990	3167	3173	ps
		t_{DIP}	1498	1572	3014	3227	3440	3440	ps
1.8V_ DIFFERENTIAL_ HSTL_ CLASS_I	8 mA	t_{OP}	1364	1430	2853	3017	3178	3184	ps
		t_{DIP}	1488	1562	3061	3254	3451	3451	ps
	10 mA	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
	12 mA (1)	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
1.5V_ DIFFERENTIAL_ HSTL_ CLASS_I	8 mA (1)	t_{OP}	1657	1738	3642	3917	4185	4191	ps
		t_{DIP}	1781	1870	3850	4154	4458	4458	ps

Figure 5–4. High-Speed I/O Timing Budget *Note (1)*



Note to Figure 5–4:
(1) The equation for the high-speed I/O timing budget is: period = TCCS + RSKM + SW + RSKM.

Table 5–48 shows the RSDS timing budget for Cyclone II devices at 311 Mbps. RSDS is supported for transmitting from Cyclone II devices. Cyclone II devices cannot receive RSDS data because the devices are intended for applications where they will be driving display drivers. Cyclone II devices support a maximum RSDS data rate of 311 Mbps using DDIO registers. Cyclone II devices support RSDS only in the commercial temperature range.

Table 5–48. RSDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max (1)	Min	Typ	Max (1)	Min	Typ	Max (1)	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×8	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×7	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×4	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×2	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×1	10	—	311	10	—	311	10	—	311	MHz
Device operation in Mbps	×10	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	311	20	—	311	20	—	311	Mbps
	×1	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%

7. PLLs in Cyclone II Devices

CII51007-3.1

Introduction

Cyclone® II devices have up to four phase-locked loops (PLLs) that provide robust clock management and synthesis for device clock management, external system clock management, and I/O interfaces. Cyclone II PLLs are versatile and can be used as a zero delay buffer, a jitter attenuator, a low skew fan out buffer, or a frequency synthesizer.

Each Cyclone II device has up to four PLLs, supporting advanced capabilities such as clock switchover and programmable switchover. These PLLs offer clock multiplication and division, phase shifting, and programmable duty cycle and can be used to minimize clock delay and clock skew, and to reduce or adjust clock-to-out (t_{CO}) and set-up (t_{SU}) times.

Cyclone II devices also support a power-down mode where unused clock networks can be turned off. The Altera® Quartus® II software enables the PLLs and their features without requiring any external devices.

Cyclone II PLLs have been characterized to operate in the commercial junction temperature range (0° to 85° C), the industrial junction temperature range (-40° to 100° C) and the extended temperature range (-40° to 125° C).

Table 7–1 shows the PLLs available in each Cyclone II device.

Table 7–1. Cyclone II Device PLL Availability

Device	PLL1	PLL2	PLL3	PLL4
EP2C5	✓	✓		
EP2C8	✓	✓		
EP2C15	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓

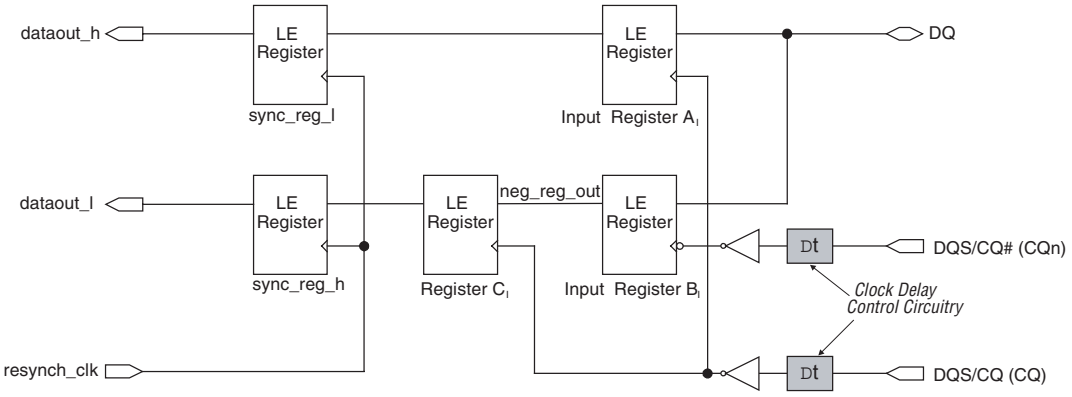
Table 8–1. Summary of M4K Memory Features (Part 2 of 2)	
Feature	**M4K Blocks**
Packed mode	✓
Address clock enable	✓
Single-port mode	✓
Simple dual-port mode	✓
True dual-port mode	✓
Embedded shift register mode *(2)*	✓
ROM mode	✓
FIFO buffer *(2)*	✓
Simple dual-port mixed width support	✓
True dual-port mixed width support	✓
Memory Initialization File (**.mif**)	✓
Mixed-clock mode	✓
Power-up condition	Outputs cleared
Register clears	Output registers only
Same-port read-during-write	New data available at positive clock edge
Mixed-port read-during-write	Old data available at positive clock edge

Notes to Table 8–1:
(1) Maximum performance information is preliminary until device characterization.
(2) FIFO buffers and embedded shift registers require external logic elements (LEs) for implementing control logic.

Table 8–2 shows the capacity and distribution of the M4K memory blocks in each Cyclone II device family member.

Table 8–2. Number of M4K Blocks in Cyclone II Devices (Part 1 of 2)		
Device	**M4K Blocks**	**Total RAM Bits**
EP2C5	26	119,808
EP2C8	36	165,888
EP2C15	52	239,616
EP2C20	52	239,616
EP2C35	105	483,840

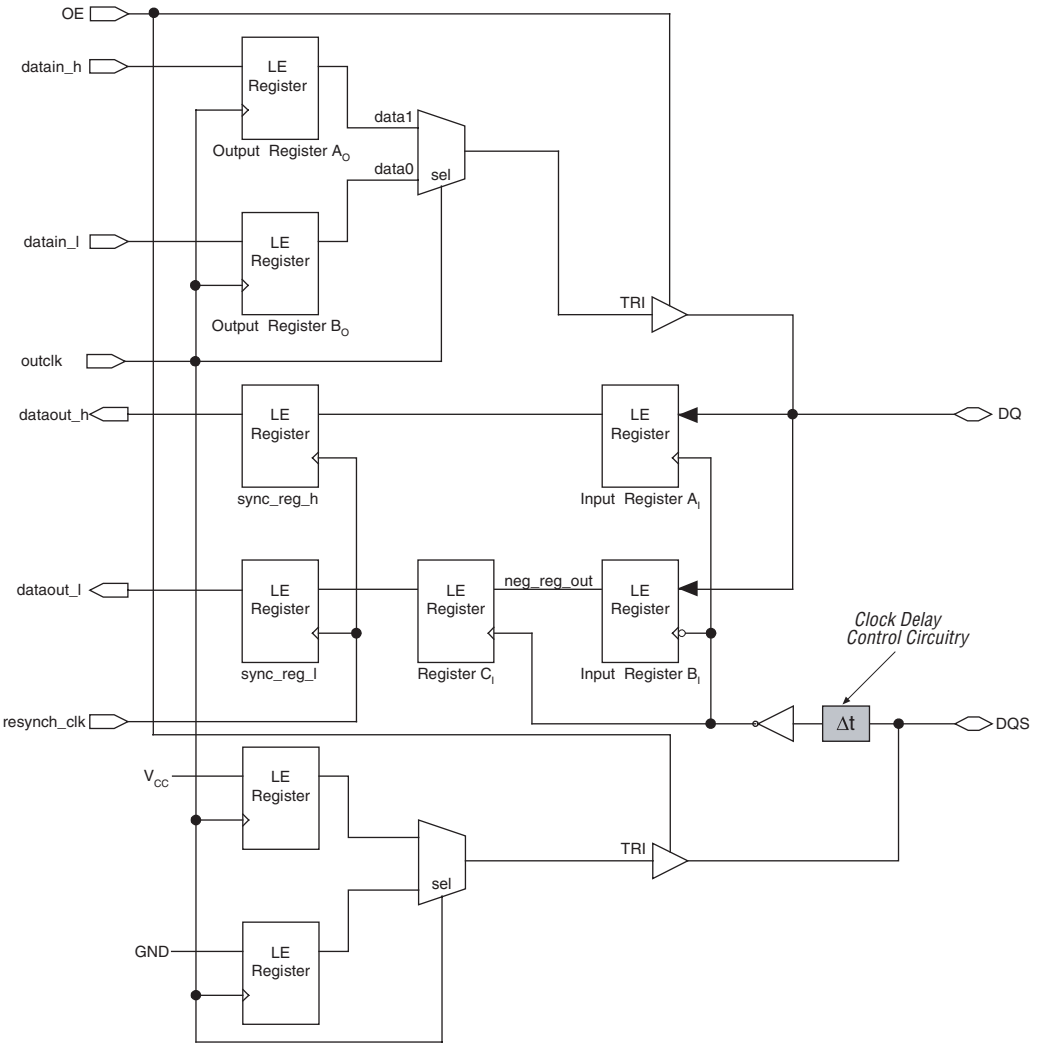
Figure 9–4. CQ & CQn Connection for QDRII SRAM Read



Read & Write Operation

Figure 9–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDRII SRAM devices send data within t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQn clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Cyclone II devices.

Figure 9–16. Bidirectional DDR Implementation for DDR Memory Interfaces *Note (1)*



Note to Figure 9–16:

(1) You can use the `altdq` and `altdqs` megafunctions to generate the DQ and DQS signals.

Figure 9–17 shows example waveforms from a bidirectional DDR implementation.

11. High-Speed Differential Interfaces in Cyclone II Devices

CII51011-2.2

Introduction

From high-speed backplane applications to high-end switch boxes, low-voltage differential signaling (LVDS) is the technology of choice. LVDS is a low-voltage differential signaling standard, allowing higher noise immunity than single-ended I/O technologies. Its low-voltage swing allows for high-speed data transfers, low power consumption, and reduced electromagnetic interference (EMI). LVDS I/O signaling is a data interface standard defined in the TIA/EIA-644 and IEEE Std. 1596.3 specifications.

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced EMI. National Semiconductor Corporation and Texas Instruments introduced the RSDS and mini-LVDS specifications, respectively. Currently, many designers use these specifications for flat panel display links between the controller and the drivers that drive display column drivers. Cyclone® II devices support the RSDS and mini-LVDS I/O standards at speeds up to 311 megabits per second (Mbps) at the transmitter.

Altera® Cyclone II devices can transmit and receive data through LVDS signals at a data rate of up to 640 Mbps and 805 Mbps, respectively. For the LVDS transmitter and receiver, the Cyclone II device's input and output pins support serialization and deserialization through internal logic.

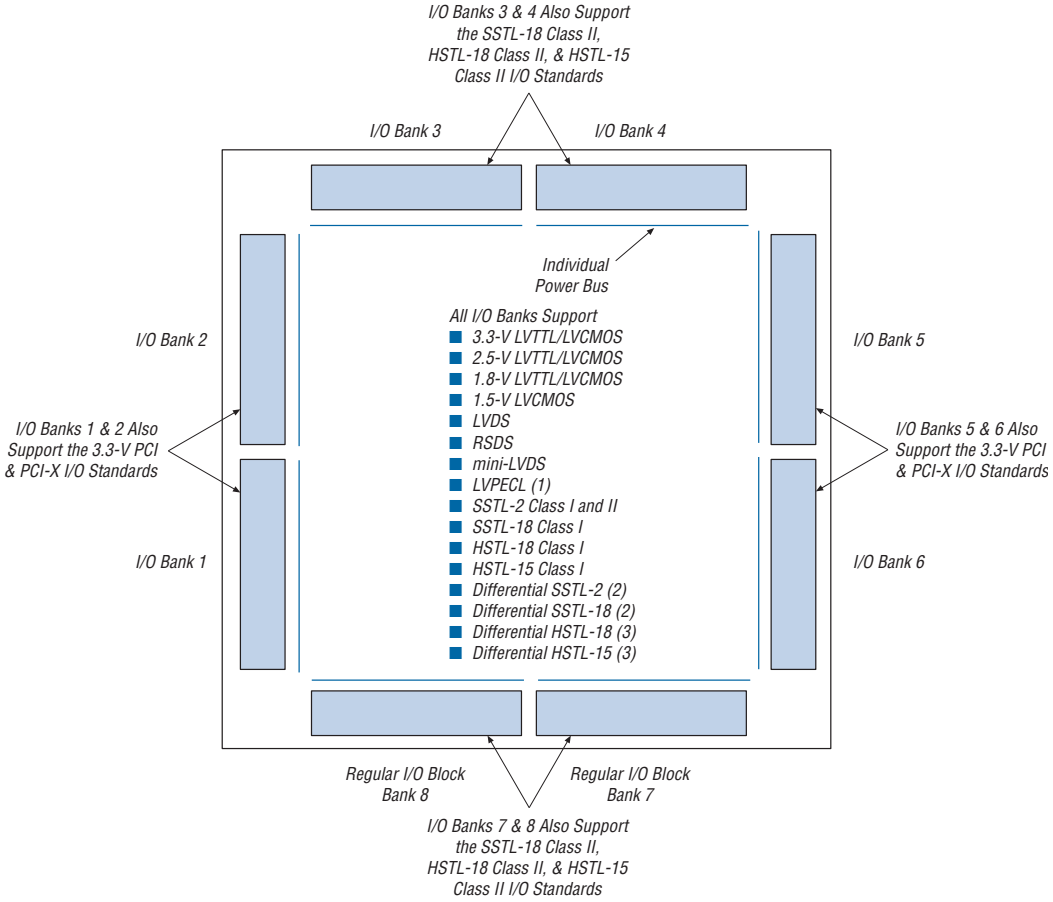
This chapter describes how to use Cyclone II I/O pins for differential signaling and contains the following topics:

- Cyclone II high-speed I/O banks
- Cyclone II high-speed I/O interface
- LVDS, RSDS, mini-LVDS, LVPECL, differential HSTL, and differential SSTL I/O standards support in Cyclone II devices
- High-speed I/O timing in Cyclone II devices
- Design guidelines

Cyclone II High-Speed I/O Banks

Cyclone II device I/O banks are shown in Figures 11–1 and 11–2. The EP2C5 and EP2C8 devices offer four I/O banks and EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices offer eight I/O banks. A subset of

Figure 11–2. I/O Banks in EP2C15, EP2C20, EP2C35, EP2C50 & EP2C70 Devices



Notes to Figure 11–2:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(2) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(3) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

Cyclone II High-Speed I/O Interface

Cyclone II devices provide a multi-protocol interface that allows communication between a variety of I/O standards, including LVDS, LVPECL, RSDS, mini-LVDS, differential HSTL, and differential SSTL. This feature makes the Cyclone II device family ideal for applications that require multiple I/O standards, such as protocol translation.

Configuration Stage

When the nSTATUS pin transitions high, the configuration device's OE pin also transitions high and the configuration device clocks data out serially to the FPGA using its internal oscillator. The Cyclone II device receives configuration data on its DATA0 pin and the clock is received on the DCLK pin. Data is latched into the FPGA on the rising edge of DCLK.

After the FPGA has received all configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by a pull-up resistor. Since the Cyclone II device's CONF_DONE pin is tied to the configuration device's nCS pin, the configuration device is disabled when CONF_DONE goes high. Enhanced configuration and EPC2 devices have an optional internal pull-up resistor on the nCS pin. You can turn this option on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you do not use this internal pull-up resistor, you need to connect an external 10-kΩ pull-up resistor to the nCS and CONF_DONE line. A low-to-high transition on CONF_DONE indicates configuration is complete, and the device can begin initialization.

Initialization Stage

In Cyclone II devices, the default initialization clock source is the Cyclone II internal oscillator (typically 10 MHz). Cyclone II devices can also use the optional CLKUSR pin. If your design uses the internal oscillator, the Cyclone II device supplies itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to use another device or source to send additional clock cycles to the CLKUSR pin during the initialization stage. Additionally, you can use of the CLKUSR pin as a user I/O pin, which means you have an additional user I/O pin.

If you want to delay the initialization of the device, you can use the CLKUSR pin. Using the CLKUSR pin allows you to control when the Cyclone II device enters user mode. You can delay the Cyclone II devices from entering user mode for an indefinite amount of time. You can turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data is accepted and CONF_DONE goes high, Cyclone II devices require 299 clock cycles to properly initialize and support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you use the INIT_DONE pin, an external 10-kΩ pull-up resistor pulls it high when

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCEO	N/A if option is on. I/O if option is off.	All	Output	This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration. If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. Use the Quartus II software to make this pin a user I/O pin.
ASDO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data. In AS mode, ASDO has an internal pull-up that is always active.
nCSO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

Table 13–12 describes the optional configuration pins. If these optional configuration pins are not enabled in the Quartus II software, they are available as general-purpose user I/O pins. Therefore during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 13–12. Optional Configuration Pins

Pin Name	User Mode	Pin Type	Description
CLKUSR	N/A if option is on. I/O if option is off.	Input	This is an optional user-supplied clock input that synchronizes the initialization of one or more devices. This pin is enabled by turning on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	This is a status pin that can be used to indicate when the device has initialized and is in user mode. When nCONFIG is low and during the beginning of configuration, the INIT_DONE pin is tri-stated and pulled high due to an external 10-kΩ pull-up resistor. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high and the FPGA enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the **Enable INIT_DONE output** option in the Quartus II software.
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows the user to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated. When this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the **Enable device-wide output enable (DEV_OE)** option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared. When this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the **Enable device-wide reset (DEV_CLRn)** option in the Quartus II software.