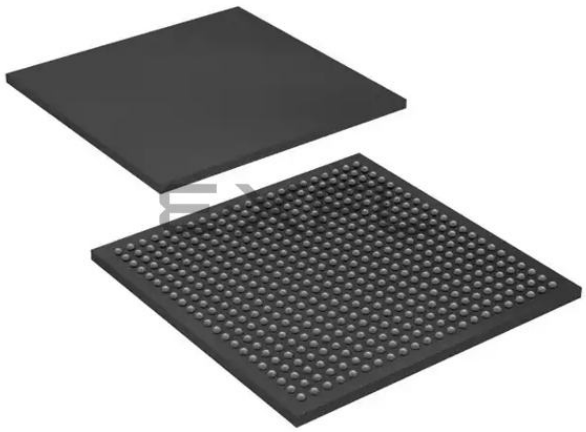

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Details	
Product Status	Active
Number of LABs/CLBs	1172
Number of Logic Elements/Cells	18752
Total RAM Bits	239616
Number of I/O	315
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c20f484c8n

Chapter 14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

Visual Cue	Meaning
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
WARNING	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

protocols. Visit the Altera IPMegaStore at www.altera.com to download IP MegaCore functions.

- Nios II Embedded Processor support

The Cyclone II family offers devices with the Fast-On feature, which offers a faster power-on-reset (POR) time. Devices that support the Fast-On feature are designated with an "A" in the device ordering code. For example, EP2C5A, EP2C8A, EP2C15A, and EP2C20A. The EP2C5A is only available in the automotive speed grade. The EP2C8A and EP2C20A are only available in the industrial speed grade. The EP2C15A is only available with the Fast-On feature and is available in both commercial and industrial grades. The Cyclone II "A" devices are identical in feature set and functionality to the non-A devices except for support of the faster POR time.

Cyclone II A devices are offered in automotive speed grade. For more information, refer to the Cyclone II section in the *Automotive-Grade Device Handbook*.

For more information on POR time specifications for Cyclone II A and non-A devices, refer to the *Hot Socketing & Power-On Reset* chapter in the *Cyclone II Device Handbook*.

Table 1–1 lists the Cyclone II device family features. Table 1–2 lists the Cyclone II device package offerings and maximum user I/O pins.

Table 1–1. Cyclone II FPGA Family Features (Part 1 of 2)

Feature	EP2C5 *(2)*	EP2C8 *(2)*	EP2C15 *(1)*	EP2C20 *(2)*	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	14,448	18,752	33,216	50,528	68,416
M4K RAM blocks (4 Kbits plus 512 parity bits	26	36	52	52	105	129	250
Total RAM bits	119,808	165,888	239,616	239,616	483,840	594,432	1,152,000
Embedded multipliers *(3)*	13	18	26	26	35	86	150
PLLs	2	2	4	4	4	4	4

Referenced Documents

This chapter references the following documents:

- *Hot Socketing & Power-On Reset* chapter in *Cyclone II Device Handbook*
- *Automotive-Grade Device Handbook*

Document Revision History

Table 1–5 shows the revision history for this document.

Table 1–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v3.2	• Added "Referenced Documents". • Updated "Features" section and Table 1–1, Table 1–2, and Table 1–4 with information about EP2C5A.	—
February 2007 v3.1	• Added document revision history. • Added new *Note (2)* to Table 1–2.	Note to explain difference between I/O pin count information provided in Table 1–2 and in the Quartus II software documentation.
November 2005 v2.1	• Updated Introduction and Features. • Updated Table 1–3.	—
July 2005 v2.0	• Updated technical content throughout. • Updated Table 1–2. • Added Tables 1–3 and 1–4.	—
November 2004 v1.1	• Updated Table 1–2. • Updated bullet list in the "Features" section.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Memory Modes

Table 2–7 summarizes the different memory modes supported by the M4K memory blocks.

Table 2–7. M4K Memory Modes

Memory Mode	Description
Single-port memory	M4K blocks support single-port mode, used when simultaneous reads and writes are not required. Single-port memory supports non-simultaneous reads and writes.
Simple dual-port memory	Simple dual-port memory supports a simultaneous read and write.
Simple dual-port with mixed width	Simple dual-port memory mode with different read and write port widths.
True dual-port memory	True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies.
True dual-port with mixed width	True dual-port mode with different read and write port widths.
Embedded shift register	M4K memory blocks are used to implement shift registers. Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock.
ROM	The M4K memory blocks support ROM mode. A MIF initializes the ROM contents of these blocks.
FIFO buffers	A single clock or dual clock FIFO may be implemented in the M4K blocks. Simultaneous read and write from an empty FIFO buffer is not supported.

Embedded Memory can be inferred in your HDL code or directly instantiated in the Quartus II software using the MegaWizard® Plug-in Manager Memory Compiler feature.

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes

Clock Mode	Description
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`.
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

Table 2–9. Cyclone II M4K Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

standards (e.g., SSTL-2) independently. If an I/O bank does not use voltage-referenced standards, the VREF pins are available as user I/O pins.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs. Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value.

MultiVolt I/O Interface

The Cyclone II architecture supports the MultiVolt I/O interface feature, which allows Cyclone II devices in all packages to interface with systems of different supply voltages. Cyclone II devices have one set of V_{CC} pins (VCCINT) that power the internal device logic array and input buffers that use the LVPECL, LVDS, HSTL, or SSTL I/O standards. Cyclone II devices also have four or eight sets of VCC pins (VCCIO) that power the I/O output drivers and input buffers that use the LVTTL, LVCMOS, or PCI I/O standards.

The Cyclone II VCCINT pins must always be connected to a 1.2-V power supply. If the V_{CCINT} level is 1.2 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V systems. Table 2–20 summarizes Cyclone II MultiVolt I/O support.

Table 2–20. Cyclone II MultiVolt I/O Support (Part 1 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
1.5	✓	✓	✓ *(2)*	✓ *(2)*	✓			
1.8	✓ *(4)*	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓		
2.5			✓	✓	✓ *(5)*	✓ *(5)*	✓	

Table 5–2 specifies the recommended operating conditions for Cyclone II devices. It shows the allowed voltage ranges for V_{CCINT}, V_{CCIO}, and the operating junction temperature (T_J). The LVTTL and LVCMOS inputs are powered by V_{CCIO} only. The LVDS and LVPECL input buffers on dedicated clock pins are powered by V_{CCINT}. The SSTL, HSTL, LVDS input buffers are powered by both V_{CCINT} and V_{CCIO}.

Table 5–2. Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(1)*	1.15	1.25	V
V_{CCIO} *(2)*	Supply voltage for output buffers, 3.3-V operation	*(1)*	3.135 (3.00)	3.465 (3.60) *(3)*	V
	Supply voltage for output buffers, 2.5-V operation	*(1)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(1)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(1)*	1.425	1.575	V
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C
		For extended temperature use	–40	125	°C
		For automotive use	–40	125	°C

Notes to Table 5–2:

(1) The V_{CC} must rise monotonically. The maximum V_{CC} (both V_{CCIO} and V_{CCINT}) rise time is 100 ms for non-A devices and 2 ms for A devices.

(2) The V_{CCIO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCIO} range specific to each of the single-ended I/O standards is given in Table 5–6, and those specific to the differential standards is given in Table 5–8.

(3) The minimum and maximum values of 3.0 V and 3.6 V, respectively, for V_{CCIO} only applies to the PCI and PCI-X I/O standards. Refer to Table 5–6 for the voltage range of other I/O standards.

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 4 of 4)

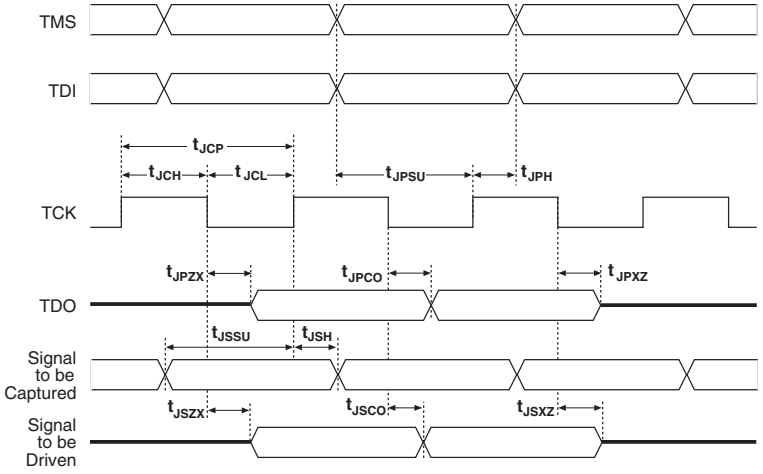
I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.5V_ DIFFERENTIAL_HSTL _CLASS_I	8 mA	210	170	140	210	170	140	210	170	140
	10 mA	220	180	150	—	—	—	—	—	—
	12 mA	230	190	160	—	—	—	—	—	—
1.5V_ DIFFERENTIAL_HSTL _CLASS_II	16 mA	210	170	140	—	—	—	—	—	—
LVDS	—	400	340	280	400	340	280	400	340	280
RSDS	—	400	340	280	400	340	280	400	340	280
MINI_LVDS	—	400	340	280	400	340	280	400	340	280
SIMPLE_RSDS	—	380	320	260	380	320	260	380	320	260
1.2V_HSTL	—	80	80	80	—	—	—	—	—	—
1.2V_ DIFFERENTIAL_HSTL	—	80	80	80	—	—	—	—	—	—
PCI	—	—	—	—	350	315	280	350	315	280
PCI-X	—	—	—	—	350	315	280	350	315	280
LVTTL	OCT_25_ OHMS	360	300	250	360	300	250	360	300	250
LVCMOS	OCT_25_ OHMS	360	300	250	360	300	250	360	300	250
2.5V	OCT_50_ OHMS	240	200	160	240	200	160	240	200	160
1.8V	OCT_50_ OHMS	290	240	200	290	240	200	290	240	200
SSTL_2_CLASS_I	OCT_50_ OHMS	240	200	160	240	200	160	—	—	—
SSTL_18_CLASS_I	OCT_50_ OHMS	290	240	200	290	240	200	—	—	—

Note to Table 5–45:
(1) This is based on single data rate I/Os.

JTAG Timing Specifications

Figure 5–7 shows the timing requirements for the JTAG signals.

Figure 5–7. Cyclone II JTAG Waveform



PLL Timing Specifications

Table 5–54 describes the Cyclone II PLL specifications when operating in the commercial junction temperature range (0° to 85° C), the industrial junction temperature range (–40° to 100° C), the automotive junction temperature range (–40° to 125° C), and the extended temperature range (–40° to 125° C). Follow the PLL specifications for –8 speed grade devices when operating in the industrial, automotive, or extended temperature range.

Table 5–54. PLL Specifications *Note (1)* ***(Part 1 of 2)***

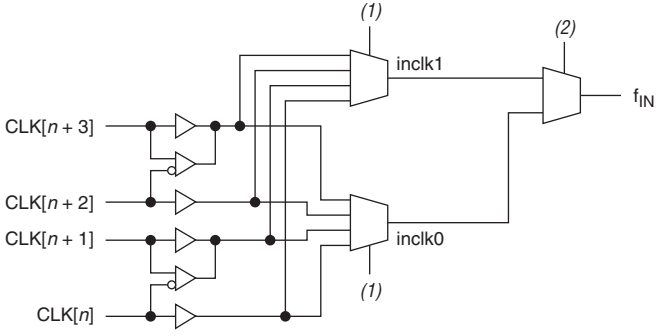
Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–6 speed grade)	10	—	*(4)*	MHz
	Input clock frequency (–7 speed grade)	10	—	*(4)*	MHz
	Input clock frequency (–8 speed grade)	10	—	*(4)*	MHz
f_{INPFD}	PFD input frequency (–6 speed grade)	10	—	402.5	MHz
	PFD input frequency (–7 speed grade)	10	—	402.5	MHz
	PFD input frequency (–8 speed grade)	10	—	402.5	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$ *(5)*	Input clock period jitter	—	200	—	ps
f_{OUT_EXT} (external clock output)	PLL output frequency (–6 speed grade)	10	—	*(4)*	MHz
	PLL output frequency (–7 speed grade)	10	—	*(4)*	MHz
	PLL output frequency (–8 speed grade)	10	—	*(4)*	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	10	—	500	MHz
	PLL output frequency (–7 speed grade)	10	—	450	MHz
	PLL output frequency (–8 speed grade)	10	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	—	55	%
t_{JITTER} (p-p) *(2)*	Period jitter for external clock output f_{OUT_EXT} > 100 MHz	—	—	300	ps
	f_{OUT_EXT} ≤100 MHz	—	—	30	mUI
t_{LOCK}	Time required to lock from end of device configuration	—	—	100 *(6)*	µs
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±60	ps

Manual Clock Switchover

The Cyclone II PLLs support manual switchover of the reference clock through internal logic. This enables you to switch between two reference input clocks. Use this feature for a dual clock domain application such as in a system that turns on the redundant clock if the primary clock stops running.

Figure 7–10 shows how the PLL input clock (f_{IN}) is generated from one of four possible clock sources. The first stage multiplexing consists of two dedicated multiplexers that generate two single-ended or two differential clocks from four dedicated clock pins. These clock signals are then multiplexed to generate f_{IN} by using another dedicated 2-to-1 multiplexer. The first stage multiplexers are controlled by configuration bit settings in the configuration file generated by the Quartus II software, while the second stage multiplexer is either controlled by the configuration bit settings or logic array signal to allow the f_{IN} to be controlled dynamically. This allows the implementation of a manual clock switchover circuit where the PLL reference clock can be switched during user mode for applications that requires clock redundancy.

Figure 7–10. Cyclone II PLL Input Clock Generation



Notes to Figure 7–10:

(1) This select line is set through the configuration file.

(2) This select line can either be set through the configuration file or it can be dynamically set in user mode when using the manual switchover feature.

Section III. Memory

This section provides information on embedded memory blocks in Cyclone® II devices and the supported external memory interfaces.

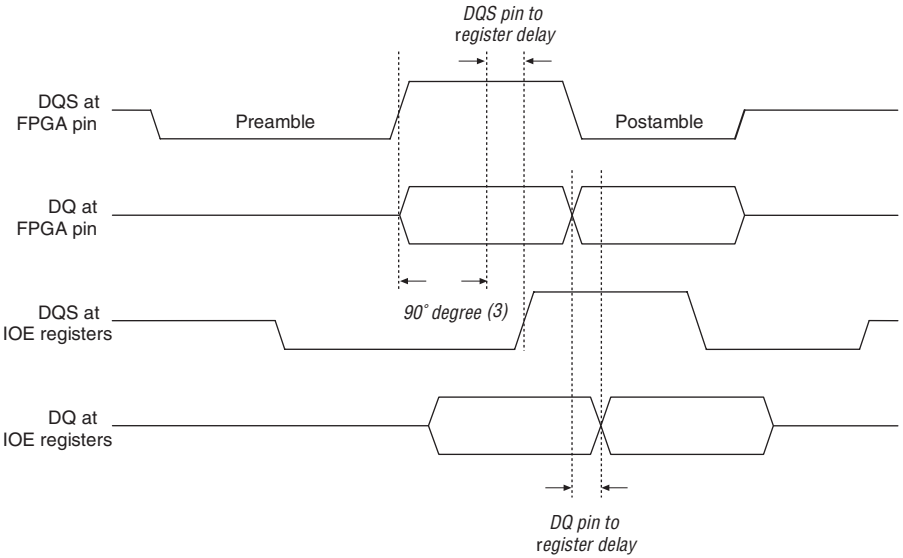
This section includes the following chapters:

- Chapter 8, Cyclone II Memory Blocks
- Chapter 9, External Memory Interfaces

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 9–1. Example of a 90° Shift on the DQS Signal *Notes (1), (2)*



Notes to Figure 9–1:
(1) RLDRAM II and QDRII SRAM memory interfaces do not have preamble and postamble specifications.
(2) DDR2 SDRAM does not support a burst length of two.
(3) The phase shift required for your system should be based on your timing analysis and may not be 90°.

During write operations to a DDR or DDR2 SDRAM device, the FPGA must send the data strobe to the memory device center-aligned relative to the data. Cyclone II devices use a PLL to center-align the data strobe by generating a 0° phase-shifted system clock for the write data strobes and a –90° phase-shifted write clock for the write data pins for the DDR and DDR2 SDRAM. Figure 9–2 shows an example of the relationship between the data and data strobe during a burst-of-two write.

Figure 9–2. DQ & DQS Relationship During a DDR & DDR2 SDRAM Write

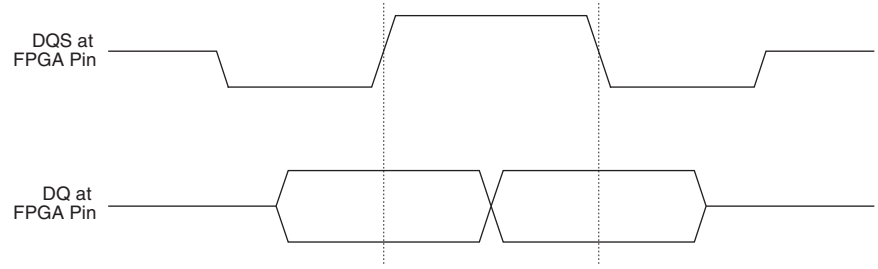
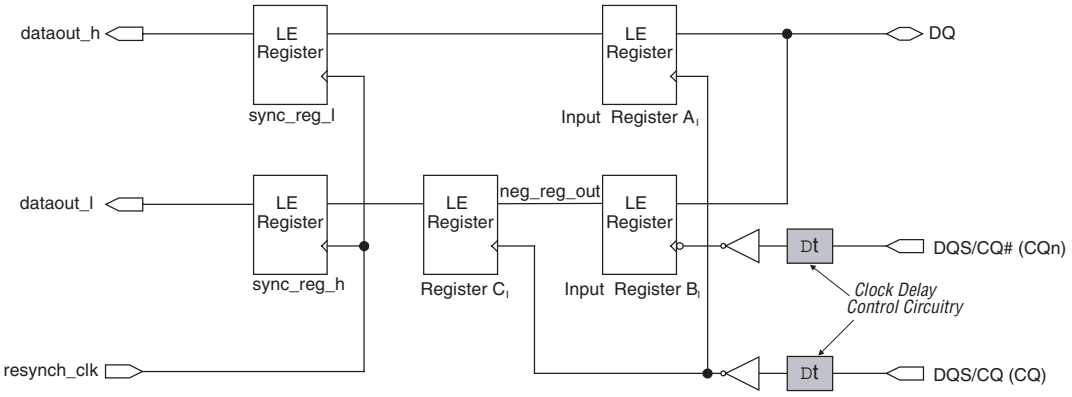


Figure 9–4. CQ & CQn Connection for QDRII SRAM Read



Read & Write Operation

Figure 9–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDRII SRAM devices send data within t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQn clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Cyclone II devices.

Table 11–1. LVDS I/O Specifications (Part 2 of 2) *Note (1)*

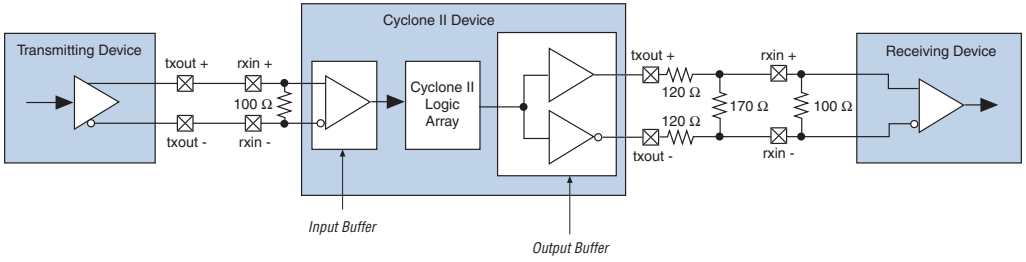
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ID}	Input differential voltage (single-ended)		0.1		0.65	V
V_{ICM}	Input common mode voltage		0.1		2.0	V
ΔV_{OS}	Change in V_{OS} between H and L	R_L = 100 Ω			50	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Note to Table 11–1:
(1) The specifications apply at the resistor network output.

LVDS Receiver & Transmitter

Figure 11–3 shows a simple point-to-point LVDS application where the source of the data is an LVDS transmitter. These LVDS signals are typically transmitted over a pair of printed circuit board (PCB) traces, but a combination of a PCB trace, connectors, and cables is a common application setup.

Figure 11–3. Typical LVDS Application



Figures 11–4 and 11–5 show the signaling levels for LVDS receiver inputs and transmitter outputs, respectively.

Combining JTAG & Active Serial Configuration Schemes

You can combine the AS configuration scheme with JTAG-based configuration. Set the MSEL[1..0] pins to 00 (AS mode) or 10 (Fast AS mode)in this setup, which uses two 10-pin download cable headers on the board. The first header programs the serial configuration device in the system via the AS programming interface, and the second header configures the Cyclone II directly via the JTAG interface.

If you try configuring the device using both schemes simultaneously, JTAG configuration takes precedence and AS configuration is terminated.

When a blank serial configuration device is attached to Cyclone II device, turn on the **Halt on-chip configuration controller** option under the Tools menu by clicking **Options**. The Options dialog box appears. In the **Category** list, select **Programmer** before starting the JTAG configuration with the Quartus II programmer. This option stops the AS reconfiguration loop from a blank serial configuration device before starting the JTAG configuration. This includes using the Serial Flash Loader IP because JTAG is used for configuring the Cyclone II device. Users do not need to recompile their Quartus II designs after turning on this Option.

Programming Serial Configuration Devices In-System Using the JTAG Interface

Cyclone II devices in a single device chain or in a multiple device chain support in-system programming of a serial configuration device using the JTAG interface via the serial flash loader design. The board's intelligent host or download cable can use the four JTAG pins on the Cyclone II device to program the serial configuration device in system, even if the host or download cable cannot access the configuration device's configuration pins (DCLK, DATA, ASDI, and nCS pins).

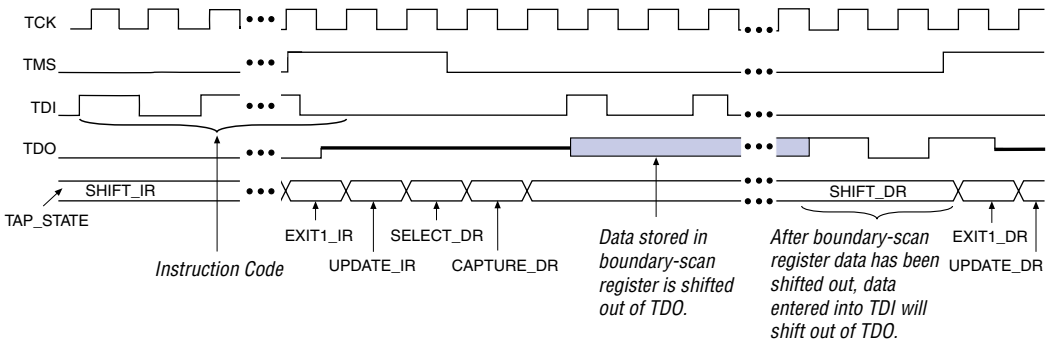
The serial flash loader design is a JTAG-based in-system programming solution for Altera serial configuration devices. The serial flash loader is a bridge design for the FPGA that uses its JTAG interface to access the EPCS JIC (JTAG Indirect Configuration Device Programming) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the serial flash loader design.

In a multiple device chain, you only need to configure the master Cyclone II device which is controlling the serial configuration device. The slave devices in the multiple device chain which are configured by the serial configuration device do not need to be configured when using this

During the capture phase, multiplexers preceding the capture registers select the active device data signals. This data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery, then out of the TDO pin. The device can simultaneously shift new test data into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. This data can then be used in the EXTEST instruction mode. See "EXTEST Instruction Mode" on page 14–11 for more information.

Figure 14–9 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state, then to the SHIFT_DR state, where it remains if TMS is held low. The data that was present in the capture registers after the capture phase is shifted out of the TDO pin. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. Figure 14–9 shows that the instruction code at TDI does not appear at the TDO pin until after the capture register data is shifted out. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

Figure 14–9. SAMPLE/PRELOAD Shift Data Register Waveforms



EXTEST Instruction Mode

The EXTEST instruction mode is used to check external pin connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, opens and shorts can be detected at pins of any device in the scan chain.

484-Pin Ultra FineLine BGA – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 15–15 and 15–16 show the package information and package outline figure references, respectively, for the 484-pin Ultra FineLine BGA package.

Table 15–15. 484-Pin Ultra FineLine BGA Package Information

Description	Specification
Ordering Code Reference	U
Package Acronym	UBGA
Substrate Material	BT
Solder Ball Composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MO-216 Variation: BAP-2
Maximum Lead Coplanarity	0.005 inches (0.12mm)
Weight	1.8 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Table 15–16. 484-Pin Ultra FineLine BGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	2.20
A1	0.20	–	–
A2	0.65	–	–
A3	0.80 TYP		
D	19.00 BSC		
E	19.00 BSC		
b	0.40	0.50	0.60
e	0.80 BSC		