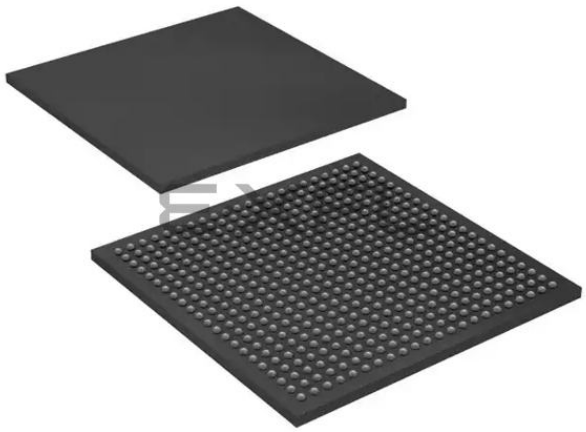


Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1172 |
| Number of Logic Elements/Cells | 18752 |
| Total RAM Bits | 239616 |
| Number of I/O | 315 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2c20f484i8 |

# Section I. Cyclone II Device Family Data Sheet

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. It contains the required PCB layout guidelines, device pin tables, and package specifications.

This section includes the following chapters:



## Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

*Table 1–3. Total Number of Non-Migratable I/O Pins for Cyclone II Vertical Migration Paths*

| Vertical Migration Path | 144-Pin TQFP | 208-Pin PQFP | 256-Pin FineLine BGA (1) | 484-Pin FineLine BGA (2) | 484-Pin Ultra FineLine BGA | 672-Pin FineLine BGA (3) |
|---|---|---|---|---|---|---|
| EP2C5 to EP2C8 | 4 | 4 | 1 (4) | — | — | — |
| EP2C8 to EP2C15 | — | — | 30 | — | — | — |
| EP2C15 to EP2C20 | — | — | 0 | 0 | — | — |
| EP2C20 to EP2C35 | | — | — | 16 | — | — |
| EP2C35 to EP2C50 | — | — | — | 28 | 28 (5) | 28 |
| EP2C50 to EP2C70 | — | — | — | — | 28 | 28 |

***Notes to Table 1–3:***

(1) Vertical migration between the EP2C5F256 to the EP2C15AF256 and the EP2C5F256 to the EP2C20F256 devices is not supported.
(2) When migrating from the EP2C20F484 device to the EP2C50F484 device, a total of 39 I/O pins are non-migratable.
(3) When migrating from the EP2C35F672 device to the EP2C70F672 device, a total of 56 I/O pins are non-migratable.
(4) In addition to the one non-migratable I/O pin, there are 34 DQ pins that are non-migratable.
(5) The pinouts of 484 FBGA and 484 UBGA are the same.

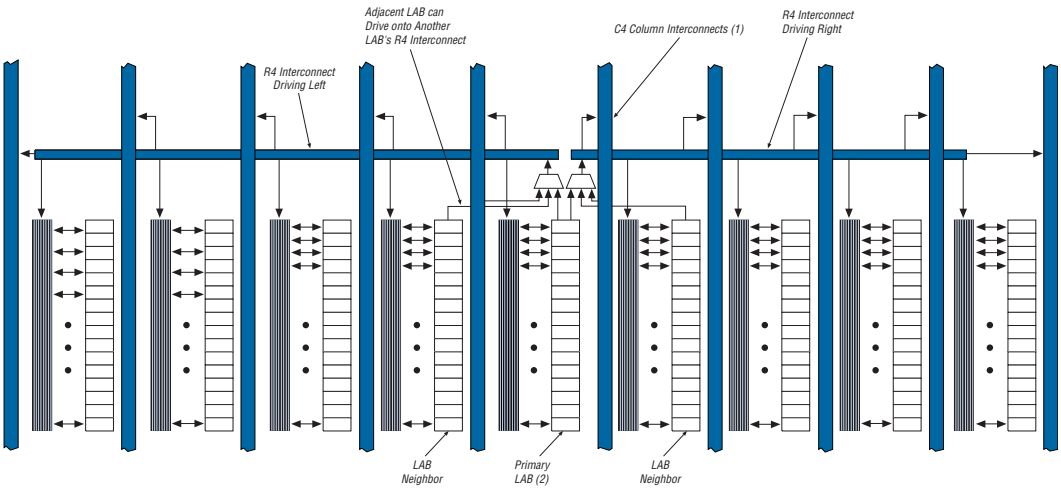
When moving from one density to a larger density, I/O pins are often lost because of the greater number of power and ground pins required to support the additional logic within the larger device. For I/O pin migration across densities, you must cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

To ensure that your board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (go to Assignments menu, then Device, then click the **Migration Devices** button). After compilation, check the information messages for a full list of I/O, DQ, LVDS, and other pins that are not available because of the selected migration path. Table 1–3 lists the Cyclone II device package offerings and shows the total number of non-migratable I/O pins when migrating from one density device to a larger density device.

The direct link interconnect allows an LAB, M4K memory block, or embedded multiplier block to drive into the local interconnect of its left and right neighbors. Only one side of a PLL block interfaces with direct link and row interconnects. The direct link interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M4K memory block, or three LABs and one embedded multiplier to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–8 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by LABs, M4K memory blocks, embedded multipliers, PLLs, and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor (see Figure 2–8) can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. Additionally, R4 interconnects can drive R24 interconnects, C4, and C16 interconnects for connections from one row to another.

***Figure 2–8. R4 Interconnect Connections***




*Notes to Figure 2–8:*

(1) C4 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

In Cyclone II devices, all the I/O banks support SDR and DDR SDRAM memory up to 167 MHz/333 Mbps. All I/O banks support DQS signals with the DQ bus modes of ×8/×9, or ×16/×18. Table 2–14 shows the external memory interfaces supported in Cyclone II devices.

*Table 2–14. External Memory Support in Cyclone II Devices* *Note (1)*

| Memory Standard | I/O Standard | Maximum Bus Width | Maximum Clock Rate Supported (MHz) | Maximum Data Rate Supported (Mbps) |
|---|---|---|---|---|
| SDR SDRAM | LVTTL *(2)* | 72 | 167 | 167 |
| DDR SDRAM | SSTL-2 class I *(2)* | 72 | 167 | 333 *(1)* |
| | SSTL-2 class II *(2)* | 72 | 133 | 267 *(1)* |
| DDR2 SDRAM | SSTL-18 class I *(2)* | 72 | 167 | 333 *(1)* |
| | SSTL-18 class II *(3)* | 72 | 125 | 250 *(1)* |
| QDRII SRAM *(4)* | 1.8-V HSTL class I *(2)* | 36 | 167 | 668 *(1)* |
| | 1.8-V HSTL class II *(3)* | 36 | 100 | 400 *(1)* |

***Notes to Table 2–14:***

(1) The data rate is for designs using the Clock Delay Control circuitry.
(2) The I/O standards are supported on all the I/O banks of the Cyclone II device.
(3) The I/O standards are supported only on the I/O banks on the top and bottom of the Cyclone II device.
(4) For maximum performance, Altera recommends using the 1.8-V HSTL I/O standard because of higher I/O drive strength. QDRII SRAM devices also support the 1.5-V HSTL I/O standard.

Cyclone II devices use data (DQ), data strobe (DQS), and clock pins to interface with external memory. Figure 2–26 shows the DQ and DQS pins in the ×8/×9 mode.

*Table 5–16. LE_FF Internal Timing Microparameters (Part 2 of 2)*

| Parameter | –6 Speed Grade (1) | | –7 Speed Grade (2) | | –8 Speed Grade (3) | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| TPRE | 191 | — | 244 | — | 244 | — | ps |
| | — | — | 217 | — | 244 | — | ps |
| TCLKL | 1000 | — | 1242 | — | 1242 | — | ps |
| | — | — | 1111 | — | 1242 | — | ps |
| TCLKH | 1000 | — | 1242 | — | 1242 | — | ps |
| | — | — | 1111 | — | 1242 | — | ps |
| tLUT | 180 | 438 | 172 | 545 | 172 | 651 | ps |
| | — | — | 180 | — | 180 | — | ps |

*Notes to Table 5–16:*

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

*Table 5–17. IOE Internal Timing Microparameters (Part 1 of 2)*

| Parameter | –6 Speed Grade (1) | | –7 Speed Grade (2) | | –8 Speed Grade (3) | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| TSU | 76 | — | 101 | — | 101 | — | ps |
| | — | — | 89 | — | 101 | — | ps |
| TH | 88 | — | 106 | — | 106 | — | ps |
| | — | — | 97 | — | 106 | — | ps |
| TCO | 99 | 155 | 95 | 171 | 95 | 187 | ps |
| | — | — | 99 | — | 99 | — | ps |
| TPIN2COMBOUT_R | 384 | 762 | 366 | 784 | 366 | 855 | ps |
| | — | — | 384 | — | 384 | — | ps |
| TPIN2COMBOUT_C | 385 | 760 | 367 | 783 | 367 | 854 | ps |
| | — | — | 385 | — | 385 | — | ps |
| TCOMBIN2PIN_R | 1344 | 2490 | 1280 | 2689 | 1280 | 2887 | ps |
| | — | — | 1344 | — | 1344 | — | ps |

*Table 5–37. Cyclone II IOE Programmable Delay on Row Pins Notes (1), (2) (Part 2 of 2)*

| Parameter | Paths Affected | Number of Settings | Fast Corner (3) | | –6 Speed Grade | | –7 Speed Grade (4) | | –8 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min Offset | Max Offset | Min Offset | Max Offset | Min Offset | Max Offset | Min Offset | Max Offset | |
| Input Delay from Pin to Input Register | Pad -> I/O input register | 8 | 0 | 2669 | 0 | 4482 | 0 | 4834 | 0 | 4859 | ps |
| | | | 0 | 2802 | — | — | 0 | 4671 | — | — | ps |
| Delay from Output Register to Output Pin | I/O output register -> Pad | 2 | 0 | 308 | 0 | 572 | 0 | 648 | 0 | 682 | ps |
| | | | 0 | 324 | — | — | 0 | 626 | — | — | ps |

*Notes to Table 5–37 :*

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.

(3) The value in the first row represents the fast corner timing parameter for industrial and automotive devices. The second row represents the fast corner timing parameter for commercial devices.

(4) The value in the first row is for automotive devices. The second row is for commercial devices.

## Default Capacitive Loading of Different I/O Standards

Refer to Table 5–38 for default capacitive loading of different I/O standards.

*Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 1 of 2)*

| I/O Standard | Capacitive Load | Unit |
|---|---|---|
| LVTTL | 0 | pF |
| LVCMOS | 0 | pF |
| 2.5V | 0 | pF |
| 1.8V | 0 | pF |
| 1.5V | 0 | pF |
| PCI | 10 | pF |
| PCI-X | 10 | pF |
| SSTL_2_CLASS_I | 0 | pF |
| SSTL_2_CLASS_II | 0 | pF |
| SSTL_18_CLASS_I | 0 | pF |

*Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 2 of 2)*

| I/O Standard | Capacitive Load | Unit |
|---|---|---|
| SSTL_18_CLASS_II | 0 | pF |
| 1.5V_HSTL_CLASS_I | 0 | pF |
| 1.5V_HSTL_CLASS_II | 0 | pF |
| 1.8V_HSTL_CLASS_I | 0 | pF |
| 1.8V_HSTL_CLASS_II | 0 | pF |
| DIFFERENTIAL_SSTL_2_CLASS_I | 0 | pF |
| DIFFERENTIAL_SSTL_2_CLASS_II | 0 | pF |
| DIFFERENTIAL_SSTL_18_CLASS_I | 0 | pF |
| DIFFERENTIAL_SSTL_18_CLASS_II | 0 | pF |
| 1.5V_DIFFERENTIAL_HSTL_CLASS_I | 0 | pF |
| 1.5V_DIFFERENTIAL_HSTL_CLASS_II | 0 | pF |
| 1.8V_DIFFERENTIAL_HSTL_CLASS_I | 0 | pF |
| 1.8V_DIFFERENTIAL_HSTL_CLASS_II | 0 | pF |
| LVDS | 0 | pF |
| 1.2V_HSTL | 0 | pF |
| 1.2V_DIFFERENTIAL_HSTL | 0 | pF |

*Table 5–48. RSDS Transmitter Timing Specification (Part 2 of 2)*

| Symbol | Conditions | –6 Speed Grade | | | –7 Speed Grade | | | –8 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max *(1)* | Min | Typ | Max *(1)* | Min | Typ | Max *(1)* | |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| $t_{RISE}$ | 20–80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | 80–20%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | — | — | | 100 | — | | 100 | — | — | 100 | µs |

*Note to Table 5–48:*

(1) These specifications are for a three-resistor RSDS implementation. For single-resistor RSDS in ×10 through ×2 modes, the maximum data rate is 170 Mbps and the corresponding maximum input clock frequency is 85 MHz. For single-resistor RSDS in ×1 mode, the maximum data rate is 170 Mbps, and the maximum input clock frequency is 170 MHz. For more information about the different RSDS implementations, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the Cyclone II Device Handbook.

In order to determine the transmitter timing requirements, RSDS receiver timing requirements on the other end of the link must be taken into consideration. RSDS receiver timing parameters are typically defined as $t_{SU}$ and $t_H$ requirements. Therefore, the transmitter timing parameter specifications are $t_{CO}$ (minimum) and $t_{CO}$ (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for RSDS are shown in Figure 5–5.

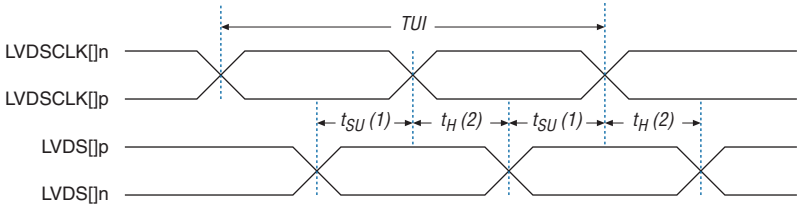
*Table 5–49. Mini-LVDS Transmitter Timing Specification (Part 2 of 2)*

| Symbol | Conditions | –6 Speed Grade | | | –7 Speed Grade | | | –8 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Device operation in Mbps | ×10 | 100 | — | 311 | 100 | — | 311 | 100 | — | 311 | Mbps |
| | ×8 | 80 | — | 311 | 80 | — | 311 | 80 | — | 311 | Mbps |
| | ×7 | 70 | — | 311 | 70 | — | 311 | 70 | — | 311 | Mbps |
| | ×4 | 40 | — | 311 | 40 | — | 311 | 40 | — | 311 | Mbps |
| | ×2 | 20 | — | 311 | 20 | — | 311 | 20 | — | 311 | Mbps |
| | ×1 | 10 | — | 311 | 10 | — | 311 | 10 | — | 311 | Mbps |
| $t_{DUTY}$ | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS | — | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| Output jitter (peak to peak) | — | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| $t_{RISE}$ | 20–80% | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| $t_{FALL}$ | 80–20% | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| $t_{LOCK}$ | | — | — | 100 | — | — | 100 | — | — | 100 | µs |

In order to determine the transmitter timing requirements, mini-LVDS receiver timing requirements on the other end of the link must be taken into consideration. The mini-LVDS receiver timing parameters are typically defined as $t_{SU}$ and $t_H$ requirements. Therefore, the transmitter timing parameter specifications are $t_{CO}$ (minimum) and $t_{CO}$ (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for mini-LVDS are shown in Figure 5–6.

*Figure 5–6. mini-LVDS Transmitter AC Timing Specification*




*Notes to Figure 5–6:*
(1) The data setup time, $t_{SU}$, is 0.225 × TUI.
(2) The data hold time, $t_H$, is 0.225 × TUI.

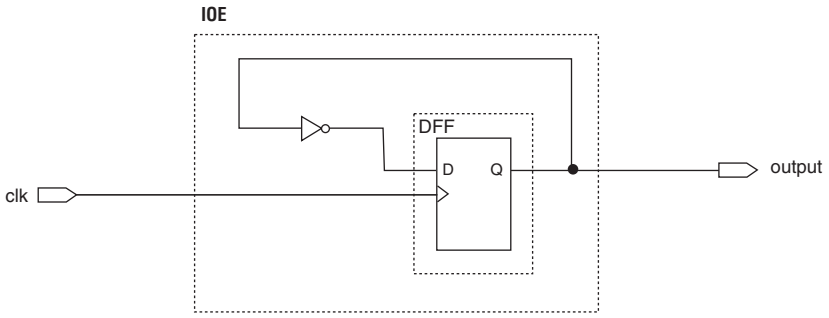
(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

## DCD Measurement Techniques

DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 5–9). Therefore, any DCD present on the input clock signal, or caused by the clock input buffer, or different input I/O standard, does not transfer to the output signal.

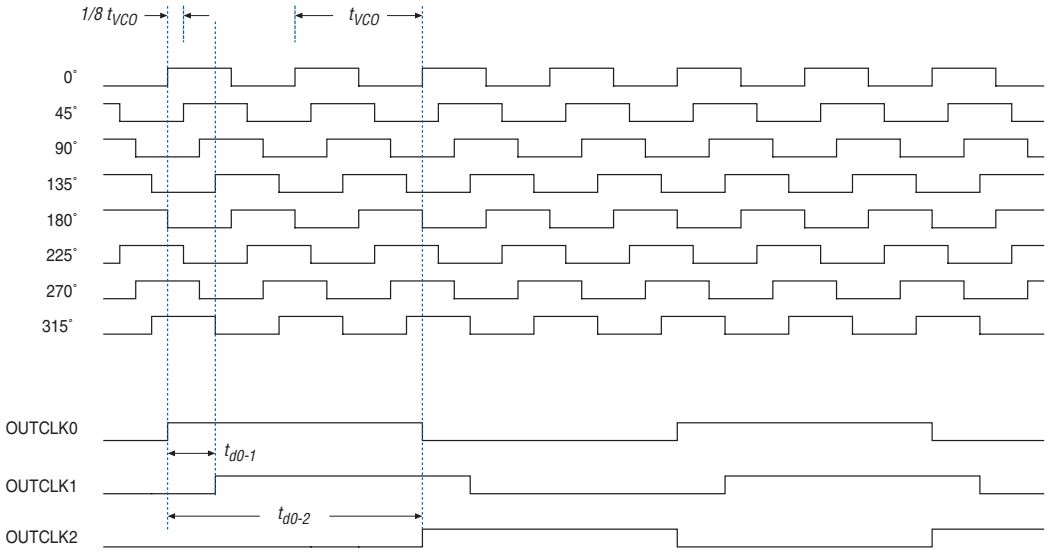
*Figure 5–9. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs*




However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 5–10). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

$\Delta t_{FINE}$ periods. OUTCLK2 is based off the 0° phase from the VCO but has the S value for the counter set to 3. This creates a delay of two $\Delta t_{COARSE}$ periods.

*Figure 7–8. Cyclone II PLL Phase Shifting using VCO Phase Output & Counter Delay Time*



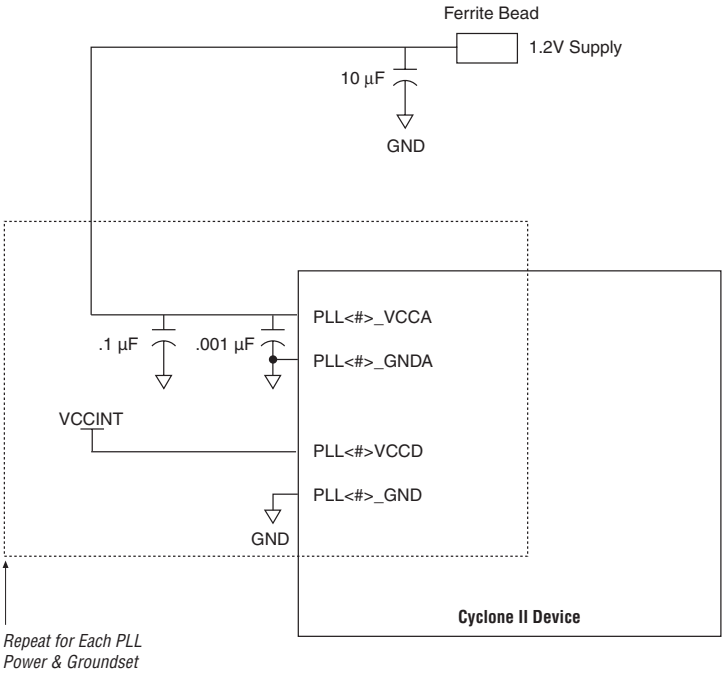

## Control Signals

The four control signals in Cyclone II PLLs (pllena, areset, pfdena, and locked) control PLL operation.

### *pllena*

The PLL enable signal, pllena, enables and disables the PLL. You can either enable/disable a single PLL (by connecting pllena port independently) or multiple PLLs (by connecting pllena ports together). The pllena signal is an active-high signal. When pllena is low, the PLL clock output ports are driven by GND and the PLL loses lock. All PLL counters, including gated lock counter return to default state. When pllena transitions high, the PLL relocks and resynchronizes to the input clock. In Cyclone II devices, the pllena port can be fed by an LE output or any general-purpose I/O pin. There is no dedicated pllena pin. This increases flexibility since each PLL can have its own pllena control circuitry or all PLLs can share the same pllena circuitry. The pllena signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to $V_{CC}$.

*Figure 7–17. PLL Power Schematic for Cyclone II PLLs*




***Note to Figure 7–17:***
(1) Applies to PLLs 1 through 4.

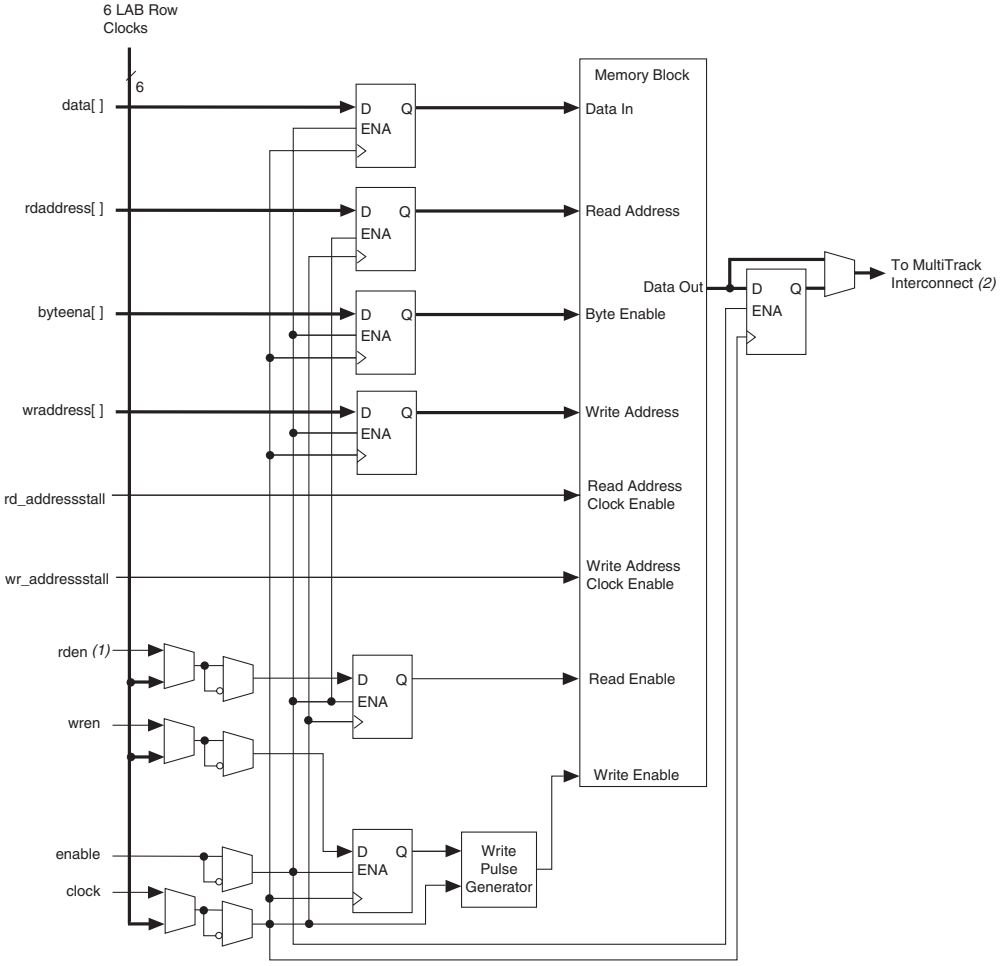
## VCCD & GND

The digital power and ground pins are labeled VCCD_ PLL<*PLL number*> and GND_PLL<*PLL number*>. The VCCD pin supplies the power for the digital circuitry in the PLL. Connect these VCCD pins to the quietest digital supply on the board. In most systems, this is the digital 1.2-V supply supplied to the device's $V_{CCINT}$ pins. Connect the VCCD pins to a power supply even if you do not use the PLL. When connecting the $V_{CCD}$ pins to $V_{CCINT}$, you do not need any filtering or isolation. You can connect the GND pins directly to the same ground plane as the device's digital ground. See Figure 7–17.

# Conclusion

Cyclone II device PLLs provide you with complete control of device clocks and system timing. These PLLs support clock multiplication/division, phase shift, and programmable duty cycle for your cost-sensitive clock synthesis applications.

*Figure 8–19. Cyclone II Single-Clock Mode in Simple Dual-Port Mode* *Notes (1), (2)*




*Notes to Figure 8–19:*

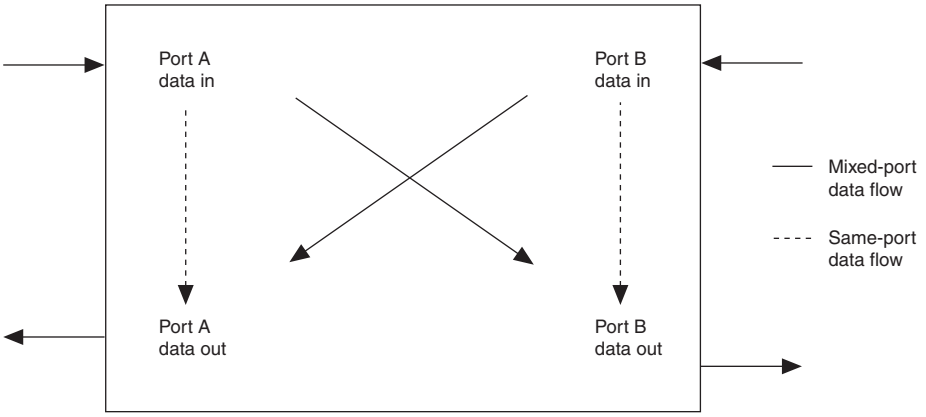
(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

## Read-During-Write Operation at the Same Address

The "Same-Port Read-During-Write Mode" and "Mixed-Port Read-During-Write Mode" sections describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two read-during-write data flows: same-port and mixed-port. Figure 8–21 shows the difference between these flows.

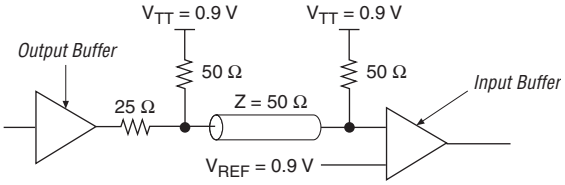
*Figure 8–21. Cyclone II Read-During-Write Data Flow*




### Same-Port Read-During-Write Mode

For read-during-write operation of a single-port RAM or the same port of a true dual-port RAM, the new data is available on the rising edge of the same clock cycle on which it was written. Figure 8–22 shows a sample functional waveform. When using byte enables in true dual-port RAM mode, the outputs for the masked bytes on the same port are unknown (see Figure 8–2 on page 8–6). The non-masked bytes are read out as shown in Figure 8–22.

*Figure 10–6. 1.8-V SSTL Class II Termination*




## 1.8-V HSTL Class I and II

The HSTL standard is a technology independent I/O standard developed by JEDEC to provide voltage scalability. It is used for applications designed to operate in the 0.0- to 1.8-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces.

Although JEDEC specifies a maximum $V_{CCIO}$ value of 1.6 V, there are various memory chip vendors with HSTL standards that require a $V_{CCIO}$ of 1.8 V. Cyclone II devices support interfaces with $V_{CCIO}$ of 1.8 V for HSTL. Figures 10–7 and 10–8 show the nominal $V_{REF}$ and $V_{TT}$ required to track the higher value of $V_{CCIO}$. The value of $V_{REF}$ is selected to provide optimum noise margin in the system. Cyclone II devices support both input and output levels of operation.

*Figure 10–7. 1.8-V HSTL Class I Termination*

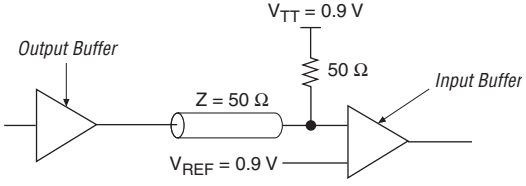
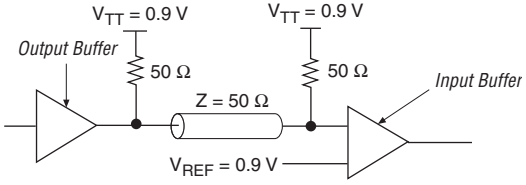



*Figure 10–8. 1.8-V HSTL Class II Termination*



software makes it easy to use these I/O standards in Cyclone II device designs. After design compilation, the software also provides clear, visual representations of pads and pins and the selected I/O standards. Taking advantage of the support of these I/O standards in Cyclone II devices allows you to lower your design costs without compromising design flexibility or complexity.

## References

For more information on the I/O standards referred to in this document, refer to the following sources:


- Stub Series Terminated Logic for 2.5-V (SSTL-2), JESD8-9A, Electronic Industries Association, December 2000.
- 1.5-V +/- 0.1-V (Normal Range) and 0.9-V - 1.6-V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-11, Electronic Industries Association, October 2000.
- 1.8-V +/- 0.15-V (Normal Range) and 1.2-V - 1.95-V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-7, Electronic Industries Association, February 1997.
- 2.5-V +/- 0.2-V (Normal Range) and 1.8-V to 2.7-V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits, JESD8-5, Electronic Industries Association, October 1995.
- Interface Standard for Nominal 3-V/ 3.3-V Supply Digital Integrated Circuits, JESD8-B, Electronic Industries Association, September 1999.
- PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group, December 1998.
- Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, ANSI/TIA/EIA-644, American National Standards Institute/Telecommunications Industry/Electronic Industries Association, October 1995.

- Maintain equal distance between traces in LVDS pairs, as much as possible. Routing the pair of traces close to each other maximizes the common-mode rejection ratio (CMRR).
- Longer traces have more inductance and capacitance. These traces should be as short as possible to limit signal integrity issues.
- Place termination resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° or 45° corners.
- Use high-performance connectors.
- Design backplane and card traces so that trace impedance matches the connector's and/or the termination's impedance.
- Keep equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths result in misplaced crossing points and decrease system margins as the channel-to-channel skew (TCCS) value increases.
- Limit vias because they cause discontinuities.
- Use the common bypass capacitor values such as 0.001, 0.01, and 0.1 µF to decouple the high-speed PLL power and ground planes.
- Keep switching transistor-to-transistor logic (TTL) signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Analyze system-level signals.

For PCB layout guidelines, see *AN 224: High-Speed Board Layout Guidelines*.

## Conclusion

Cyclone II differential I/O capabilities enable you to keep pace with increasing design complexity. Support for I/O standards including LVDS, LVPECL, RSDS, mini-LVDS, differential SSTL and differential HSTL allows Cyclone II devices to fit into a wide variety of applications. Taking advantage of these I/O capabilities and Cyclone II pricing allows you to lower your design costs while remaining on the cutting edge of technology.

# 15. Package Information for Cyclone II Devices

CII51015-2.3

## Introduction

This chapter provides package information for Altera® Cyclone® II devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Table 15–1 shows Cyclone II device package options.

*Table 15–1. Cyclone II Device Package Options*

| Device | Package | Pins |
|---|---|---|
| EP2C5 | Plastic Thin Quad Flat Pack (TQFP) – Wirebond | 144 |
| | Plastic Quad Flat Pack (PQFP) – Wirebond | 208 |
| | Low profile FineLine BGA® – Wirebond | 256 |
| EP2C8 | TQFP – Wirebond | 144 |
| | PQFP – Wirebond | 208 |
| | Low profile FineLine BGA – Wirebond | 256 |
| EP2C15 | Low profile FineLine BGA, Option 2 – Wirebond | 256 |
| | FineLine BGA, Option 3– Wirebond | 484 |
| EP2C20 | PQFP – Wirebond | 240 |
| | Low profile FineLine BGA, Option 2 – Wirebond | 256 |
| | FineLine BGA, Option 3– Wirebond | 484 |
| EP2C35 | FineLine BGA, Option 3 – Wirebond | 484 |
| | Ultra FineLine BGA – Wirebond | 484 |
| | FineLine BGA, Option 3 – Wirebond | 672 |
| EP2C50 | FineLine BGA, Option 3 – Wirebond | 484 |
| | Ultra FineLine BGA – Wirebond | 484 |
| | FineLine BGA, Option 3 – Wirebond | 672 |
| EP2C70 | FineLine BGA, Option 3 – Wirebond | 672 |
| | FineLine BGA – Wirebond | 896 |

# Thermal Resistance

Thermal resistance values for Cyclone II devices are provided for a board meeting JEDEC specifications and for a typical board. The values provided are as follows:

- $\theta_{JA}$ (°C/W) Still Air—Junction-to-ambient thermal resistance with no airflow when a heat sink is not being used.
- $\theta_{JA}$ (°C/W) 100 ft./minute—Junction-to-ambient thermal resistance with 100 ft./minute airflow when a heat sink is not being used.
- $\theta_{JA}$ (°C/W) 200 ft./minute—Junction-to-ambient thermal resistance with 200 ft./minute airflow when a heat sink is not being used.
- $\theta_{JA}$ (°C/W) 400 ft./minute—Junction-to-ambient thermal resistance with 400 ft./minute airflow when a heat sink is not being used.
- $\theta_{JC}$ (°C/W)—Junction-to-case thermal resistance for device.
- $\theta_{JB}$ (°C/W)—Junction-to-board thermal resistance for specific board being used.

Table 15–2 provides $\theta_{JA}$ (junction-to-ambient thermal resistance) values and $\theta_{JC}$ (junction-to-case thermal resistance) values for Cyclone II devices on a board meeting JEDEC specifications for thermal resistance calculation. The JEDEC board specifications require two signal and two power/ground planes and are available at **www.jedec.org**.

*Table 15–2. Thermal Resistance of Cyclone II Devices for Board Meeting JEDEC Specifications (Part 1 of 2)*

| Device | Pin Count | Package | $\theta_{JA}$ (°C/W) Still Air | $\theta_{JA}$ (°C/W) 100 ft./min. | $\theta_{JA}$ (°C/W) 200 ft./min. | $\theta_{JA}$ (°C/W) 400 ft./min. | $\theta_{JC}$ (°C/W) |
|---|---|---|---|---|---|---|---|
| EP2C5 | 144 | TQFP | 31 | 29.3 | 27.9 | 25.5 | 10 |
| | 208 | PQFP | 30.4 | 29.2 | 27.3 | 22.3 | 5.5 |
| | 256 | FineLine BGA | 30.2 | 26.1 | 23.6 | 21.7 | 8.7 |
| EP2C8 | 144 | TQFP | 29.8 | 28.3 | 26.9 | 24.9 | 9.9 |
| | 208 | PQFP | 30.2 | 28.8 | 26.9 | 21.7 | 5.4 |
| | 256 | FineLine BGA | 27 | 23 | 20.5 | 18.5 | 7.1 |
| EP2C15 | 256 | FineLine BGA | 24.2 | 20 | 17.8 | 16 | 5.5 |
| | 484 | FineLine BGA | 21 | 17 | 14.8 | 13.1 | 4.2 |
| EP2C20 | 240 | PQFP | 26.6 | 24 | 21.4 | 17.4 | 4.2 |
| | 256 | FineLine BGA | 24.2 | 20 | 17.8 | 16 | 5.5 |
| | 484 | FineLine BGA | 21 | 17 | 14.8 | 13.1 | 4.2 |
| EP2C35 | 484 | FineLine BGA | 19.4 | 15.4 | 13.3 | 11.7 | 3.3 |
| | 484 | Ultra FineLine BGA | 20.6 | 16.6 | 14.5 | 12.8 | 5 |
| | 672 | FineLine BGA | 18.6 | 14.6 | 12.6 | 11.1 | 3.1 |