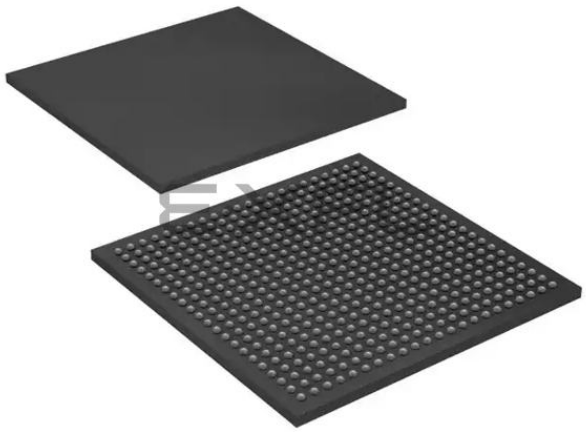

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	322
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35f484c7

Contents

Section I. Cyclone II Device Family Data Sheet

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. It contains the required PCB layout guidelines, device pin tables, and package specifications.

This section includes the following chapters:

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

A LAB-wide asynchronous load signal to control the logic for the register's preset signal is not available. The register preset is achieved by using a NOT gate push-back technique. Cyclone II devices can only support either a preset or asynchronous clear signal.

In addition to the clear port, Cyclone II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Cyclone II architecture, connections between LEs, M4K memory blocks, embedded multipliers, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row (direct link, R4, and R24) and column (register chain, C4, and C16) interconnects that span fixed distances. A routing structure with fixed-length resources for all devices allows predictable and repeatable performance when migrating through different device densities.

Row Interconnects

Dedicated row interconnects route signals to and from LABs, PLLs, M4K memory blocks, and embedded multipliers within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 interconnects for high-speed access across the length of the device

There are five dynamic control input signals that feed the embedded multiplier: `signa`, `signb`, `clk`, `clkena`, and `aclr`. `signa` and `signb` can be registered to match the data signal input path. The same `clk`, `clkena`, and `aclr` signals feed all registers within a single embedded multiplier.

For more information on Cyclone II embedded multipliers, see the *Embedded Multipliers in Cyclone II Devices* chapter.

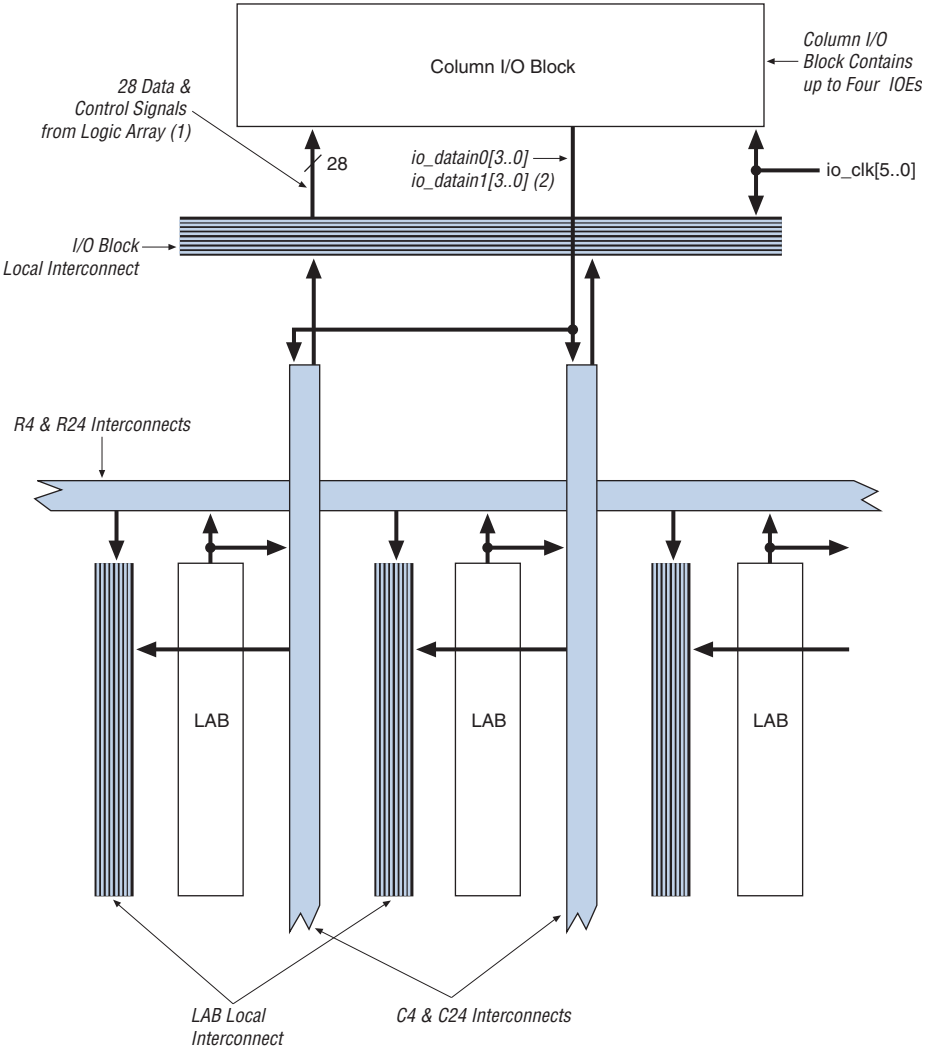
I/O Structure & Features

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- V_{REF} pins

Cyclone II device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–20 shows the Cyclone II IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. You can use IOEs as input, output, or bidirectional pins.

Figure 2–22. Column I/O Block Connection to the Interconnect



Notes to Figure 2–22:

(1) The 28 data and control signals consist of four data out lines, `io_dataout[3..0]`, four output enables, `io_coe[3..0]`, four input clock enables, `io_cce_in[3..0]`, four output clock enables, `io_cce_out[3..0]`, four clocks, `io_cclk[3..0]`, four asynchronous clear signals, `io_caclr[3..0]`, and four synchronous clear signals, `io_csclr[3..0]`.

(2) Each of the four IOEs in the column I/O block can have two `io_datain` (combinational or registered) inputs.

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 2 of 2) *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups *(5)*, *(6)*	Number of ×16 Groups	Number of ×18 Groups *(5)*, *(6)*
EP2C35	484-pin FineLine BGA	16 *(4)*	8	8	8
	672-pin FineLine BGA	20 *(4)*	8	8	8
EP2C50	484-pin FineLine BGA	16 *(4)*	8	8	8
	672-pin FineLine BGA	20 *(4)*	8	8	8
EP2C70	672-pin FineLine BGA	20 *(4)*	8	8	8
	896-pin FineLine BGA	20 *(4)*	8	8	8

Notes to Table 2–15:

(1) Numbers are preliminary.
(2) EP2C5 and EP2C8 devices in the 144-pin TQFP package do not have any DQ pin groups in I/O bank 1.
(3) Because of available clock resources, only a total of 6 DQ/DQS groups can be implemented.
(4) Because of available clock resources, only a total of 14 DQ/DQS groups can be implemented.
(5) The ×9 DQS/DQ groups are also used as ×8 DQS/DQ groups. The ×18 DQS/DQ groups are also used as ×16 DQS/DQ groups.
(6) For QDRI implementation, if you connect the D ports (write data) to the Cyclone II DQ pins, the total available ×9 DQS /DQ and ×18 DQS/DQ groups are half of that shown in Table 2–15.

You can use any of the DQ pins for the parity pins in Cyclone II devices. The Cyclone II device family supports parity in the ×8/×9, and ×16/×18 mode. There is one parity bit available per eight bits of data pins.

The data mask, DM, pins are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pin indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. In Cyclone II devices, the DM pins are assigned and are the preferred pins. Each group of DQS and DQ signals requires a DM pin.

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two clock outputs is needed to generate the system and write clock. The system clock is used to clock the DQS write signals, commands, and addresses. The write clock is shifted by –90° from the system clock and is used to clock the DQ signals during writes.

Figure 2–27 illustrates DDR SDRAM interfacing from the I/O through the dedicated circuitry to the logic array.

Table 5–57. Maximum for DDIO Output on Row Pins with PLL in the Clock Path Notes (1), (2) (Part 2 of 2)

Row Pins with PLL in the Clock Path	C6	C7	C8	Unit
1.5-V	280	280	280	ps
SSTL-2 Class I	150	190	230	ps
SSTL-2 Class II	155	200	230	ps
SSTL-18 Class I	180	240	260	ps
HSTL-18 Class I	180	235	235	ps
HSTL-15 Class I	205	220	220	ps
Differential SSTL-2 Class I	150	190	230	ps
Differential SSTL-2 Class II	155	200	230	ps
Differential SSTL-18 Class I	180	240	260	ps
Differential HSTL-18 Class I	180	235	235	ps
Differential HSTL-15 Class I	205	220	220	ps
LVDS	95	110	120	ps
Simple RSDS	100	155	155	ps
Mini LVDS	95	110	120	ps
PCI	285	305	335	ps
PCI-X	285	305	335	ps

Notes to Table 5–57:

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

For DDIO outputs, you can calculate actual half period from the following equation:

Actual half period = ideal half period – maximum DCD

For example, if the DDR output I/O standard is SSTL-2 Class II, the maximum DCD for a –5 device is 155 ps (refer to Table 5–57). If the clock frequency is 167 MHz, the half-clock period T/2 is:

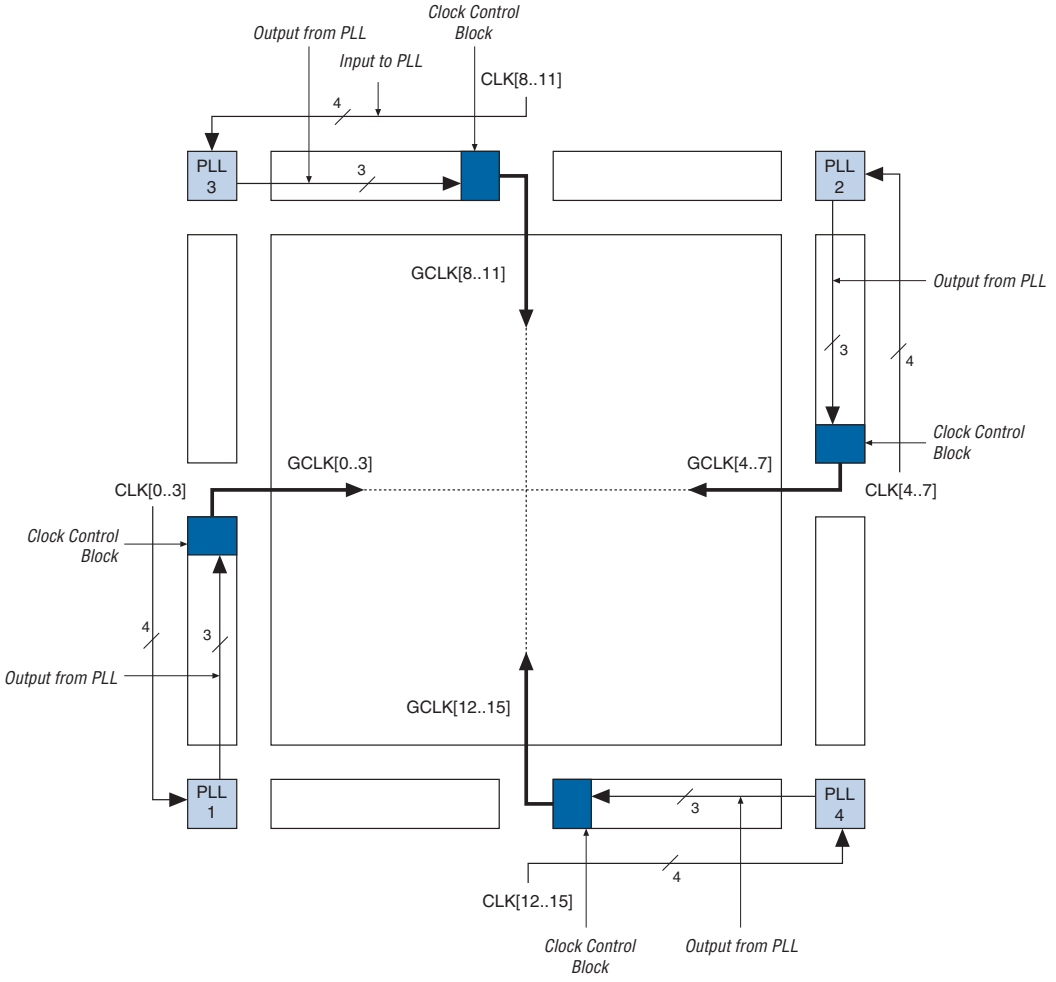
T/2 = 1/(2* f)= 1 /(2*167 MHz) = 3 ns = 3000 ps

Table 7–8 shows the clock sources connectivity to the global clock networks.

Table 7–8. Global Clock Network Connections (Part 1 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CLK0/LVDSCLK0p	✓		✓													
CLK1/LVDSCLK0n		✓	✓													
CLK2/LVDSCLK1p	✓			✓												
CLK3/LVDSCLK1n		✓		✓												
CLK4/LVDSCLK2p					✓		✓									
CLK5/LVDSCLK2n						✓	✓									
CLK6/LVDSCLK3p					✓			✓								
CLK7/LVDSCLK3n						✓		✓								
CLK8/LVDSCLK4n									✓		✓					
CLK9/LVDSCLK4p										✓	✓					
CLK10/LVDSCLK5n									✓			✓				
CLK11/LVDSCLK5p										✓		✓				
CLK12/LVDSCLK6n													✓		✓	
CLK13/LVDSCLK6p														✓	✓	
CLK14/LVDSCLK7n													✓			✓
CLK15/LVDSCLK7p														✓		✓
PLL1_c0	✓	✓		✓												
PLL1_c1	✓		✓	✓												
PLL1_c2		✓	✓													
PLL2_c0					✓	✓		✓								
PLL2_c1					✓		✓	✓								
PLL2_c2						✓	✓									
PLL3_c0									✓	✓		✓				
PLL3_c1									✓		✓	✓				
PLL3_c2										✓	✓					

Figure 7–12. Cyclone II Clock Control Blocks Placement



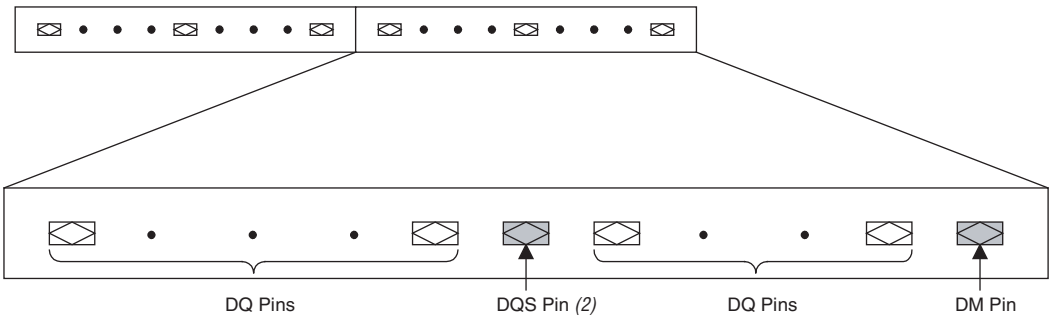
The inputs to the four clock control blocks on each side are chosen from among the following clock sources:

- Four clock input pins
- Three PLL counter outputs
- Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins and two CDPCLK pins from both the top and bottom
- Four signals from internal logic

DDR Memory Interface Pins

Cyclone II devices use data (DQ), data strobe (DQS), and clock pins to interface with external memory. Figure 9–6 shows the DQ and DQS pins in the ×8/×9 mode.

Figure 9–6. Cyclone II Device DQ & DQS Groups in ×8/×9 Mode *Notes (1), (3)*



Notes to Figure 9–6:

(1) Each DQ group consists of a DQS pin, a DM pin, and up to nine DQ pins.

(2) For the QDRII memory interface, other DQS pins implement the CQn pins. These pins are denoted by DQS/CQ# in the pin table.

(3) This is an idealized pin layout. For the actual pin layout, refer to the pin tables in the *PCB Layout Guidelines* section of the *Cyclone II Device Handbook, Volume 1*.

Data & Data Strobe Pins

Cyclone II data pins for the DDR memory interfaces are called DQ pins. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. Depending on the external memory interface, either the memory device's read data strobes or read clocks feed the DQS pins.

In Cyclone II devices, all the I/O banks support DDR and DDR2 SDRAM and QDRII SRAM memory at up to 167 MHz. All the I/O banks support DQS signals with the DQ bus modes of ×8/×9 and ×16/×18. Cyclone II devices can support either bidirectional data strobes or unidirectional read clocks.

DDR2 and QDRII interfaces with class II I/O standard can only be implemented on the top and bottom I/O banks of the Cyclone II device.

For example, to implement a 72-bit wide SDRAM memory interface in Cyclone II devices, use 5 DQS/DQ groups in the top I/O bank and 4 DQS/DQ groups in the bottom I/O bank, or vice-versa. In this case, if DQS0T or DQS1T is used for the fifth DQS signal, the DQS2R or DQS2L pins become regular I/O pins and are unavailable for DQS signals in memory interface. For detailed information about the global clock network, refer to the *Global Clock Network & Phase Locked Loops* section in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

You must configure the DQ and DQS pins as bidirectional DDR pins on all the I/O banks of the device. Use the `altdq` and `altdqs` megafunctions to configure the DQ and DQS paths, respectively. If you only want to use the DQ or DQS pins as inputs, for instance in the QDRII memory interface where DQ and DQS are unidirectional read data and read clock, set the output enable of the DQ or DQS pins to ground. For further information, please refer to the section "QDRII SRAM" on page 9–5 of this handbook.

Clock, Command & Address Pins

You can use any of the user I/O pins on all the I/O banks (that support the external memory's I/O standard) of the device to generate clocks and command and address signals to the memory device.

Parity, DM & ECC Pins

You can use any of the DQ pins for the parity pins in Cyclone II devices. Cyclone II devices support parity in the ×8/×9 and ×16/×18 modes. There is one parity bit available per 8 bits of data pins.

The data mask (DM) pins are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pin indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. In Cyclone II devices, the DM pins are pre-assigned in the device pin outs, and these are the preferred pins. Each group of DQS and DQ signals requires a DM pin. Similar to the DQ output signals, the DM signals are clocked by the –90° shifted clock.

Some DDR SDRAM and DDR2 SDRAM devices support error correction coding (ECC) or parity. Parity bit checking is a way to detect errors, but it has no correction capabilities. ECC can detect and automatically correct errors in data transmission. In 72-bit DDR SDRAM, there are 8 ECC pins on top of the 64 data pins. Connect the DDR and DDR2 SDRAM ECC pins to a Cyclone II device's DQS/DQ group. The memory controller needs extra logic to encode and decode the ECC data.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pads in relation to differential pads in the same I/O bank. Use the following guidelines for placing single-ended pads with respect to differential pads and for differential output pads placement in Cyclone II devices.

For the LVDS I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVDS I/O pad.
- Single-ended outputs can be no closer than five pads away from an LVDS I/O pad.
- Maximum of four 155-MHz (or greater) LVDS output channels per VCCIO and ground pair.
- Maximum of three 311-MHz (or greater) LVDS output channels per VCCIO and ground pair.

For optimal signal integrity at the LVDS input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVDS input pad.

The Quartus II software only checks the first two cases.

For the RSDS and mini-LVDS I/O standards:

- Single-ended inputs can be no closer than four pads away from an RSDS and mini-LVDS output pad.
- Single-ended outputs can be no closer than five pads away from an RSDS and mini-LVDS output pad.
- Maximum of three 85-MHz (or greater) RSDS and mini-LVDS output channels per VCCIO and ground pair.

The Quartus II software only checks the first two cases.

For the LVPECL I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVPECL input pad.
- Single-ended outputs can be no closer than five pads away from an LVPECL input pad.

For optimal signal integrity at the LVPECL input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVPECL input pad.

Table 13–1. Cyclone II Configuration Schemes		
Configuration Scheme	**MSEL1**	**MSEL0**
AS (20 MHz)	0	0
PS	0	1
Fast AS (40 MHz) *(1)*	1	0
JTAG-based Configuration *(2)*	*(3)*	*(3)*

Notes to Table 13–1:

(1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

(2) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

(3) Do not leave the MSEL pins floating; connect them to V_{CCIO} or ground. These pins support the non-JTAG configuration scheme used in production. If you are only using JTAG configuration, you should connect the MSEL pins to ground.

You can download configuration data to Cyclone II FPGAs with the AS, PS, or JTAG interfaces using the options in Table 13–2.

Table 13–2. Cyclone II Device Configuration Schemes	
Configuration Scheme	**Description**
AS configuration	Configuration using serial configuration devices (EPCS1, EPCS4, EPCS16 or EPCS64 devices)
PS configuration	Configuration using enhanced configuration devices (EPC4, EPC8, and EPC16 devices), EPC2 and EPC1 configuration devices, an intelligent host (microprocessor), or a download cable
JTAG-based configuration	Configuration via JTAG pins using a download cable, an intelligent host (microprocessor), or the Jam™ Standard Test and Programming Language (STAPL)

Configuration File Format

Table 13–3 shows the approximate uncompressed configuration file sizes for Cyclone II devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

Table 13–3. Cyclone II Raw Binary File (.rbf) Sizes *Note (1)*

Device	Data Size (Bits)	Data Size (Bytes)
EP2C5	1,265,792	152,998
EP2C8	1,983,536	247,974
EP2C15	3,892,496	486,562
EP2C20	3,892,496	486,562
EP2C35	6,858,656	857,332
EP2C50	9,963,392	1,245,424
EP2C70	14,319,216	1,789,902

Note to Table 13–3:
(1) These values are preliminary.

Use the data in Table 13–3 only to estimate the file size before design compilation. Different configuration file formats, such as a Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) format, have different file sizes. However, for any specific version of the Quartus® II software, any design targeted for the same device has the same uncompressed configuration file size. If compression is used, the file size can vary after each compilation since the compression ratio is dependent on the design.

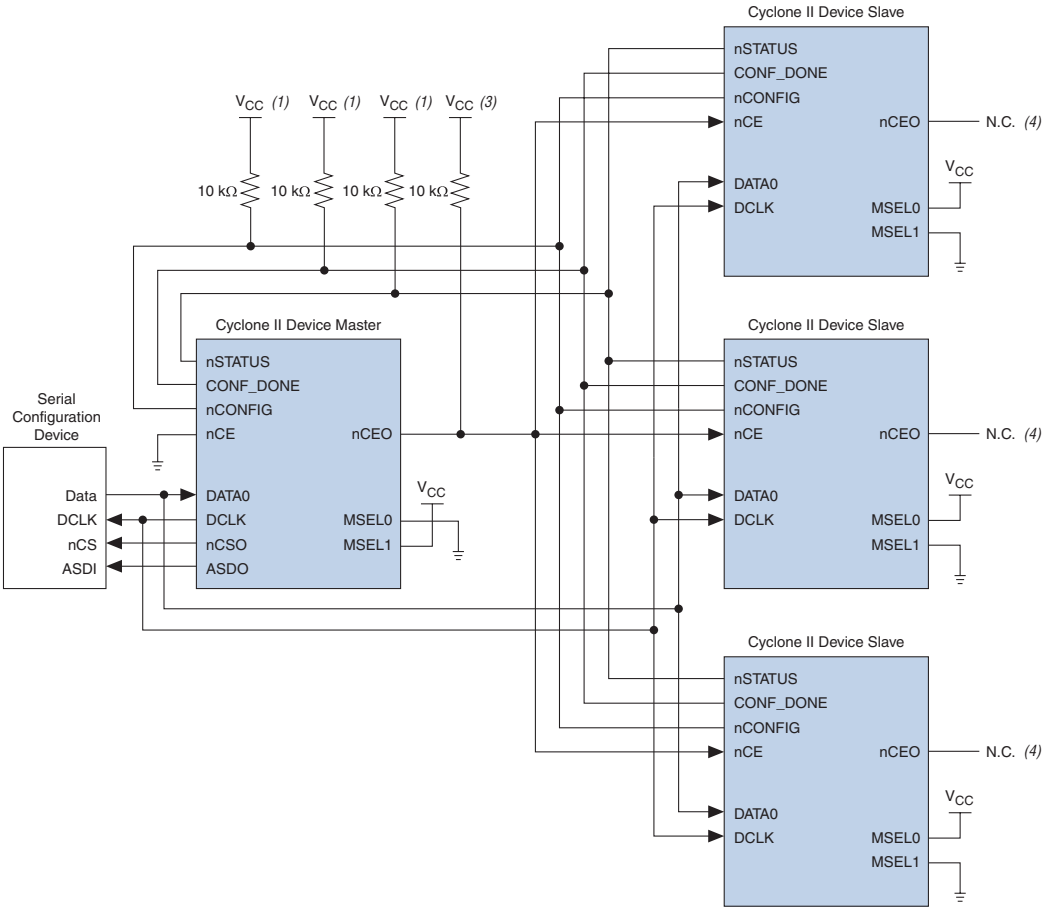
Configuration Data Compression

Cyclone II devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Cyclone II devices. During configuration, the Cyclone II device decompresses the bitstream in real time and programs its SRAM cells.

Preliminary data indicates that compression reduces configuration bitstream size by 35 to 55%.

Cyclone II devices support decompression in the AS and PS configuration schemes. Decompression is not supported in JTAG-based configuration.

Figure 13–5. Multiple Device AS Configuration When FPGAs Receive the Same Data with Multiple SOFs



Notes to Figure 13–5:

(1) Connect the pull-up resistors to a 3.3-V supply.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

Table 13–7 defines the timing parameters for Cyclone II devices for PS configuration.

Table 13–7. PS Timing Parameters for Cyclone II Devices

Symbol	Parameter	Minimum	Maximum	Units
t_{POR}	POR delay *(1)*	100		ms
t_{CF2CD}	nCONFIG low to CONF_DONE low		800	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low		800	ns
t_{CFG}	nCONFIG low pulse width	2		µs
t_{STATUS}	nSTATUS low pulse width	10	40 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high		40 *(2)*	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	40		µs
t_{ST2CK}	nSTATUS high to first rising edge on DCLK	1		µs
t_{DSU}	Data setup time before rising edge on DCLK	7		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CH}	DCLK high time	4		ns
t_{CL}	DCLK low time	4		ns
t_{CLK}	DCLK period	10		ns
f_{MAX}	DCLK frequency		100	MHz
t_{CD2UM}	CONF_DONE high to user mode *(3)*	18	40	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period		
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (299 × CLKUSR period)		

Notes to Table 13–7:

(1) The POR delay minimum of 100 ms only applies for non "A" devices.

(2) This value is applicable if users do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

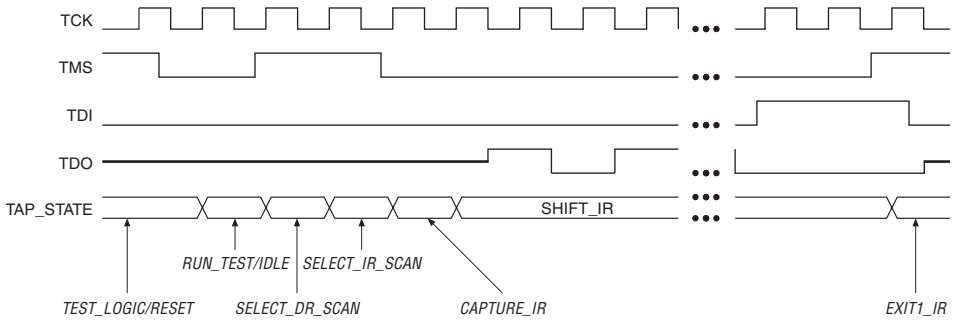
(3) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting the device.

Device configuration options and how to create configuration files are discussed further in the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

PS Configuration Using a Microprocessor

In the PS configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone II device.

Figure 14–7. Selecting the Instruction Mode



The TDO pin is tri-stated in all states except in the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the instruction code must be clocked at the same time that the next state, EXIT1_IR, is activated. Set TMS high to activate the EXIT1_IR state. Once in the EXIT1_IR state, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to serially shift test data in one of seven modes (SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE, USERCODE, CLAMP, or HIGHZ) that are described below.

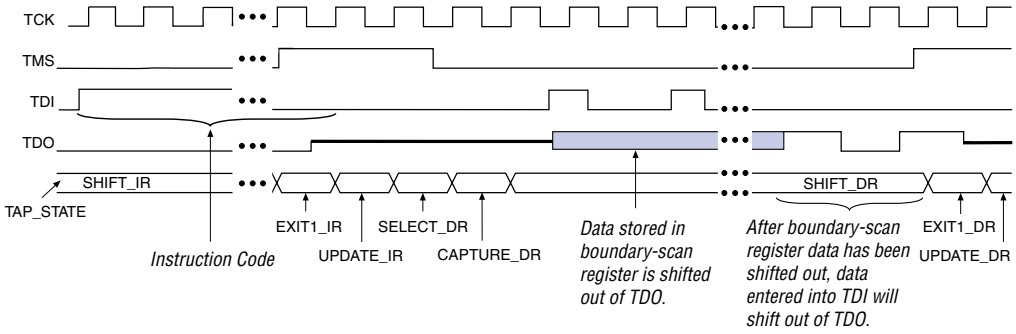
SAMPLE/PRELOAD Instruction Mode

The SAMPLE/PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. You can also use this instruction to preload the test data into the update registers prior to loading the EXTEST instruction. Figure 14–8 shows the capture, shift, and update phases of the SAMPLE/PRELOAD mode.

EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the output and output enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data. Thus, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers, then shifted out of TDO during the shift phase. New test data can then be stored in the update registers during the update phase.

The EXTEST waveform diagram in Figure 14–11 resembles the SAMPLE/PRELOAD waveform diagram, except for the instruction code. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

Figure 14–11. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS mode is activated when an instruction code of all 1's is loaded in the instruction register. The waveforms in Figure 14–12 show how scan data passes through a device once the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 15–8 shows a 896-pin FineLine BGA package outline.

Figure 15–8. 896-Pin FineLine BGA Package Outline