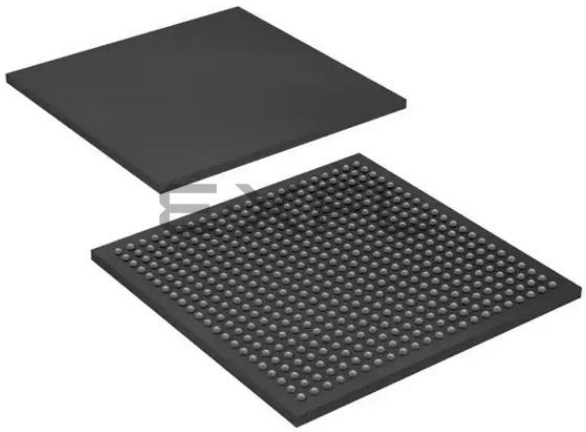

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

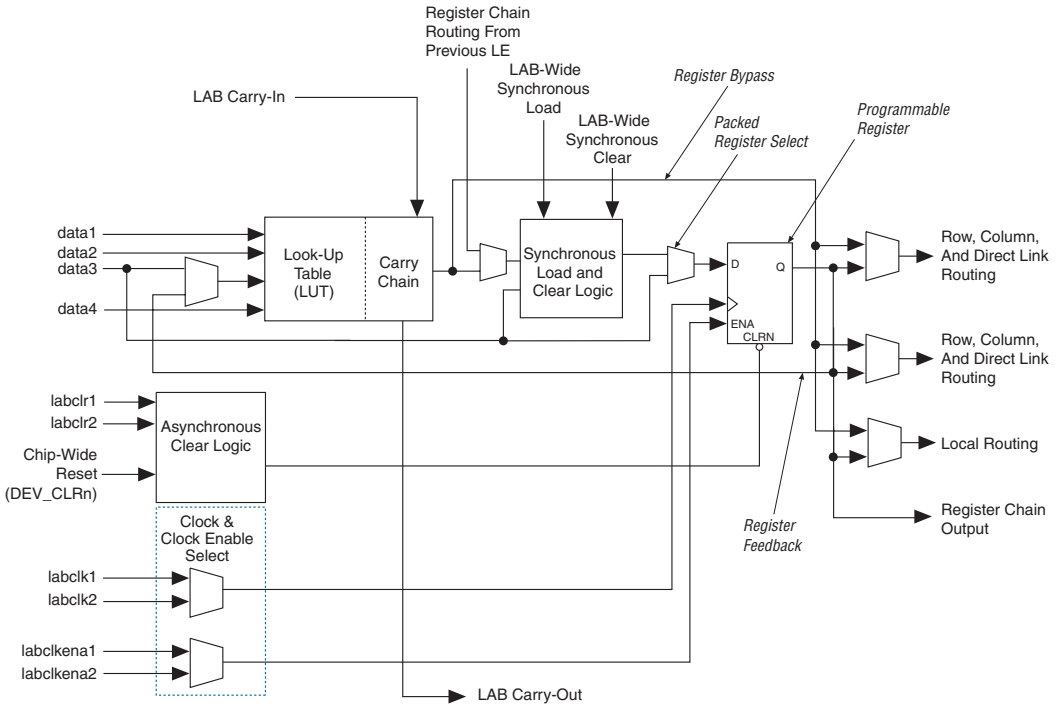
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	322
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35f484c7n

Figure 2–2 shows a Cyclone II LE.

Figure 2–2. Cyclone II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, clock, clock enable, and clear inputs. Signals that use the global clock network, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources, allowing the LUT to drive one output while the register drives another output. This feature, register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. When using register packing, the LAB-wide synchronous load control signal is not available. See "LAB Control Signals" on page 2–8 for more information.

Table 2–16. Programmable Drive Strength (Part 2 of 2) Note (1)		
I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top & Bottom I/O Pins	Side I/O Pins
LVCMOS (1.5 V)	2	2
	4	4
	6	6
	8	
SSTL-2 class I	8	8
	12	12
SSTL-2 class II	16	16
	20	
	24	
SSTL-18 class I	6	6
	8	8
	10	10
	12	
SSTL-18 class II	16	
	18	
HSTL-18 class I	8	8
	10	10
	12	12
HSTL-18 class II	16	
	18	
	20	
HSTL-15 class I	8	8
	10	
	12	
HSTL-15 class II	16	

Note to Table 2–16:
(1) The default current in the Quartus II software is the maximum setting for each I/O standard.

Open-Drain Output

Cyclone II devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (that is, interrupt and write-enable signals) that can be asserted by any of several devices.

standards (e.g., SSTL-2) independently. If an I/O bank does not use voltage-referenced standards, the VREF pins are available as user I/O pins.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs. Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value.

MultiVolt I/O Interface

The Cyclone II architecture supports the MultiVolt I/O interface feature, which allows Cyclone II devices in all packages to interface with systems of different supply voltages. Cyclone II devices have one set of V_{CC} pins (VCCINT) that power the internal device logic array and input buffers that use the LVPECL, LVDS, HSTL, or SSTL I/O standards. Cyclone II devices also have four or eight sets of VCC pins (VCCIO) that power the I/O output drivers and input buffers that use the LVTTL, LVCMOS, or PCI I/O standards.

The Cyclone II VCCINT pins must always be connected to a 1.2-V power supply. If the V_{CCINT} level is 1.2 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V systems. Table 2–20 summarizes Cyclone II MultiVolt I/O support.

Table 2–20. Cyclone II MultiVolt I/O Support (Part 1 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
1.5	✓	✓	✓ *(2)*	✓ *(2)*	✓			
1.8	✓ *(4)*	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓		
2.5			✓	✓	✓ *(5)*	✓ *(5)*	✓	

Table 5–9. DC Characteristics for User I/O Pins Using Differential I/O Standards Note (1) *(Part 2 of 2)*

I/O Standard	V_{OD} (mV)			ΔV_{OD} (mV)		V_{OCM} (V)			V_{OH} (V)		V_{OL} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
Differential 1.8-V HSTL class I and II (3)	—	—	—	—	—	—	—	—	V_{CCIO} – 0.4	—	—	0.4
Differential SSTL-2 class I (4)	—	—	—	—	—	—	—	—	V_{TT} + 0.57	—	—	V_{TT} – 0.57
Differential SSTL-2 class II (4)	—	—	—	—	—	—	—	—	V_{TT} + 0.76	—	—	V_{TT} – 0.76
Differential SSTL-18 class I (4)	—	—	—	—	—	0.5 × V_{CCIO} – 0.125	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.125	V_{TT} + 0.475	—	—	V_{TT} – 0.475
Differential SSTL-18 class II (4)	—	—	—	—	—	0.5 × V_{CCIO} – 0.125	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.125	V_{CCIO} – 0.28	—	—	0.28

Notes to Table 5–9:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
(2) The RSDS and mini-LVDS I/O standards are only supported on output pins.
(3) The differential 1.8-V HSTL and differential 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.
(4) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

DC Characteristics for Different Pin Types

Table 5–10 shows the types of pins that support bus hold circuitry.

Table 5–10. Bus Hold Support

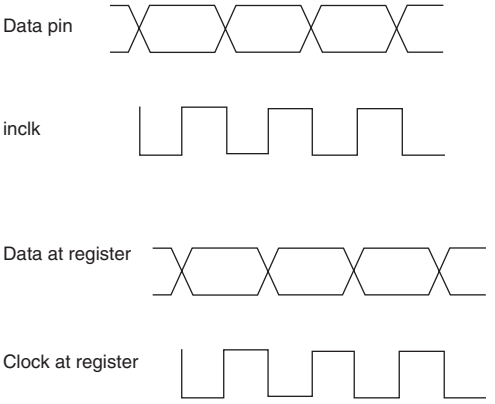
Pin Type	Bus Hold
I/O pins using single-ended I/O standards	Yes
I/O pins using differential I/O standards	No
Dedicated clock pins	No
JTAG	No
Configuration pins	No

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 4 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.5V_ DIFFERENTIAL_HSTL _CLASS_I	8 mA	210	170	140	210	170	140	210	170	140
	10 mA	220	180	150	—	—	—	—	—	—
	12 mA	230	190	160	—	—	—	—	—	—
1.5V_ DIFFERENTIAL_HSTL _CLASS_II	16 mA	210	170	140	—	—	—	—	—	—
LVDS	—	400	340	280	400	340	280	400	340	280
RSDS	—	400	340	280	400	340	280	400	340	280
MINI_LVDS	—	400	340	280	400	340	280	400	340	280
SIMPLE_RSDS	—	380	320	260	380	320	260	380	320	260
1.2V_HSTL	—	80	80	80	—	—	—	—	—	—
1.2V_ DIFFERENTIAL_HSTL	—	80	80	80	—	—	—	—	—	—
PCI	—	—	—	—	350	315	280	350	315	280
PCI-X	—	—	—	—	350	315	280	350	315	280
LVTTL	OCT_25_ OHMS	360	300	250	360	300	250	360	300	250
LVCMOS	OCT_25_ OHMS	360	300	250	360	300	250	360	300	250
2.5V	OCT_50_ OHMS	240	200	160	240	200	160	240	200	160
1.8V	OCT_50_ OHMS	290	240	200	290	240	200	290	240	200
SSTL_2_CLASS_I	OCT_50_ OHMS	240	200	160	240	200	160	—	—	—
SSTL_18_CLASS_I	OCT_50_ OHMS	290	240	200	290	240	200	—	—	—

Note to Table 5–45:
(1) This is based on single data rate I/Os.

Figure 7–7. Phase Relationship between Cyclone II PLL Clocks in Source-Synchronous Compensation Mode



Set the input pin to the register delay chain within the IOE to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL.

Hardware Features

Cyclone II device PLLs support a number of features for general-purpose clock management. This section discusses clock multiplication and division implementation, phase-shifting implementation and PLL lock circuits.

Clock Multiplication & Division

Cyclone II device PLLs provide clock synthesis for PLL output ports using $m/(n \times \text{post-scale})$ scaling factors. Every PLL has one pre-scale divider, n, with a range of 1 to 4 and one multiply counter, m, with a range of 1 to 32. The input clock, f_{IN}, is divided by a pre-scale counter, n, to produce the input reference clock, f_{REF}, to the PFD. This input reference clock, f_{REF}, is then multiplied by the m feedback factor. The control loop drives the VCO frequency to match $f_{IN} \times (m/n)$. The equations for these frequencies are:

$$f_{REF} = \frac{f_{IN}}{n}$$

$$f_{VCO} = f_{REF} \times m = f_{IN} \frac{m}{n}$$

locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals

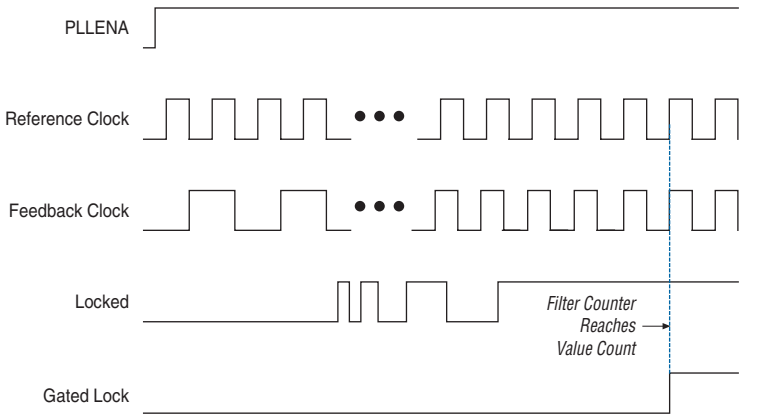
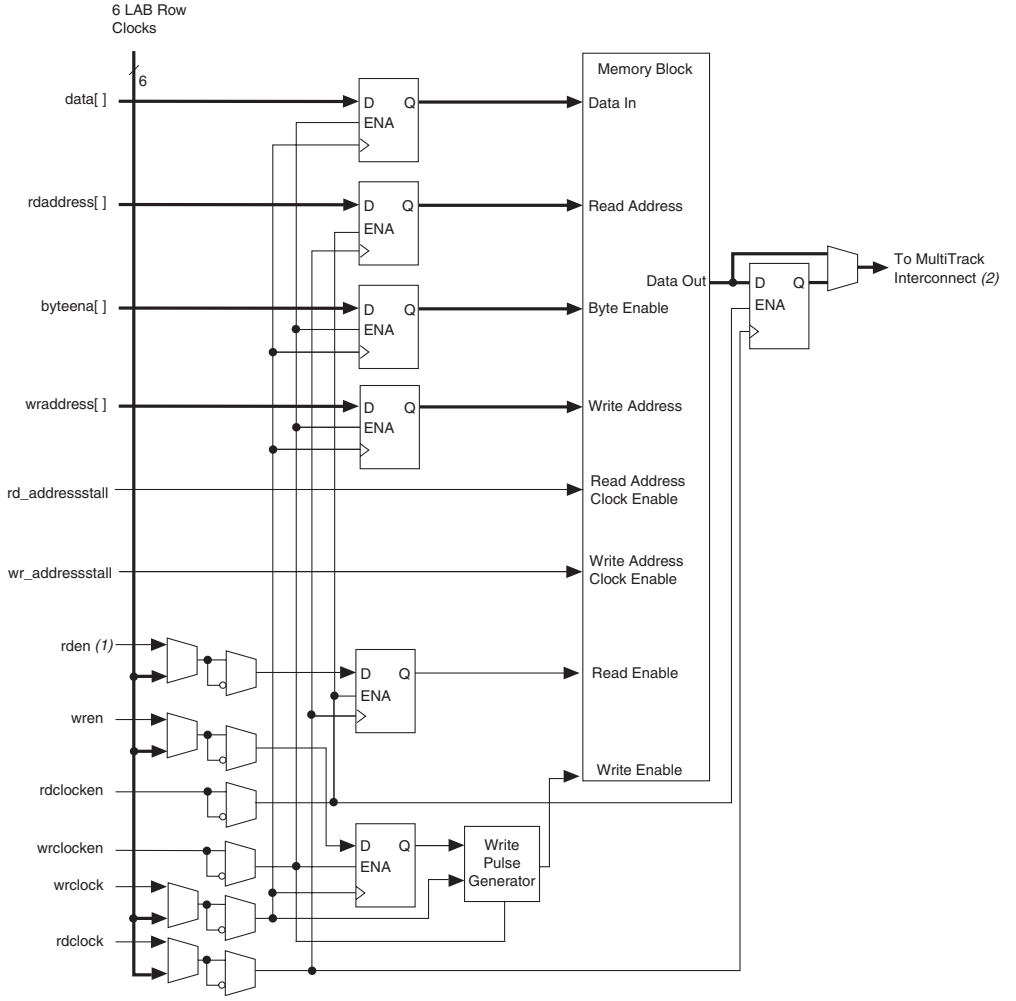


Figure 8–17. Cyclone II Read/Write Clock Mode *Notes (1), (2)*



Notes to Figure 8–17:

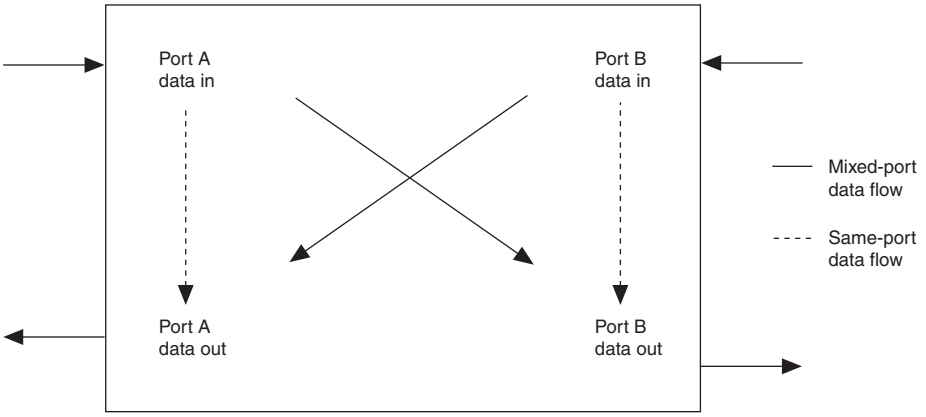
(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) For more information about the MultiTract interconnect, refer to *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Read-During-Write Operation at the Same Address

The "Same-Port Read-During-Write Mode" and "Mixed-Port Read-During-Write Mode" sections describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two read-during-write data flows: same-port and mixed-port. Figure 8–21 shows the difference between these flows.

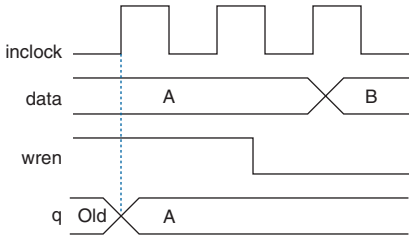
Figure 8–21. Cyclone II Read-During-Write Data Flow



Same-Port Read-During-Write Mode

For read-during-write operation of a single-port RAM or the same port of a true dual-port RAM, the new data is available on the rising edge of the same clock cycle on which it was written. Figure 8–22 shows a sample functional waveform. When using byte enables in true dual-port RAM mode, the outputs for the masked bytes on the same port are unknown (see Figure 8–2 on page 8–6). The non-masked bytes are read out as shown in Figure 8–22.

Figure 8–22. Cyclone II Same-Port Read-During-Write Functionality *Note (1)*



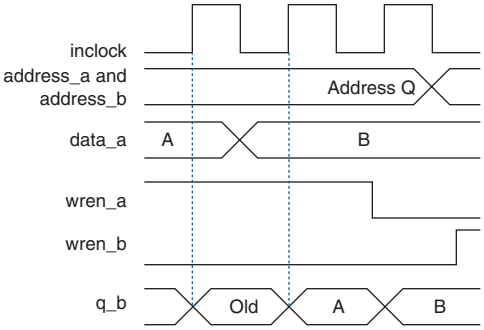
Note to Figure 8–22:
(1) Outputs are not registered.

Mixed-Port Read-During-Write Mode

This mode applies to a RAM in simple or true dual-port mode, which has one port reading and the other port writing to the same address location with the same clock.

In this mode, you also have two output choices: old data or don't care. In Old Data Mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In Don't Care Mode, the same operation results in a "don't care" or unknown value on the RAM outputs.

Figure 8–23. Cyclone II Mixed-Port Read-During-Write: Old Data Mode *Note (1)*



Note to Figure 8–23:
(1) Outputs are not registered.

QDRII SRAM devices use the following clock signals:

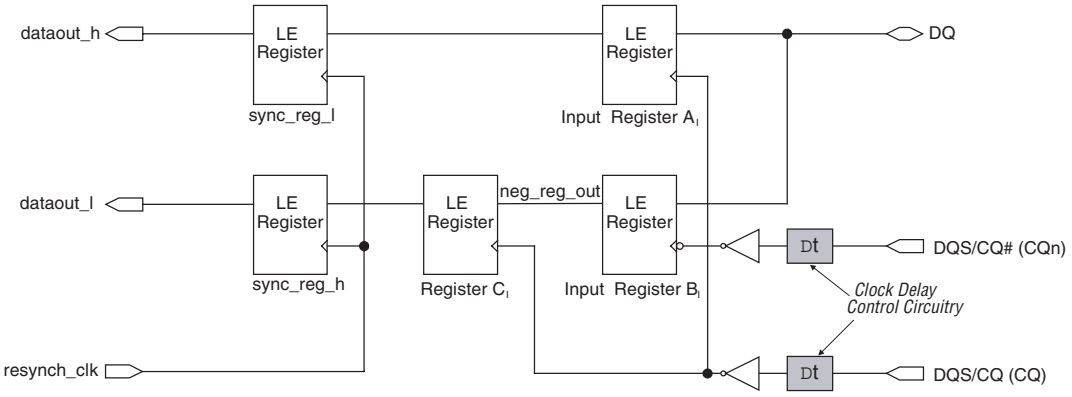
- Input clocks K and K#
- Optional output clocks C and C#
- Echo clocks CQ and CQn

Clocks C#, K#, and CQn are logical complements of clocks C, K, and CQ, respectively. Clocks C, C#, K, and K# are inputs to the QDRII SRAM, and clocks CQ and CQn are outputs from the QDRII SRAM. Cyclone II devices use single-clock mode for QDRII SRAM interfacing. The K and K# clocks are used for both read and write operations, and the C and C# clocks are unused.

You can generate C, C#, K, and K# clocks using any of the I/O registers via the DDR registers. Due to strict skew requirements between K and K# signals, use adjacent pins to generate the clock pair. Surround the pair with buffer pins tied to V_{CC} and pins tied to ground for better noise immunity from other signals.

In Cyclone II devices, another DQS pin implements the CQn pin in the QDRII SRAM memory interface. These pins are denoted by DQS/CQ# in the pin table. Connect CQ and CQn pins to the Cyclone II DQS/CQ and DQS/CQ# pins of the same DQ groups, respectively. You must configure the DQS/CQ and DQS/CQ# as bidirectional pins. However, because CQ and CQn pins are output-only pins from the memory device, the Cyclone II device's QDRII SRAM memory interface requires that you ground the DQS/CQ and DQS/CQ# output enable. To capture data presented by the memory device, connect the shifted CQ signal to register C_I and input register A_I. Connect the shifted CQn to input register B_I. Figure 9–4 shows the CQ and CQn connections for a QDRII SRAM read.

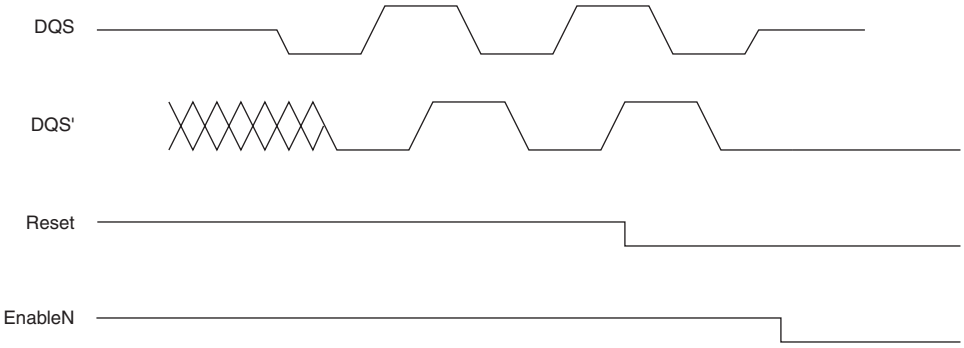
Figure 9–4. CQ & CQn Connection for QDRII SRAM Read



Read & Write Operation

Figure 9–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDRII SRAM devices send data within t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQn clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Cyclone II devices.

Figure 9–10. Cyclone II DQS Postamble Circuitry Control Timing Waveform



DDR Input Registers

In Cyclone II devices, the DDR input registers are implemented with five internal LE registers located in the logic array block (LAB) adjacent to the DDR input pin (see Figure 9–11). The DDR data is fed to the first two registers, input register A_I and input register B_I. Input register B_I captures the DDR data present during the rising edge of the clock. Input register A_I captures the DDR data present during the falling edge of the clock. Register C_I aligns the data before it is transferred to the resynchronization registers.

Figure 9–11. DDR Input Implementation

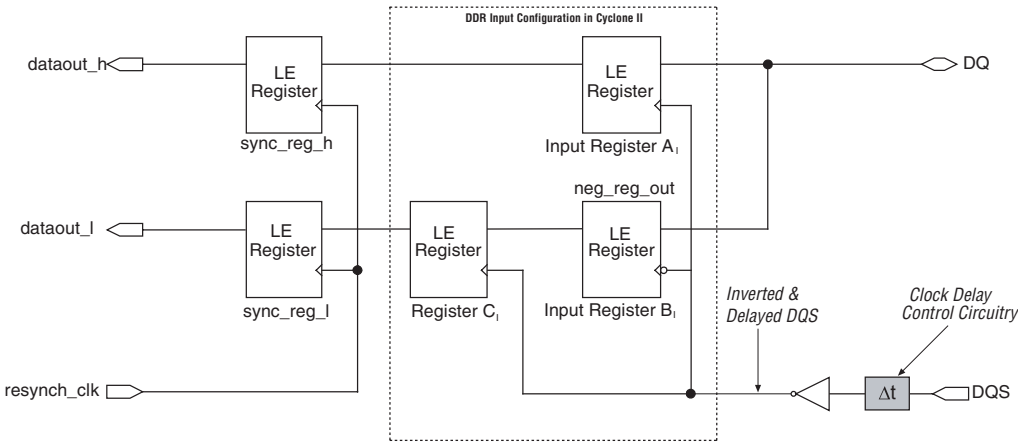
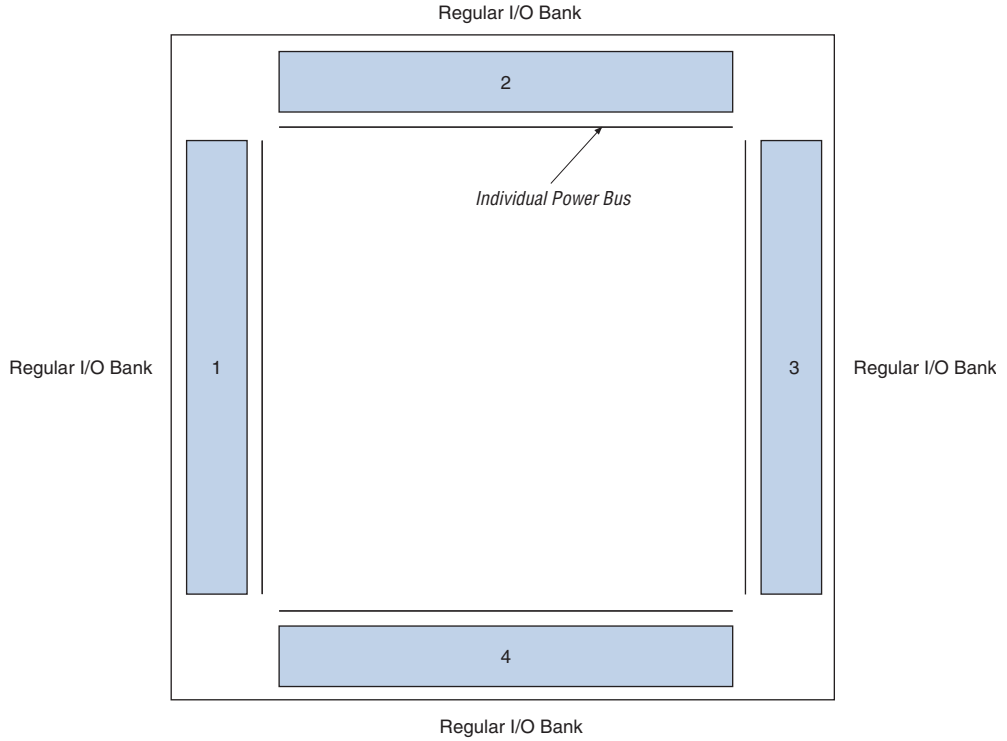


Figure 10–19. EP2C5 and EP2C8 Device I/O Banks *Notes (1), (2)*



Notes to Figure 10–19:

(1) This is a top view of the silicon die.

(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Table 11–5 defines the parameters of the timing diagram shown in Figure 11–16. Figure 11–17 shows the Cyclone II high-speed I/O timing budget.

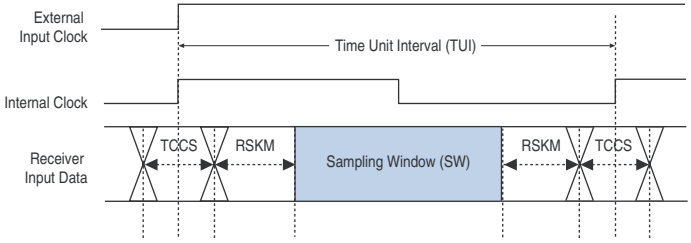
Table 11–5. High-Speed I/O Timing Definitions

Parameter	Symbol	Description
Transmitter channel-to-channel skew *(1)*	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window. $T_{SW} = T_{SU} + T_{hd}$ + PLL jitter.
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: RSKM = (TUI – SW – TCCS) / 2.
Input jitter tolerance (peak-to-peak)		Allowed input jitter on the input clock to the PLL that is tolerable while maintaining PLL lock.
Output jitter (peak-to-peak)		Peak-to-peak output jitter from the PLL.

Note to Table 11–5:

(1) The TCCS specification applies to the entire bank of LVDS as long as the SERDES logic are placed within the LAB adjacent to the output pins.

Figure 11–16. High-Speed I/O Timing Diagram



data A signal through a register and send the data B signal directly to the multiplier). The following control signals are available to each register within the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers within a single embedded multiplier are fed by the same clock, clock enable, or asynchronous clear signal.

Multiplier Stage

The multiplier stage supports 9 × 9 or 18 × 18 multipliers as well as other smaller multipliers in between these configurations. See "Operational Modes" on page 12–6 for details. Depending on the data width or operational mode of the multiplier, a single embedded multiplier can perform one or two multiplications in parallel.

Each multiplier operand can be a unique signed or unsigned number. Two signals, `signa` and `signb`, control whether a multiplier's input is a signed or unsigned value. If the `signa` signal is high, the data A operand is a signed number, and if the `signa` signal is low, the data A operand is an unsigned number. Table 12–3 shows the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

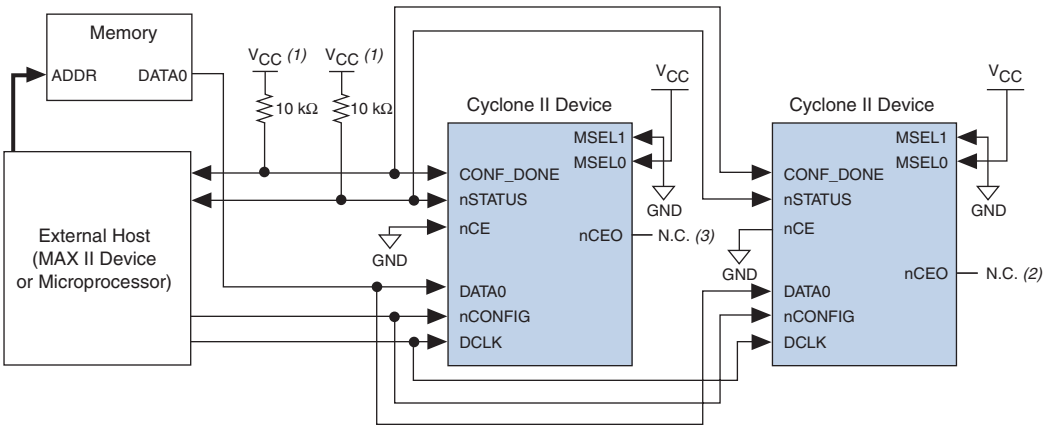
Table 12–3. Multiplier Sign Representation

Data A		Data B		Result
signa Value	Logic Level	signb Value	Logic Level	
Unsigned	Low	Unsigned	Low	Unsigned
Unsigned	Low	Signed	High	Signed
Signed	High	Unsigned	Low	Signed
Signed	High	Signed	High	Signed

There is only one `signa` and one `signb` signal for each embedded multiplier. The `signa` and `signb` signals can be changed dynamically to modify the sign representation of the input operands at run time. You can send the `signa` and `signb` signals through a dedicated input register. The multiplier offers full precision regardless of the sign representation.

If your system has multiple Cyclone II devices (in the same density and package) with the same configuration data, you can configure them in one configuration cycle by connecting all device's nCE pins to ground and connecting all the Cyclone II device's configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) together. You can also use the nCEO pin as a user I/O pin after configuration. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Make sure the DCLK and DATA lines are buffered for every fourth device. All devices start and complete configuration at the same time. Figure 13–11 shows multiple device PS configuration when both Cyclone II devices are receiving the same configuration data.

Figure 13–11. Multiple Device PS Configuration When Both FPGAs Receive the Same Data



Notes to Figure 13–11:

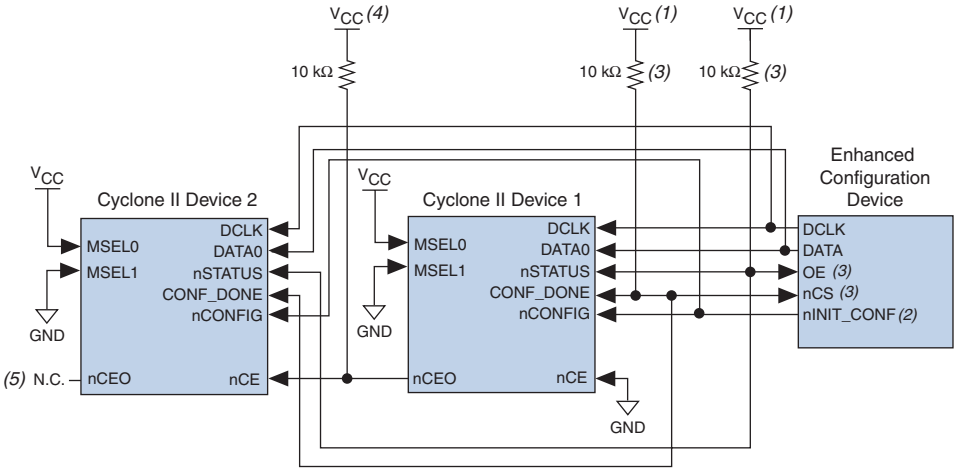
(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

(2) The nCEO pins of both devices can be left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

You can use a single configuration chain to configure Cyclone II devices with other Altera devices. Connect all the Cyclone II device's and all other Altera device's CONF_DONE and nSTATUS pins together so all devices in the chain complete configuration at the same time or that an error reported by one device initiates reconfiguration in all devices.

For more information on configuring multiple Altera devices in the same configuration chain, see *Configuring Mixed Altera FPGA Chains* in the *Configuration Handbook*.

Figure 13–14. Multiple Device PS Configuration Using an Enhanced Configuration Device



Notes to Figure 13–14:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(5) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

You cannot cascade enhanced configuration devices (EPC16, EPC8, and EPC4 devices).

When configuring multiple devices, you must generate the configuration device's POF from each project's SOF. You can combine multiple SOFs using the **Convert Programming Files** window in the Quartus II software.

For more information on how to create configuration files for multiple device configuration chains, see the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

When configuring multiple devices with the PS scheme, connect the first Cyclone II device's nCE pin to GND and connect its nCEO pin to the nCE pin of the Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's nCEO pin to the V_{CCIO} level when

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCEO	N/A if option is on. I/O if option is off.	All	Output	This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration. If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. Use the Quartus II software to make this pin a user I/O pin.
ASDO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data. In AS mode, ASDO has an internal pull-up that is always active.
nCSO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

Figure 15–1 shows a 144-pin TQFP package outline.

Figure 15–1. 144-Pin TQFP Package Outline