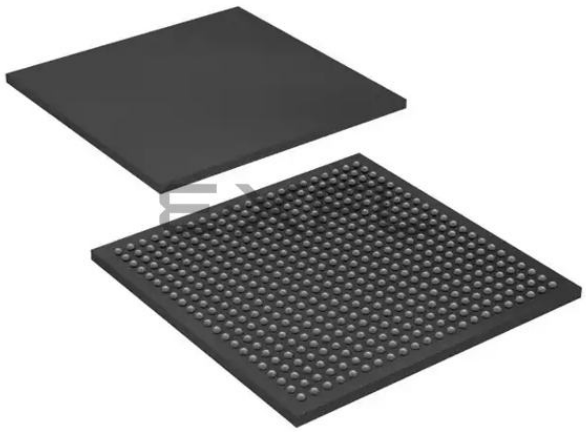

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	322
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35f484c8

Section I. Cyclone II Device Family Data Sheet

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. It contains the required PCB layout guidelines, device pin tables, and package specifications.

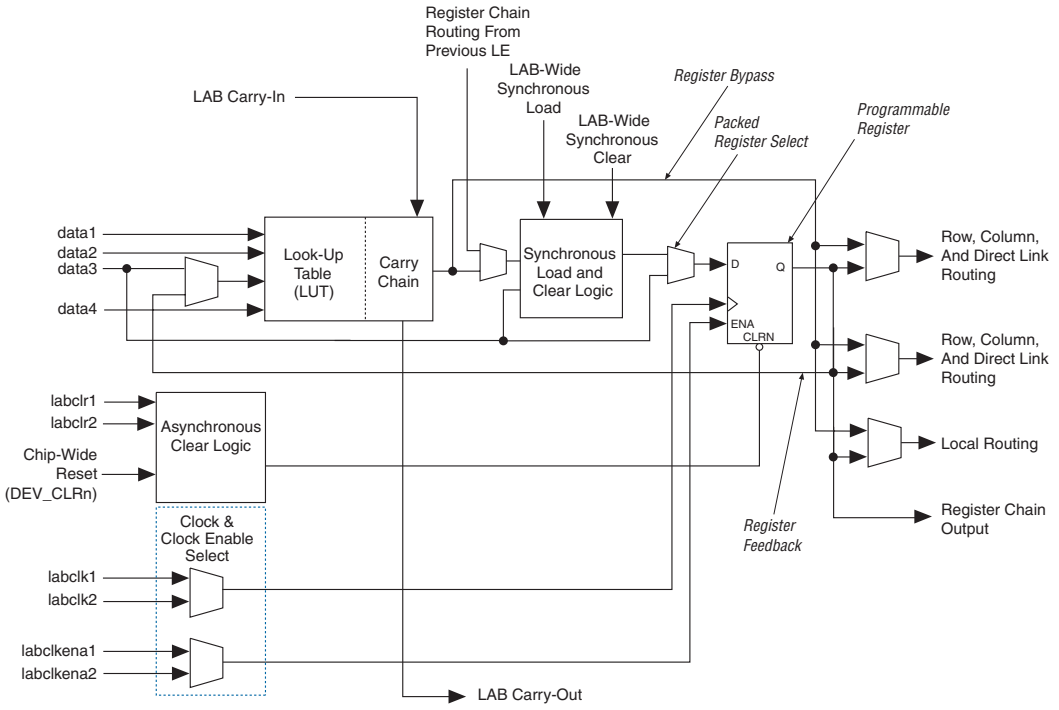
This section includes the following chapters:

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 2–2 shows a Cyclone II LE.

Figure 2–2. Cyclone II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, clock, clock enable, and clear inputs. Signals that use the global clock network, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources, allowing the LUT to drive one output while the register drives another output. This feature, register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. When using register packing, the LAB-wide synchronous load control signal is not available. See "LAB Control Signals" on page 2–8 for more information.

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 2 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.5V_HSTL_CLASS_I	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.5V_HSTL_CLASS_II	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.8V_HSTL_CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_HSTL_CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
DIFFERENTIAL_SSTL_2_ CLASS_I	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
DIFFERENTIAL_SSTL_2_ CLASS_II	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
DIFFERENTIAL_SSTL_18_ CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
DIFFERENTIAL_SSTL_18_ CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	589	617	1145	1176	1208	1208	ps
	t_{PCOUT}	375	393	683	731	780	780	ps
LVDS	t_{PI}	623	653	1072	1075	1078	1078	ps
	t_{PCOUT}	409	429	610	630	650	650	ps
1.2V_HSTL	t_{PI}	570	597	1263	1324	1385	1385	ps
	t_{PCOUT}	356	373	801	879	957	957	ps

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins *Notes (1), (2)* *(Part 2 of 2)*

Row I/O Output Standard	C6	C7	C8	Unit
Differential SSTL-2 Class I	60	90	90	ps
Differential SSTL-2 Class II	65	75	75	ps
Differential SSTL-18 Class I	90	165	165	ps
Differential HSTL-18 Class I	85	155	155	ps
Differential HSTL-15 Class I	145	145	205	ps
LVDS	60	60	60	ps
Simple RSDS	60	60	60	ps
Mini LVDS	60	60	60	ps
PCI	195	255	255	ps
PCI-X	195	255	255	ps

Notes to Table 5–55:
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Here is an example for calculating the DCD as a percentage for an SDR output on a row I/O on a –6 device:

If the SDR output I/O standard is SSTL-2 Class II, the maximum DCD is 65 ps (refer to Table 5–55). If the clock frequency is 167 MHz, the clock period T is:

$$T = 1/f = 1 / 167\ \text{MHz} = 6\ \text{ns} = 6000\ \text{ps}$$

To calculate the DCD as a percentage:

$(T/2 - DCD) / T = (6000\ \text{ps}/2 - 65\ \text{ps}) / 6000\ \text{ps} = 48.91\%$ (for low boundary)

$(T/2 + DCD) / T = (6000\ \text{ps}/2 + 65\ \text{ps}) / 6000\text{ps} = 51.08\%$ (for high boundary

Table 5–56. Maximum DCD for SDR Output on Column I/O *Notes (1), (2)* *(Part 1 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
LVCMOS	195	285	285	ps
LVTTL	210	305	305	ps

The actual half period is then = 3000 ps – 155 ps = 2845 ps

Table 5–58. Maximum DCD for DDIO Output on Column I/O Pins with PLL in the Clock Path *Notes (1), (2)*

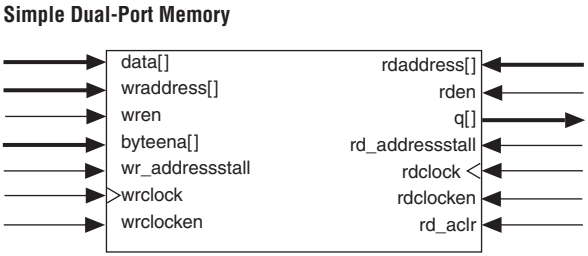
Column I/O Pins in the Clock Path	C6	C7	C8	Unit
LVCMOS	285	400	445	ps
LVTTL	305	405	460	ps
2.5-V	175	195	285	ps
1.8-V	190	205	260	ps
1.5-V	605	645	645	ps
SSTL-2 Class I	125	210	245	ps
SSTL-2 Class II	195	195	195	ps
SSTL-18 Class I	130	240	245	ps
SSTL-18 Class II	135	270	330	ps
HSTL-18 Class I	135	240	240	ps
HSTL-18 Class II	165	240	285	ps
HSTL-15 Class I	220	335	335	ps
HSTL-15 Class II	190	210	375	ps
Differential SSTL-2 Class I	125	210	245	ps
Differential SSTL-2 Class II	195	195	195	ps
Differential SSTL-18 Class I	130	240	245	ps
Differential SSTL-18 Class II	132	270	330	ps
Differential HSTL-18 Class I	135	240	240	ps
Differential HSTL-18 Class II	165	240	285	ps
Differential HSTL-15 Class I	220	335	335	ps
Differential HSTL-15 Class II	190	210	375	ps
LVDS	110	120	125	ps
Simple RSDS	125	125	275	ps
Mini-LVDS	110	120	125	ps

Notes to Table 5–58:

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

Figure 8–8. Cyclone II Simple Dual-Port Mode *Note (1)*



Note to Figure 8–8:
(1) Simple dual-port RAM supports input and output clock mode in addition to the read and write clock mode shown.

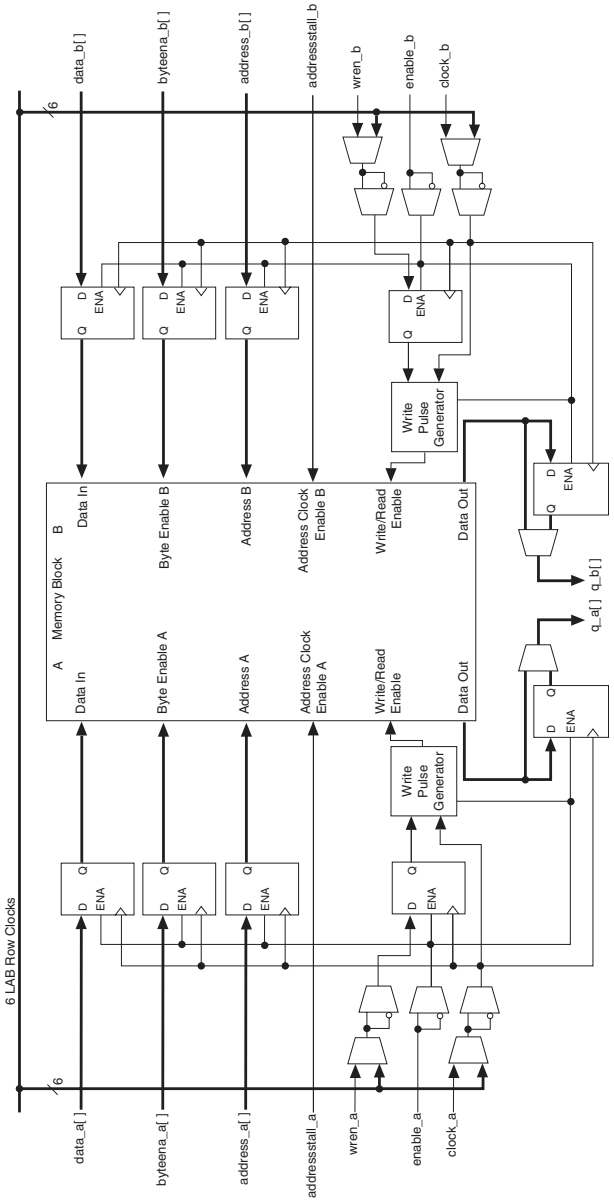
Cyclone II memory blocks support mixed-width configurations, allowing different read and write port widths. Tables 8–5 and 8–6 show the mixed-width configurations.

Table 8–5. Cyclone II Memory Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

In simple dual-port mode, the memory blocks have one write enable and one read enable signal. They do not support a clear port on the write enable and read enable registers. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is the old data stored at the memory

Figure 8–13. Cyclone II Memory Block in Independent Clock Mode *Note (1)*

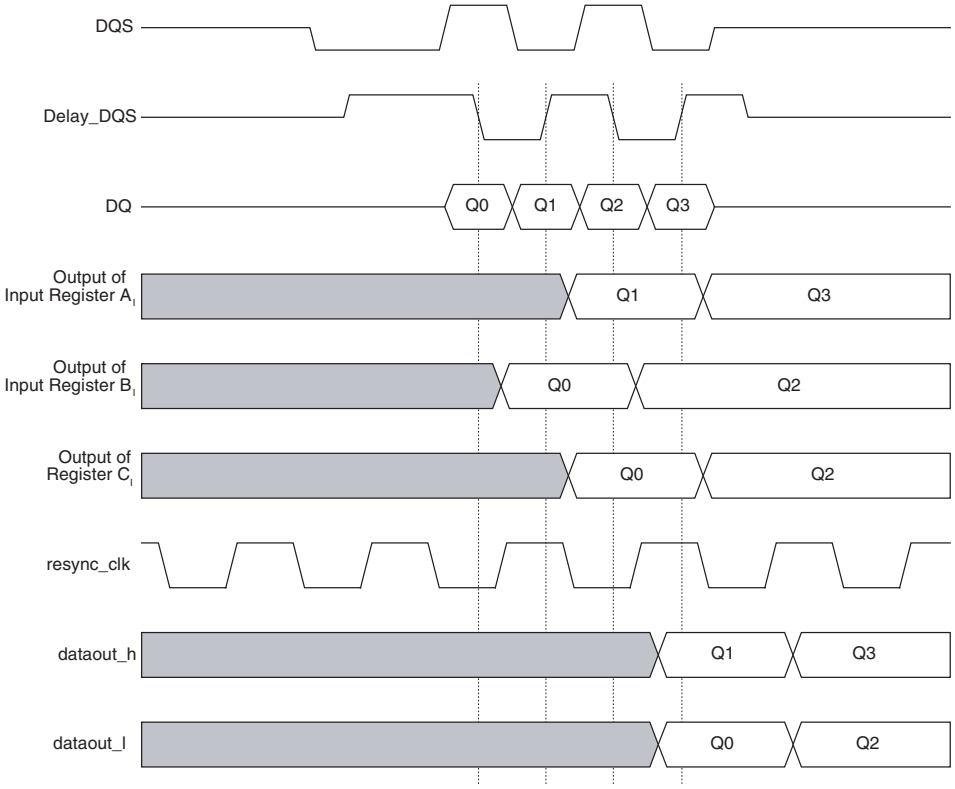


Note to Figure 8–13:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Registers sync_reg_h and sync_reg_l synchronize the two data streams to the rising edge of the resynchronization clock. Figure 9–12 shows examples of functional waveforms from a double data rate input implementation.

Figure 9–12. DDR Input Functional Waveforms



The Cyclone II DDR input registers require you to invert the incoming DQS signal to ensure proper data transfer. The altdq megafunction automatically adds the inverter on the clock port of the DQ signals. As shown in Figure 9–11, the inverted DQS signal's rising edge clocks register A_I, its falling edge clocks register B_I, and register C_I aligns the data clocked by register B_I with register A_I on the inverted DQS signal's rising edge. In a DDR memory read operation, the last data coincides with the falling edge of DQS signal. If you do not invert the DQS pin, you do not get this last data because the register does not latch until the next rising edge of the DQS signal.

3.3-V LVCMOS (EIA/JEDEC Standard JESD8-B)

The 3.3-V LVCMOS I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVCMOS standard defines the DC interface parameters for digital circuits operating from a 3.0- or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices.

The LVCMOS standard specifies the same input voltage requirements as LVTTL ($-0.3\ V \leq V_I \leq 3.9\ V$). The output buffer drives to the rail to meet the minimum high-level output voltage requirements. The 3.3-V I/O standard does not require input reference voltages or board terminations. Cyclone II devices support both input and output levels specified by the 3.3-V LVCMOS I/O standard.

3.3-V (PCI Special Interest Group [SIG] PCI Local Bus Specification Revision 3.0)

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 3.0 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires a 3.3-V V_{CCIO}. The 3.3-V PCI standard does not require input reference voltages or board terminations.

The side (left and right) I/O banks on all Cyclone II devices are fully compliant with the 3.3V PCI Local Bus Specification Revision 3.0 and meet 32-bit/66 MHz operating frequency and timing requirements.

Table 10–2 lists the specific Cyclone II devices that support 64- and 32-bit PCI at 66 MHz.

Table 10–2. Cyclone II 66-MHz PCI Support (Part 1 of 2)

Device	Package	–6 and –7 Speed Grades	
		64 Bits	32 Bits
EP2C5	144-pin TQFP		
	208-pin PQFP		✓
	256-pin FineLineBGA®		✓

Table 10–5 shows I/O standards supported when a pin is used as a regular I/O pin in the I/O banks of Cyclone II devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pads in relation to differential pads in the same I/O bank. Use the following guidelines for placing single-ended pads with respect to differential pads and for differential output pads placement in Cyclone II devices.

For the LVDS I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVDS I/O pad.
- Single-ended outputs can be no closer than five pads away from an LVDS I/O pad.
- Maximum of four 155-MHz (or greater) LVDS output channels per VCCIO and ground pair.
- Maximum of three 311-MHz (or greater) LVDS output channels per VCCIO and ground pair.

For optimal signal integrity at the LVDS input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVDS input pad.

The Quartus II software only checks the first two cases.

For the RSDS and mini-LVDS I/O standards:

- Single-ended inputs can be no closer than four pads away from an RSDS and mini-LVDS output pad.
- Single-ended outputs can be no closer than five pads away from an RSDS and mini-LVDS output pad.
- Maximum of three 85-MHz (or greater) RSDS and mini-LVDS output channels per VCCIO and ground pair.

The Quartus II software only checks the first two cases.

For the LVPECL I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVPECL input pad.
- Single-ended outputs can be no closer than five pads away from an LVPECL input pad.

For optimal signal integrity at the LVPECL input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVPECL input pad.

You can use I/O pins and internal logic to implement a high-speed I/O receiver and transmitter in Cyclone II devices. Cyclone II devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal global phase-locked loops (PLLs), and I/O cells are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

I/O Standards Support

This section provides information on the I/O standards that Cyclone II devices support.

LVDS Standard Support in Cyclone II Devices

The LVDS I/O standard is a high-speed, low-voltage swing, low power, and general purpose I/O interface standard. The Cyclone II device meets the ANSI/TIA/EIA-644 standard.

I/O banks on all four sides of the Cyclone II device support LVDS channels. See the pin tables on the Altera web site for the number of LVDS channels supported throughout different family members. Cyclone II LVDS receivers (input) support a data rate of up to 805 Mbps while LVDS transmitters (output) support up to 640 Mbps. The maximum internal clock frequency for a receiver and for a transmitter is 402.5 MHz. The maximum input data rate of 805 Mbps and the maximum output data rate of 640 Mbps is only achieved when DDIO registers are used. The LVDS standard does not require an input reference voltage; however, it does require a 100-Ω termination resistor between the two signals at the input buffer.

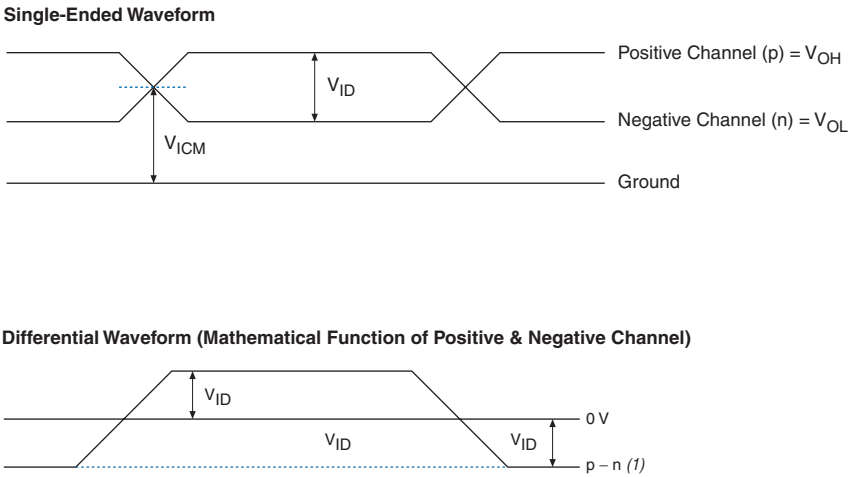
For LVDS data rates in Cyclone II devices with different speed grades, see the *DC Characteristics & Timing Specifications* chapter of the *Cyclone II Device Handbook*.

Table 11–1 shows LVDS I/O specifications.

Table 11–1. LVDS I/O Specifications (Part 1 of 2) *Note (1)*

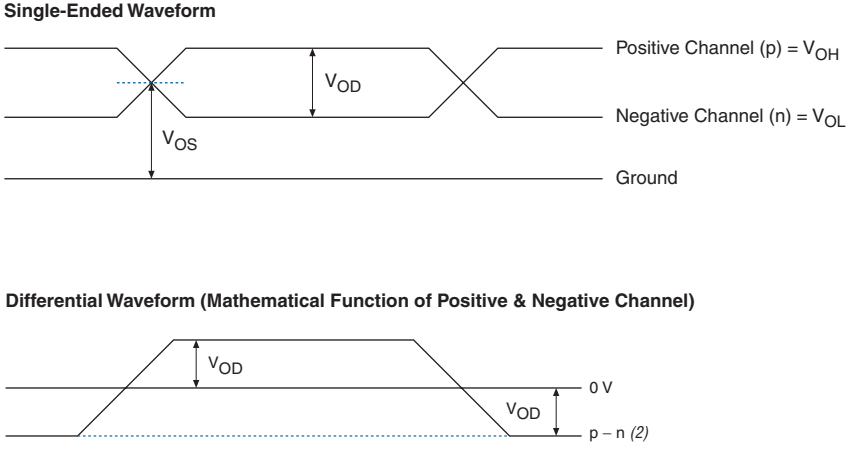
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCINT}	Supply voltage		1.15	1.2	1.25	V
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		600	mV
ΔV_{OD}	Change in V_{OD} between H and L	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V

Figure 11–4. Receiver Input Waveforms for the LVDS Differential I/O Standard



Note to Figure 11–4:
(1) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 11–5. Transmitter Output Waveform for the LVDS Differential I/O Standard *Note (2)*



Notes to Figure 11–5:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Reset Stage

When nCONFIG or nSTATUS are low, the device is in reset. After POR, the Cyclone II device releases nSTATUS. An external 10-kΩ pull-up resistor pulls the nSTATUS signal high, and the Cyclone II device enters configuration mode.

V_{CCINT} and V_{CCIO} of the banks where the configuration and JTAG pins reside need to be fully powered to the appropriate voltage levels in order to begin the configuration process.

Configuration Stage

The serial clock (DCLK) generated by the Cyclone II device controls the entire configuration cycle and provides the timing for the serial interface. Cyclone II devices use an internal oscillator to generate DCLK. Using the MSEL[] pins, you can select either a 20- or 40-MHz oscillator. Although you can select either 20- or 40-MHz oscillator when designing with serial configuration devices, the 40-MHz oscillator provides faster configuration times. There is some variation in the internal oscillator frequency because of the process, temperature, and voltage conditions in Cyclone II devices. The internal oscillator is designed such that its maximum frequency is guaranteed to meet EPCS device specifications.

Table 13–5 shows the AS DCLK output frequencies.

Table 13–5. AS DCLK Output Frequency *Note (1)*

Oscillator Selected	Minimum	Typical	Maximum	Units
40 MHz	20	26	40	MHz
20 MHz	10	13	20	MHz

Note to Table 13–5:
(1) These values are preliminary.

In both AS and Fast AS configuration schemes, the serial configuration device latches input and control signals on the rising edge of DCLK and drives out configuration data on the falling edge. Cyclone II devices drive out control signals on the falling edge of DCLK and latch configuration data on the falling edge of DCLK.

In configuration mode, the Cyclone II device enables the serial configuration device by driving its nCSO output pin low, which connects to the chip select (nCS) pin of the configuration device. The Cyclone II device uses the serial clock (DCLK) and serial data output (ASDO) pins to send operation commands and/or read address signals to the serial

it feeds the next device's nCE pin. After the first device in the chain completes configuration, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration. The nCEO pin is a dual-purpose pin in Cyclone II devices.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the device is in a chain, and the nCEO pin is connected to the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O pin after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

Connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Buffer the DCLK and DATA lines for every fourth device.

When configuring multiple devices, configuration does not begin until all devices release their OE or nSTATUS pins. Similarly, since all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

You should not pull CONF_DONE low to delay initialization. Instead, use the Quartus II software's **User-Supplied Start-Up Clock** option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain initialize together since their CONF_DONE pins are tied together.

Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if there is an error when configuring the first Cyclone II device, it resets the chain by pulling its nSTATUS pin low. This low signal drives the OE pin low on the enhanced configuration device and drives nSTATUS low on all FPGAs, which causes them to enter a reset state.

If the **Auto-restart configuration after error** option is turned on, the devices automatically initiate reconfiguration if an error occurs. The FPGAs release their nSTATUS pins after a reset time-out period (40 µs maximum). When all the nSTATUS pins are released and pulled high, the configuration device reconfigures the chain. If the **Auto-restart configuration after error** option is turned off, a microprocessor or controller must monitor the nSTATUS pin for errors and then pulse

In addition, because the nSTATUS pins are connected, all the Cyclone II devices in the chain stop configuration if any device detects an error. If this happens, you must manually restart configuration in the Quartus II software.

Figure 13–20 shows how to configure multiple Cyclone II devices with a download cable.

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCEO	N/A if option is on. I/O if option is off.	All	Output	This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration. If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. Use the Quartus II software to make this pin a user I/O pin.
ASDO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data. In AS mode, ASDO has an internal pull-up that is always active.
nCSO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

Document Revision History

Table 13–14 shows the revision history for this document.

Table 13–14. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	• Added document revision history. • Added *Note (1)* to Table 13–1. • Added *Note (1)* to Table 13–4. • Updated Figure 13–3. • Updated Figures 13–6 and 13–7. • Updated *Note (2)* to Figure 13–13. • Updated "Single Device PS Configuration Using a Configuration Device" section. • Updated *Note (2)* to Figure 13–14. • Updated *Note (2)* to Figure 13–15. • Updated *Note (2)* to Figure 13–16. • Updated *Note (2)* to Figure 13–17. • Updated *Note (4)* to Figure 13–21. • Updated *Note (2)* to Figure 13–25.	• Changed unit 'kw' to 'kΩ' in Figures 13–6 and 13–7. • Added note about serial configuration devices supporting 20 MHz and 40 MHz DCLK. • Added infomation about the need for a resistor on nCONFIG if reconfiguration is required. • Added information about MSEL[1..0] internal pull-down resistor value.
July 2005 v2.0	• Updated "Configuration Stage" section. • Updated "PS Configuration Using a Download Cable" section. • Updated Figures 13–8, 13–12, and 13–18.	—
November 2004 v1.1	• Updated "Configuration Stage" section in "Single Device AS Configuration" section. • Updated "Initialization Stage" section in "Single Device AS Configuration" section. • Updated Figure 13–8. • Updated "Initialization Stage" section in "Single Device PS Configuration Using a MAX II Device as an External Host" section. • Updated Table 13–7. • Updated "Single Device PS Configuration Using a Configuration Device" section. • Updated "Initialization Stage" section in "Single Device PS Configuration Using a Configuration Device" section. • Updated Figure 13–18. • Updated "Single Device JTAG Configuration" section.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Table 14–2 describes the capture and update register capabilities of all types of boundary-scan cells within Cyclone II devices.

Table 14–2. Cyclone II Device Boundary Scan Cell Descriptions *Note (1)*

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Dedicated clock input	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to clock network or logic array
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to control logic
Dedicated bidirectional (open drain) *(4)*	0	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to configuration control
Dedicated bidirectional *(5)*	OUTJ	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	OUTJ drives to output buffer

Notes to Table 14–2:

(1) TDI, TDO, TMS, TCK, all V_{CC} and GND pin types do not have BSCs.
(2) N.C.: no connect.
(3) This includes nCONFIG, MSEL0, MSEL1, DATA0, and nCE pins and DCLK (when not used in Active Serial mode).
(4) This includes CONF_DONE and nSTATUS pins.
(5) This includes DCLK (when not used in Active Serial mode).

IEEE Std. 1149.1 BST Operation Control

Cyclone II devices implement the following IEEE Std. 1149.1 BST instructions: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE, USERCODE, CLAMP, and HIGHZ. The BST instruction length is 10 bits. These instructions are described later in this chapter.

For summaries of the BST instructions and their instruction codes, see the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

The IEEE Std. 1149.1 test access port (TAP) controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 14–5 shows the TAP controller state machine.