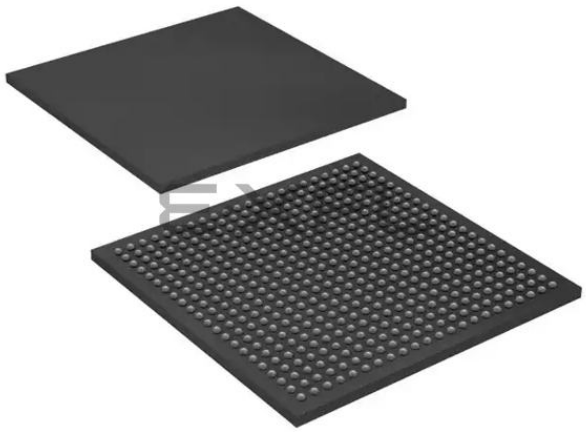

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	322
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35f484c8n

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes

Clock Mode	Description
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`.
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

Table 2–9. Cyclone II M4K Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Table 2–20. Cyclone II MultiVolt I/O Support (Part 2 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
3.3			✓ *(4)*	✓	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓

Notes to Table 2–20:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on **Allow voltage overdrive for LVTTL/LVCMOS input pins** option in Device setting option in the Quartus II software.

(3) When V_{CCIO} = 1.8-V, a Cyclone II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(4) When V_{CCIO} = 3.3-V and a 2.5-V input signal feeds an input pin or when V_{CCIO} = 1.8-V and a 1.5-V input signal feeds an input pin, the V_{CCIO} supply current will be slightly larger than expected. The reason for this increase is that the input signal level does not drive to the V_{CCIO} rail, which causes the input buffer to not completely shut off.

(5) When V_{CCIO} = 2.5-V, a Cyclone II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(6) When V_{CCIO} = 3.3-V, a Cyclone II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Table 5–19. M4K Block Internal Timing Microparameters (Part 3 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Notes to Table 5–19:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Cyclone II Clock Timing Parameters

Refer to Tables 5–20 through 5–34 for Cyclone II clock timing parameters.

Table 5–20. Cyclone II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2C5/A Clock Timing Parameters

Tables 5–21 and 5–22 show the clock timing parameters for EP2C5/A devices.

Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.283	1.343	2.329	2.484	2.688	2.688	ns
t_{COUT}	1.297	1.358	2.363	2.516	2.717	2.717	ns
t_{PLLCIN}	–0.188	–0.201	0.076	0.038	0.042	0.052	ns

I/O Delays

Refer to Tables 5–39 through 5–43 for I/O delays.

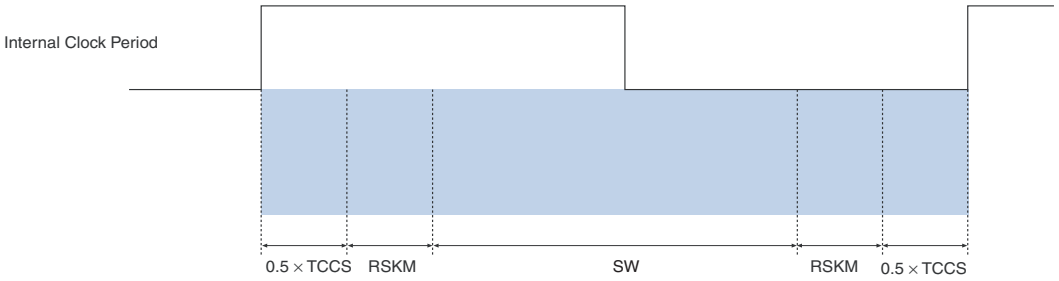
Table 5–39. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 1 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
LVTTL	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
2.5V	t_{PI}	624	654	1192	1238	1283	1283	ps
	t_{PCOUT}	410	430	730	793	855	855	ps
1.8V	t_{PI}	725	760	1372	1428	1484	1484	ps
	t_{PCOUT}	511	536	910	983	1056	1056	ps
1.5V	t_{PI}	790	828	1439	1497	1556	1556	ps
	t_{PCOUT}	576	604	977	1052	1128	1128	ps
LVCMOS	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
SSTL_2_CLASS_I	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_2_CLASS_II	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_18_CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
SSTL_18_CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps

Figure 5–4. High-Speed I/O Timing Budget *Note (1)*



Note to Figure 5–4:
(1) The equation for the high-speed I/O timing budget is: period = TCCS + RSKM + SW + RSKM.

Table 5–48 shows the RSDS timing budget for Cyclone II devices at 311 Mbps. RSDS is supported for transmitting from Cyclone II devices. Cyclone II devices cannot receive RSDS data because the devices are intended for applications where they will be driving display drivers. Cyclone II devices support a maximum RSDS data rate of 311 Mbps using DDIO registers. Cyclone II devices support RSDS only in the commercial temperature range.

Table 5–48. RSDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max (1)	Min	Typ	Max (1)	Min	Typ	Max (1)	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×8	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×7	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×4	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×2	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×1	10	—	311	10	—	311	10	—	311	MHz
Device operation in Mbps	×10	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	311	20	—	311	20	—	311	Mbps
	×1	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%

Figure 5–5. RSDS Transmitter Clock to Data Relationship

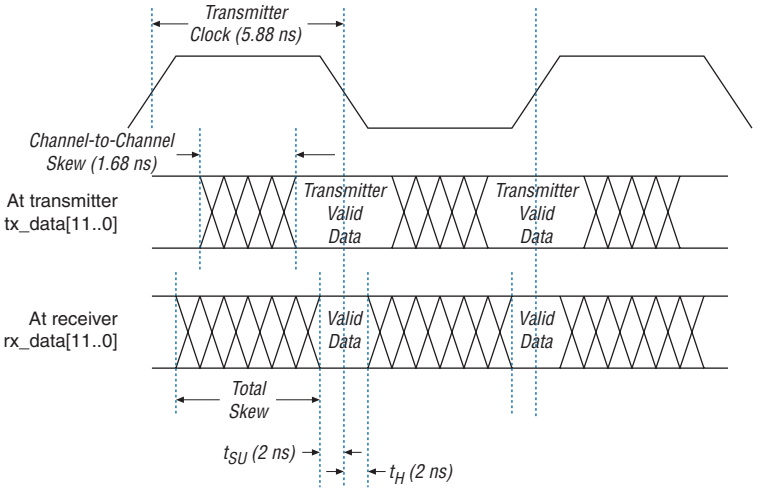


Table 5–49 shows the mini-LVDS transmitter timing budget for Cyclone II devices at 311 Mbps. Cyclone II devices cannot receive mini-LVDS data because the devices are intended for applications where they will be driving display drivers. A maximum mini-LVDS data rate of 311 Mbps is supported for Cyclone II devices using DDIO registers. Cyclone II devices support mini-LVDS only in the commercial temperature range.

Table 5–49. Mini-LVDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×8	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×7	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×4	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×2	10	—	155.5	10	—	155.5	10	—	155.5	MHz
	×1	10	—	311	10	—	311	10	—	311	MHz

Section II. Clock Management

This section provides information on the phase-locked loops (PLLs). Cyclone® II PLLs offer general-purpose clock management with multiplication and phase shifting and also have the ability to drive off chip to control system-level clock networks. This section contains detailed information on the features, the interconnections to the logic array and off chip, and the specifications for Cyclone II PLLs.

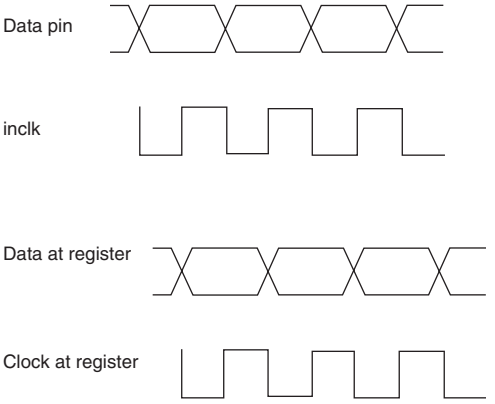
This section includes the following chapter:

- Chapter 7, PLLs in Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 7–7. Phase Relationship between Cyclone II PLL Clocks in Source-Synchronous Compensation Mode



Set the input pin to the register delay chain within the IOE to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL.

Hardware Features

Cyclone II device PLLs support a number of features for general-purpose clock management. This section discusses clock multiplication and division implementation, phase-shifting implementation and PLL lock circuits.

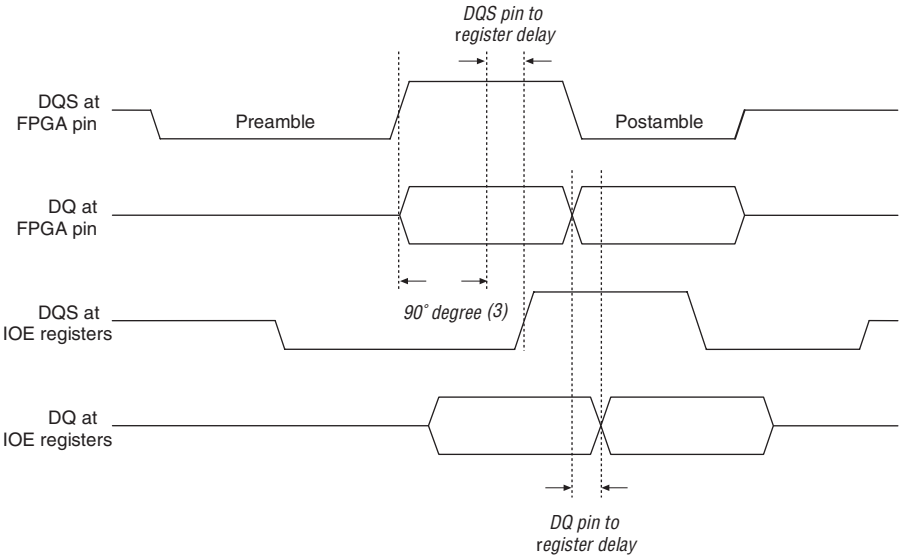
Clock Multiplication & Division

Cyclone II device PLLs provide clock synthesis for PLL output ports using $m/(n \times \text{post-scale})$ scaling factors. Every PLL has one pre-scale divider, n, with a range of 1 to 4 and one multiply counter, m, with a range of 1 to 32. The input clock, f_{IN}, is divided by a pre-scale counter, n, to produce the input reference clock, f_{REF}, to the PFD. This input reference clock, f_{REF}, is then multiplied by the m feedback factor. The control loop drives the VCO frequency to match $f_{IN} \times (m/n)$. The equations for these frequencies are:

$$f_{REF} = \frac{f_{IN}}{n}$$

$$f_{VCO} = f_{REF} \times m = f_{IN} \frac{m}{n}$$

Figure 9–1. Example of a 90° Shift on the DQS Signal *Notes (1), (2)*



Notes to Figure 9–1:
(1) RLDRAM II and QDRII SRAM memory interfaces do not have preamble and postamble specifications.
(2) DDR2 SDRAM does not support a burst length of two.
(3) The phase shift required for your system should be based on your timing analysis and may not be 90°.

During write operations to a DDR or DDR2 SDRAM device, the FPGA must send the data strobe to the memory device center-aligned relative to the data. Cyclone II devices use a PLL to center-align the data strobe by generating a 0° phase-shifted system clock for the write data strobes and a –90° phase-shifted write clock for the write data pins for the DDR and DDR2 SDRAM. Figure 9–2 shows an example of the relationship between the data and data strobe during a burst-of-two write.

Figure 9–2. DQ & DQS Relationship During a DDR & DDR2 SDRAM Write

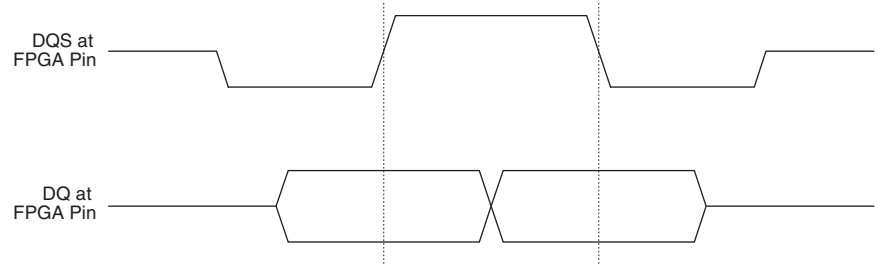
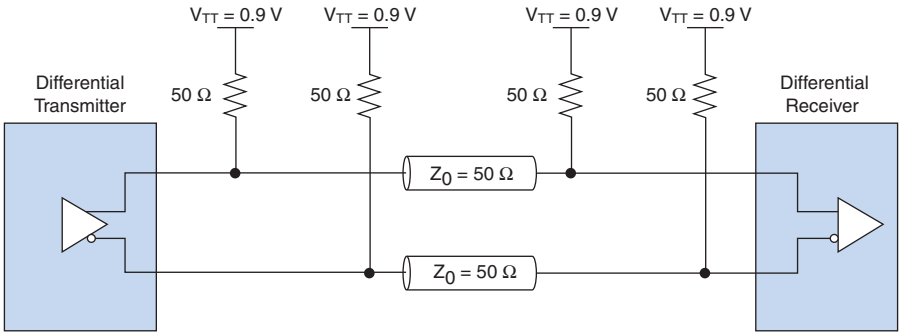


Figure 10–12. 1.8-V Differential HSTL Class II Termination



1.5-V LVCMOS (EIA/JEDEC Standard JESD8-11)

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices.

The 1.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.5-V LVCMOS.

1.5-V HSTL Class I and II

The 1.5-V HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic nominal switching range. This standard defines single-ended input and output specifications for all HSTL-compliant digital integrated circuits. The 1.5-V HSTL I/O standard in Cyclone II devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE, APEX 20KC, Stratix® II, Stratix GX, Stratix, and in Cyclone II devices themselves because the input and output voltage thresholds are compatible. Refer to Figures 10–13 and 10–14. Cyclone II devices support both input and output levels with V_{REF} and V_{TT}.

V_{REF} Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply and to prevent output switching noise from shifting the V_{REF} rail, there are restrictions on the placement of single-ended voltage referenced I/Os with respect to V_{REF} pads and VCCIO and ground pairs. Use the following guidelines for placing single-ended pads in Cyclone II devices.

The Quartus II software automatically does all the calculations in this section.

Input Pads

Each V_{REF} pad supports up to 15 input pads on each side of the V_{REF} pad for FineLine BGA devices. Each V_{REF} pad supports up to 10 input pads on each side of the V_{REF} pad for quad flat pack (QFP) devices. This is irrespective of VCCIO and ground pairs, and is guaranteed by the Cyclone II architecture.

Output Pads

When a voltage referenced input or bidirectional pad does not exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each VCCIO and ground pair supports 9 output pins for Fineline BGA packages (not more than 9 output pins per 12 consecutive row I/O pins) or 5 output pins for QFP packages (not more than 5 output pins per 12 consecutive row I/O pins or 8 consecutive column I/O pins). Any non-SSTL and non-HSTL output can be no closer than two pads away from a V_{REF} pad. Altera recommends that any SSTL or HSTL output, except for pintable defined DQ and DQS outputs, to be no closer than two pads away from a V_{REF} pad to maintain acceptable noise levels.

Quartus II software will not check for the SSTL and HSTL output pads placement rule.

Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

Bidirectional Pads

Bidirectional pads must satisfy input and output guidelines simultaneously.

Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

November 2005 v2.1	• Updated Tables 10–2 and 10–3. • Added PCI Express information. • Updated Table 10–6.	—
July 2005 v2.0	Updated Table 10–1.	—
November 2004 v1.1	Updated Table 10–7.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

The **Enable user-supplied start-up clock (CLKUSR)** option can be turned on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data has been accepted and CONF_DONE goes high, Cyclone II devices require 299 clock cycles to initialize properly and support a CLKUSR f_{MAX} of 100 MHz.

If the optional CLKUSR pin is being used and nCONFIG is pulled low to restart configuration during device initialization, you need to ensure that CLKUSR continues toggling during the time nSTATUS is low (maximum of 40 µs).

An optional INIT_DONE pin signals the end of initialization and the start of user mode with a low-to-high transition. By default, the INIT_DONE output is disabled. You can enable the INIT_DONE output by turning on the **Enable INIT_DONE output** option in the Quartus II software. If you use the INIT_DONE pin, an external 10-kΩ pull-up resistor pulls the pin high when nCONFIG is low and during the beginning of configuration. Once the optional bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin transitions low. When initialization is complete, the INIT_DONE pin is released and pulled high. The MAX II device must be able to detect this low-to-high transition, which signals the FPGA has entered user mode.

If you want to use the INIT_DONE pin as a user I/O pin, you should wait for the maximum value of t_{CD2UM} (see Table 13–7) after the CONF_DONE signal transitions high so to ensure the Cyclone II device has been initialized properly and is in user mode.

Make sure the MAX II device does not drive the CONF_DONE signal low during configuration, initialization, and before the device enters user mode.

User Mode

When initialization is complete, the Cyclone II device enters user mode. In user mode, the user I/O pins no longer have pull-up resistors and function as assigned in your design.

To ensure DCLK and DATA0 are not left floating at the end of configuration, the MAX II device must drive them either high or low, which ever is convenient on your PCB. The Cyclone II device DATA0 pin is not available as a user I/O pin after configuration.

When the FPGA is in user mode, you can initiate a reconfiguration by transitioning the nCONFIG pin low-to-high. The nCONFIG pin must be low for at least 2 µs. When the nCONFIG transitions low, the Cyclone II

Table 13–7 defines the timing parameters for Cyclone II devices for PS configuration.

Table 13–7. PS Timing Parameters for Cyclone II Devices

Symbol	Parameter	Minimum	Maximum	Units
t_{POR}	POR delay *(1)*	100		ms
t_{CF2CD}	nCONFIG low to CONF_DONE low		800	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low		800	ns
t_{CFG}	nCONFIG low pulse width	2		µs
t_{STATUS}	nSTATUS low pulse width	10	40 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high		40 *(2)*	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	40		µs
t_{ST2CK}	nSTATUS high to first rising edge on DCLK	1		µs
t_{DSU}	Data setup time before rising edge on DCLK	7		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CH}	DCLK high time	4		ns
t_{CL}	DCLK low time	4		ns
t_{CLK}	DCLK period	10		ns
f_{MAX}	DCLK frequency		100	MHz
t_{CD2UM}	CONF_DONE high to user mode *(3)*	18	40	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period		
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (299 × CLKUSR period)		

Notes to Table 13–7:

(1) The POR delay minimum of 100 ms only applies for non "A" devices.

(2) This value is applicable if users do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting the device.

Device configuration options and how to create configuration files are discussed further in the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

PS Configuration Using a Microprocessor

In the PS configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone II device.

it feeds the next device's nCE pin. After the first device in the chain completes configuration, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration. The nCEO pin is a dual-purpose pin in Cyclone II devices.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the device is in a chain, and the nCEO pin is connected to the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O pin after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

Connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Buffer the DCLK and DATA lines for every fourth device.

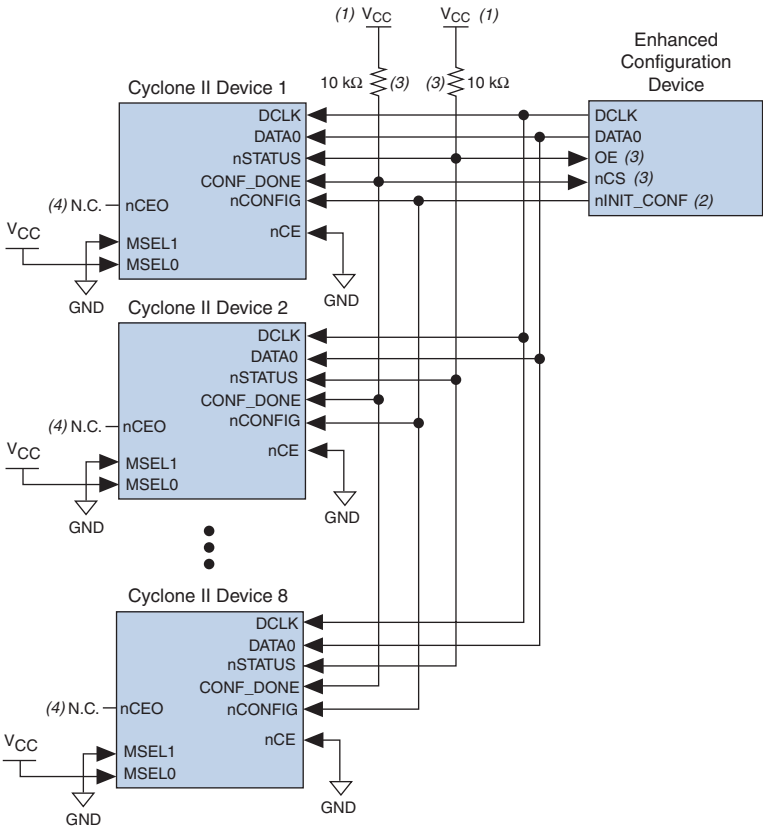
When configuring multiple devices, configuration does not begin until all devices release their OE or nSTATUS pins. Similarly, since all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

You should not pull CONF_DONE low to delay initialization. Instead, use the Quartus II software's **User-Supplied Start-Up Clock** option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain initialize together since their CONF_DONE pins are tied together.

Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if there is an error when configuring the first Cyclone II device, it resets the chain by pulling its nSTATUS pin low. This low signal drives the OE pin low on the enhanced configuration device and drives nSTATUS low on all FPGAs, which causes them to enter a reset state.

If the **Auto-restart configuration after error** option is turned on, the devices automatically initiate reconfiguration if an error occurs. The FPGAs release their nSTATUS pins after a reset time-out period (40 µs maximum). When all the nSTATUS pins are released and pulled high, the configuration device reconfigures the chain. If the **Auto-restart configuration after error** option is turned off, a microprocessor or controller must monitor the nSTATUS pin for errors and then pulse

Figure 13–16. Multiple Device PS Configuration Using an Enhanced Configuration Device When FPGAs Receive the Same Data



Notes to Figure 13–16:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

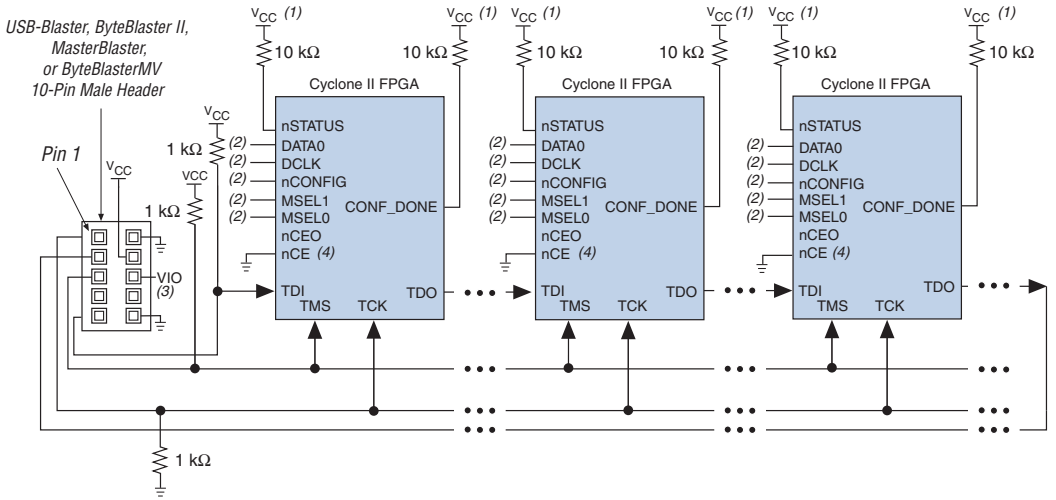
(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

You can cascade several EPC2 or EPC1 devices to configure multiple Cyclone II devices. The first configuration device in the chain is the master configuration device, and the subsequent devices are the slave devices. The master configuration device sends DCLK to the Cyclone II

Figure 13–24. JTAG Configuration of Multiple Devices Using a Download Cable



Notes to Figure 13–24:

(1) The pull-up resistor should be connected to the same supply voltage as the USB-Blaster, MasterBlaster (VIO pin), ByteBlaster II or ByteBlasterMV cable.

(2) Connect the nCONFIG and MSEL[1..0] pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the nCONFIG pin to V_{CC}, and the MSEL[1..0] pins to ground. In addition, pull DCLK and DATA0 to either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cable, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) nCE must be connected to ground or driven low for successful JTAG configuration.

Connect the nCE pin to GND or pull it low during JTAG configuration. In multiple device AS and PS configuration chains, connect the first device's nCE pin to GND and connect its nCEO pin to the nCE pin of the next device in the chain or you can use it as a user I/O pin after configuration.

After the first device completes configuration in a multiple device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, you should make sure the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multiple device configuration chain, the nCEO pin of the previous device drives the nCE pin of the next device low when it has successfully been JTAG configured.

14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

CII51014-2.1

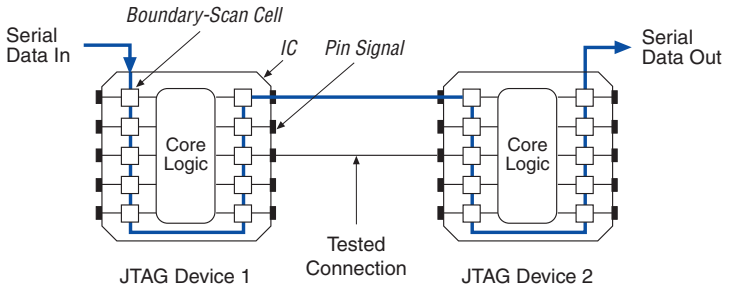
Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (e.g., external test probes and "bed-of-nails" test fixtures) harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

This BST architecture tests pin connections without using physical test probes and captures functional data while a device is operating normally. Boundary-scan cells in a device force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared with expected results. Figure 14–1 shows the concept of boundary-scan testing.

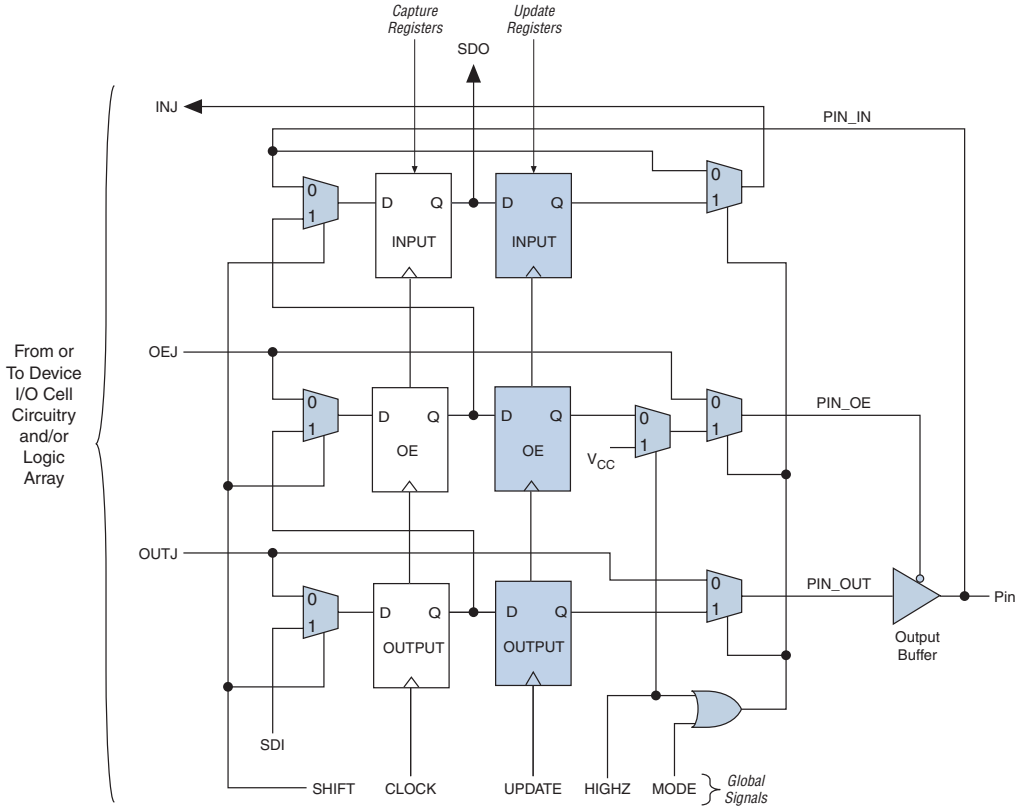
Figure 14–1. IEEE Std. 1149.1 Boundary-Scan Testing



to external device data via the PIN_IN signal, while the update registers connect to external data through the PIN_OUT and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 14–4 shows the Cyclone II device's user I/O boundary-scan cell.

Figure 14–4. Cyclone II Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry



484-Pin FineLine BGA, Option 3 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 15–13 and 15–14 show the package information and package outline figure references, respectively, for the 484-pin FineLine BGA package.

Table 15–13. 484-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAJ-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	5.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–14. 484-Pin FineLine BGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	23.00 BSC		
E	23.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		