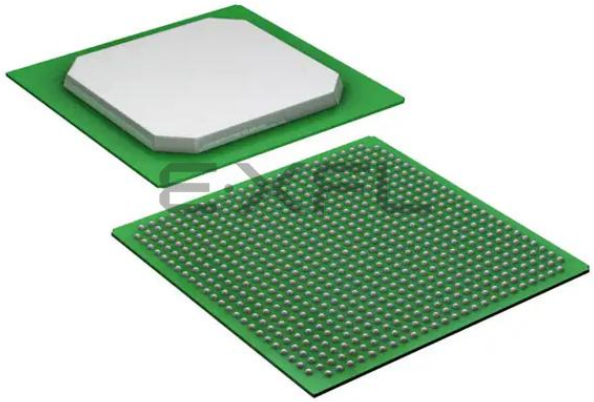

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

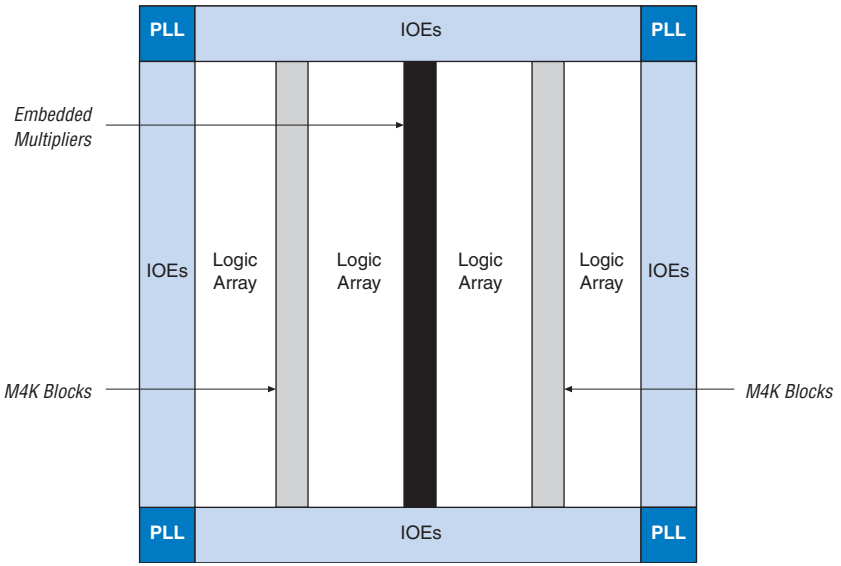
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	475
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35f672c6n

phase-align double data rate (DDR) signals) provide interface support for external memory devices such as DDR, DDR2, and single data rate (SDR) SDRAM, and QDRII SRAM devices at up to 167 MHz.

Figure 2–1 shows a diagram of the Cyclone II EP2C20 device.

Figure 2–1. Cyclone II EP2C20 Device Block Diagram



The number of M4K memory blocks, embedded multiplier blocks, PLLs, rows, and columns vary per device.

Logic Elements

The smallest unit of logic in the Cyclone II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE features:

- A four-input look-up table (LUT), which is a function generator that can implement any function of four variables
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and direct link interconnects
- Support for register packing
- Support for register feedback

Dedicated Clock Pins

Larger Cyclone II devices (EP2C15 and larger devices) have 16 dedicated clock pins (CLK[15..0], four pins on each side of the device). Smaller Cyclone II devices (EP2C5 and EP2C8 devices) have eight dedicated clock pins (CLK[7..0], four pins on left and right sides of the device). These CLK pins drive the global clock network (GCLK), as shown in Figures 2–11 and 2–12.

If the dedicated clock pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the logic array using the MultiTrack interconnect. However, if they are used as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Dual-Purpose Clock Pins

Cyclone II devices have either 20 dual-purpose clock pins, DPCLK[19..0] or 8 dual-purpose clock pins, DPCLK[7..0]. In the larger Cyclone II devices (EP2C15 devices and higher), there are 20 DPCLK pins; four on the left and right sides and six on the top and bottom of the device. The corner CDPCLK pins are first multiplexed before they drive into the clock control block. Since the signals pass through a multiplexer before feeding the clock control block, these signals incur more delay to the clock control block than other DPCLK pins that directly feed the clock control block. In the smaller Cyclone II devices (EP2C5 and EP2C8 devices), there are eight DPCLK pins; two on each side of the device (see Figures 2–11 and 2–12).

A programmable delay chain is available from the DPCLK pin to its fan-out destinations. To set the propagation delay from the DPCLK pin to its fan-out destinations, use the **Input Delay from Dual-Purpose Clock Pin to Fan-Out Destinations** assignment in the Quartus II software.

These dual-purpose pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables, or protocol control signals such as TRDY and IRDY for PCI, or DQS signals for external memory interfaces.

If you cannot meet the maximum V_{CC} ramp time requirement, you must use an external component to hold nCONFIG low until the power supplies have reached their minimum recommend operating levels. Otherwise, the device may not properly configure and enter user mode.

Conclusion

Cyclone II devices are hot socketable and support all power-up and power-down sequences with the one requirement that V_{CCIO} and V_{CCINT} be powered up and down within 100 ms of each other to keep the I/O pins from driving out. Cyclone II devices do not require any external devices for hot socketing and power sequencing.

Document Revision History

Table 4–1 shows the revision history for this document.

Table 4–1. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	• Added document revision history. • Updated "I/O Pins Remain Tri-Stated during Power-Up" section. • Updated "Power-On Reset Circuitry" section. • Added footnote to Figure 4–3.	• Specified V_{CCIO} and V_{CCINT} supplies must be GND when "not powered". • Added clarification about input-tristate behavior. • Added infomation on V_{CC} monotonic ramp.
July 2005 v2.0	Updated technical content throughout.	
February 2005 v1.1	Removed ESD section.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.174	–0.186	0.11	0.07	0.071	0.081	ns

Notes to Table 5–21:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–22. EP2C5/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.212	1.267	2.210	2.351	2.54	2.540	ns
t_{COUT}	1.214	1.269	2.226	2.364	2.548	2.548	ns
t_{PLLCIN}	–0.259	–0.277	–0.043	–0.095	–0.106	–0.096	ns
$t_{PLLCOUT}$	–0.257	–0.275	–0.027	–0.082	–0.098	–0.088	ns

Notes to Table 5–22:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C8/A Clock Timing Parameters

Tables 5–23 and 5–24 show the clock timing parameters for EP2C8/A devices.

Table 5–23. EP2C8/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.339	1.404	2.405	2.565	2.764	2.774	ns
t_{COUT}	1.353	1.419	2.439	2.597	2.793	2.803	ns
t_{PLLCIN}	–0.193	–0.204	0.055	0.015	0.016	0.026	ns

The loop filter converts these up and down signals to a voltage that is used to bias the VCO. If the charge pump receives a logic high on the up signal, current is driven into the loop filter. If the charge pump receives a logic high on the down signal, current is drawn from the loop filter. The loop filter filters out glitches from the charge pump and prevents voltage over-shoot, which minimizes the jitter on the VCO.

The voltage from the charge pump determines how fast the VCO operates. The VCO is implemented as an four-stage differential ring oscillator. A divide counter, *m*, is inserted in the feedback loop to increase the VCO frequency above the input reference frequency, making the VCO frequency $f_{VCO} = m \times f_{REF}$. Therefore, the feedback clock, f_{FB}, applied to one input of the PFD, is locked to the input reference clock, f_{REF} (f_{IN}/n), applied to the other input of the PFD.

The VCO output can feed up to three post-scale counters (c0, c1, and c2). These post-scale counters allow a number of harmonically related frequencies to be produced by the PLL.

Additionally, Cyclone II PLLs have internal delay elements to compensate for routing on the global clock networks and I/O buffers. These internal delays are fixed and not accessible to the user.

Figure 7–2 shows a simplified block diagram of the major components of a Cyclone II device PLL.

Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 2 of 2)

I/O Standard	Input	Output	
	inclk	lock	pll_out
SSTL-25 class II	✓	✓	✓
RSDS/mini-LVDS *(4)*		✓	✓

Notes to Table 7–6:
(1) The PCI-X I/O standard is supported only on side I/O pins.
(2) Differential SSTL and HSTL outputs are only supported on the PLL<#>_OUT pins.
(3) These I/O standards are only supported on top and bottom I/O pins.
(4) The RSDS and mini-LVDS pins are only supported on output pins.

Clock Feedback Modes

Cyclone II PLLs support four clock feedback modes: normal mode, zero delay buffer mode, no compensation mode, and source synchronous mode. Cyclone II PLLs do not have support for external feedback mode. All the supported clock feedback modes allow for multiplication and division, phase shifting, and programmable duty cycle. The phase relationships shown in the waveforms in Figures 7–4 through 7–6 are for the default (zero degree) phase shift setting. Changing the phase-shift setting changes the relationships between the output clocks from the PLL.

Normal Mode

In normal mode, the PLL phase-aligns the input reference clock with the clock signal at the ports of the registers in the logic array I/O registers to compensate for the internal global clock network delay. Use the `altpll` megafunction in the Quartus II software to define which internal clock output from the PLL (c0, c1, or c2) to compensate for.

If an external clock output pin (PLL<#>_OUT) is used in this mode, there is a phase shift with respect to the clock input pin. Similarly, if the internal PLL clock outputs are used to drive general-purpose I/O pins, there is be phase shift with respect to the clock input pin.

Figure 7–4 shows an example waveform of the PLL clocks' phase relationship in this mode.

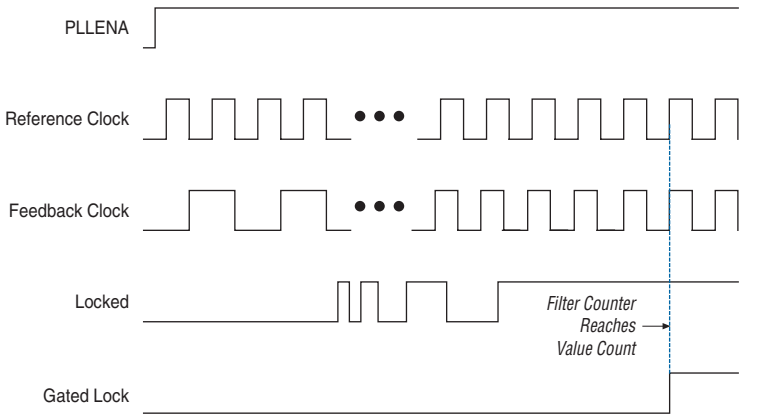
locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals



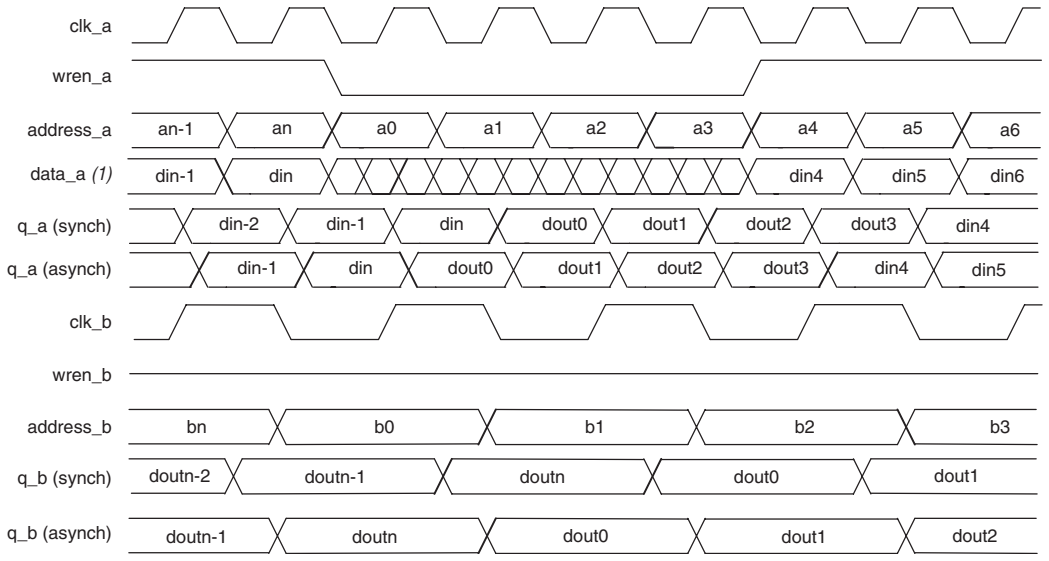
outputs, respectively. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle on which it was written. See "Read-During- Write Operation at the Same Address" on page 8–28 for waveforms and information on mixed-port read-during-write mode.

Potential write contentions must be resolved external to the RAM because writing to the same address location at both ports results in unknown data storage at that location.

For the maximum synchronous write cycle time, refer to the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Figure 8–11 shows true dual-port timing waveforms for the write operation at port A and the read operation at port B.

Figure 8–11. Cyclone II True Dual-Port Timing Waveforms

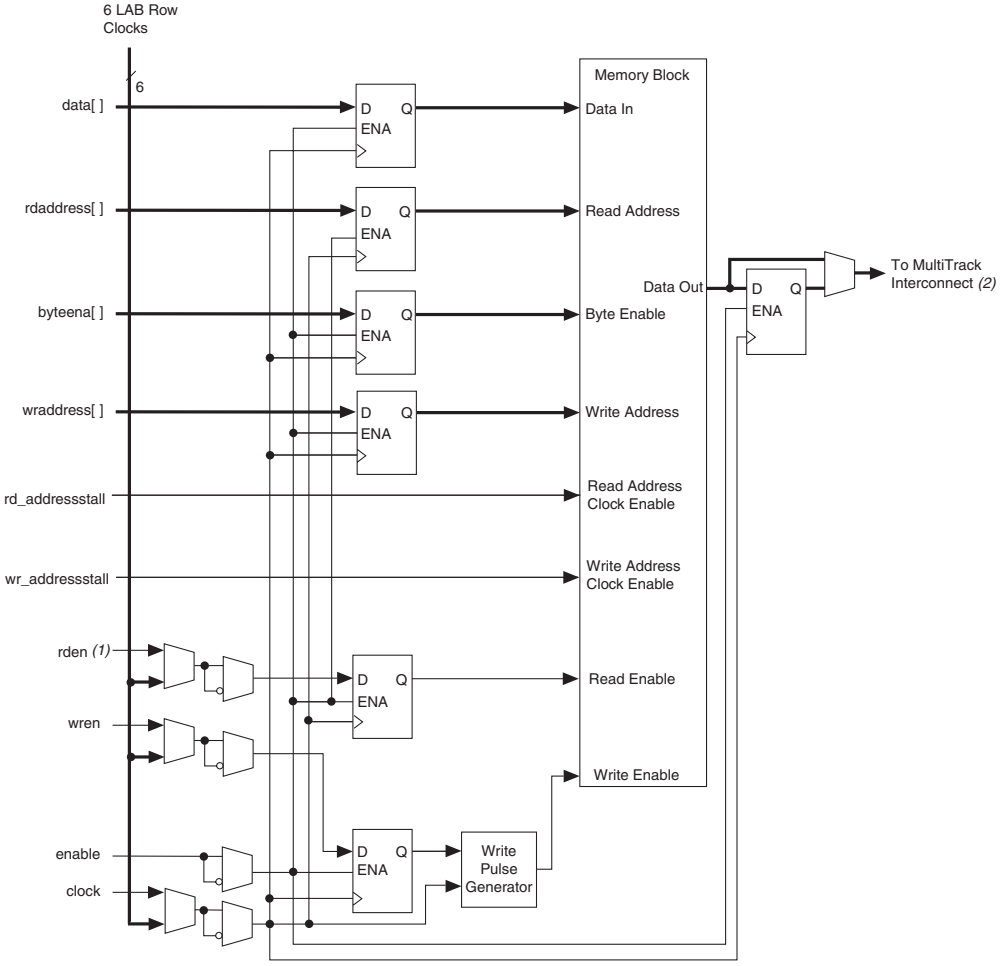


Note to Figure 8–11:
(1) The crosses in the `data_a` waveform during write indicate "don't care."

Shift Register Mode

Cyclone II memory blocks can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto-correlation and cross-correlation functions. These and other DSP

Figure 8–19. Cyclone II Single-Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*

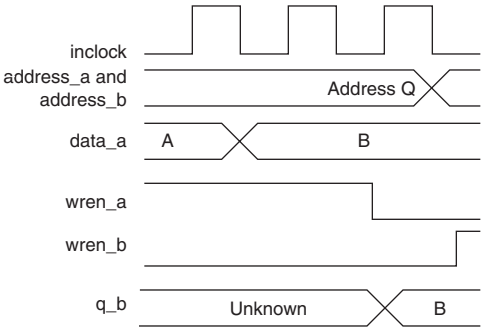


Notes to Figure 8–19:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

Figure 8–24. Cyclone II Mixed-Port Read-During-Write: Don't Care Mode *Note (1)*



Note to Figure 8–24:
(1) Outputs are not registered.

Mixed-port read-during-write is not supported when two different clocks are used in a dual-port RAM. The output value is unknown during a mixed-port read-during-write operation.

Conclusion

The M4K memory structure of Cyclone II devices provides a flexible memory architecture with high memory bandwidth. It addresses the needs of different memory applications in FPGA designs with features such as different memory modes, byte enables, parity bit storage, address clock enables, mixed clock mode, shift register mode, mixed-port width support, and true dual-port mode.

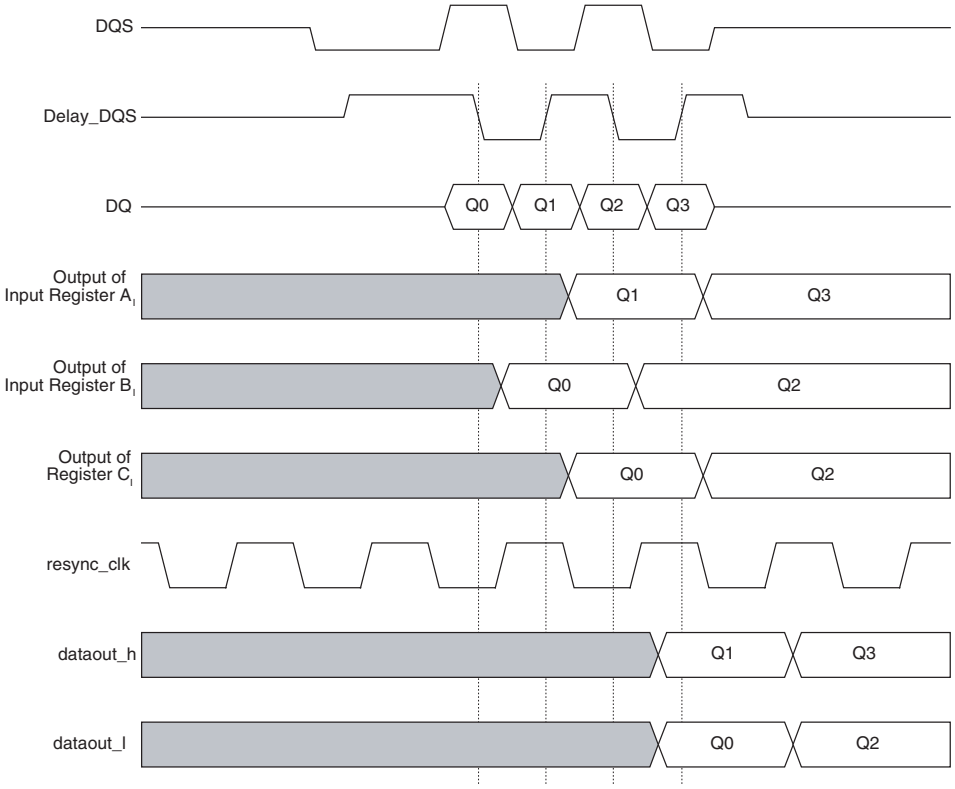
Referenced Documents

This chapter references the following documents:

- *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*
- *Single- and Dual-Clock FIFO Megafunction User Guide*
- *Using Parity to Detect Errors White Paper*

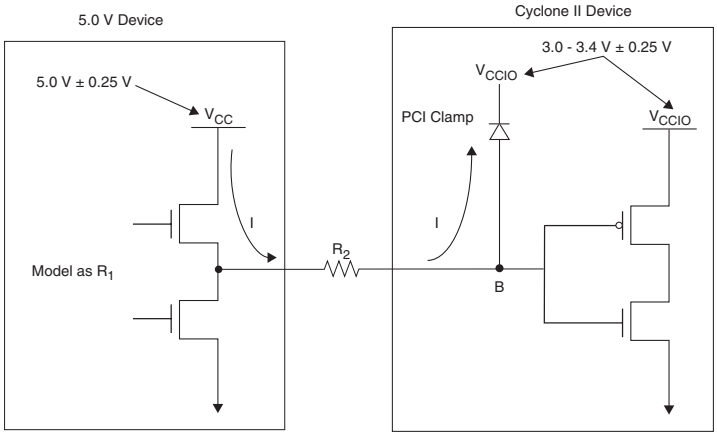
Registers sync_reg_h and sync_reg_l synchronize the two data streams to the rising edge of the resynchronization clock. Figure 9–12 shows examples of functional waveforms from a double data rate input implementation.

Figure 9–12. DDR Input Functional Waveforms



The Cyclone II DDR input registers require you to invert the incoming DQS signal to ensure proper data transfer. The altdq megafunction automatically adds the inverter on the clock port of the DQ signals. As shown in Figure 9–11, the inverted DQS signal's rising edge clocks register A_I, its falling edge clocks register B_I, and register C_I aligns the data clocked by register B_I with register A_I on the inverted DQS signal's rising edge. In a DDR memory read operation, the last data coincides with the falling edge of DQS signal. If you do not invert the DQS pin, you do not get this last data because the register does not latch until the next rising edge of the DQS signal.

Figure 10–21. Driving a Cyclone II Device with a 5.0-Volt Device



If V_{CCIO} is between 3.0 V and 3.6 V and the PCI clamping diode is enabled, the voltage at point B in Figure 10–21 is 4.3 V or less. To limit large current draw from the 5.0-V device, R_2 should be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (I_{OH}) specifications of the devices driving the trace. The PCI clamping diode in the Cyclone II device can support 25 mA of current.

To compute the required value of R_2, first calculate the model of the pull-up transistors on the 5.0-V device. This output resistor (R_1) can be modeled by dividing the 5.0-V device supply voltage (V_{CC}) by the I_{OH}: $R_1 = V_{CC}/I_{OH}$.

Figure 10–22 shows an example of typical output drive characteristics of a 5.0-V device.

12. Embedded Multipliers in Cyclone II Devices

CII51012-1.2

Introduction

Use Cyclone® II FPGAs alone or as digital signal processing (DSP) co-processors to improve price-to-performance ratios for DSP applications. You can implement high-performance yet low-cost DSP systems with the following Cyclone II device features and design support:

- Up to 150 18 x 18 multipliers
- Up to 1.1 Mbit of on-chip embedded memory
- High-speed interface to external memory
- DSP Intellectual Property (IP) cores
- DSP Builder interface to the Mathworks Simulink and Matlab design environment
- DSP Development Kit, Cyclone II Edition

This chapter focuses on the Cyclone II embedded multiplier blocks.

Cyclone II devices have embedded multiplier blocks optimized for multiplier-intensive low-cost DSP applications. These embedded multipliers combined with the flexibility of programmable logic devices (PLDs), provide you with the ability to efficiently implement various cost sensitive DSP functions easily. Consumer-based application systems such as digital television (DTV) and home entertainment systems typically require a cost effective solution for implementing multipliers to perform signal processing functions like finite impulse response (FIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

Along with the embedded multipliers, the M4K memory blocks in Cyclone II devices also support various soft multiplier implementations. These, in combination with the embedded multipliers increase the available number of multipliers in Cyclone II devices and provide the user with a wide variety of implementation options and flexibility when designing their systems.

See the Cyclone II Device Family Data Sheet section in Volume 1 of the ***Cyclone II Device Handbook*** for more information on Cyclone II devices.

Section VI. Configuration & Test

This section provides configuration information for all of the supported configuration schemes for Cyclone® II devices. These configuration schemes use either a microprocessor, configuration device, or download cable. There is detailed information on how to design with Altera® configuration devices. The last chapter provides information on JTAG support in Cyclone II devices.

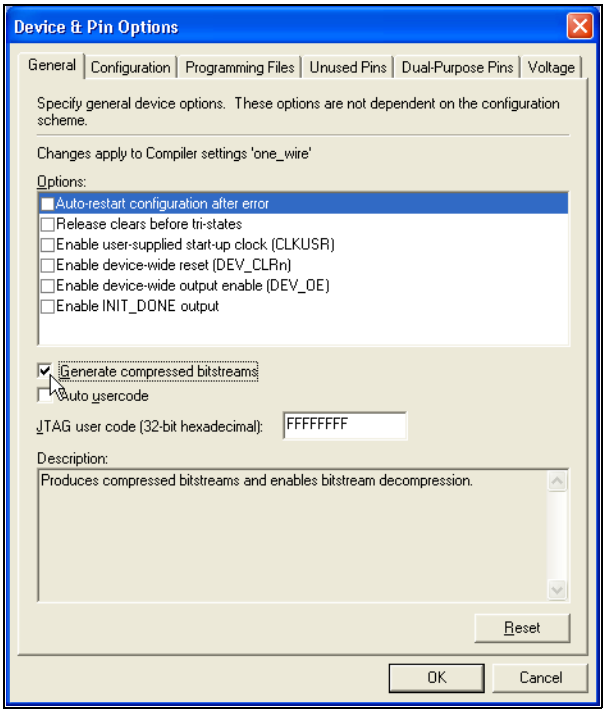
This section includes the following chapters:

- Chapter 13, Configuring Cyclone II Devices
- Chapter 14, IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 13–1. Enabling Compression for Cyclone II Bitstreams in Compiler Settings



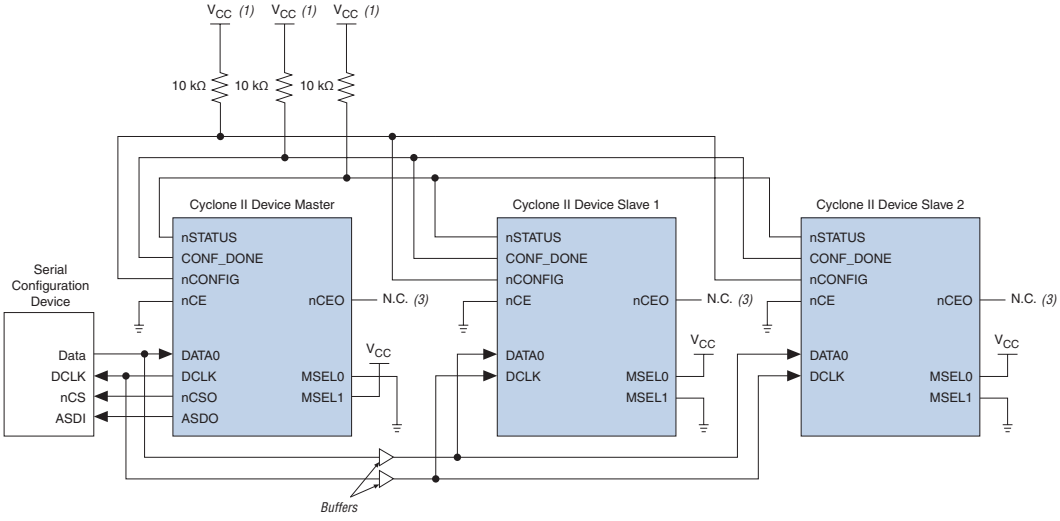
You can also use the following steps to enable compression when creating programming files from the Convert Programming Files window.

1. Click **Convert Programming Files** (File menu).
2. Select the Programming File type. Only Programmer Object Files (**.pof**), SRAM HEXOUT, RBF, or TTF files support compression.
3. For POFs, select a configuration device.
4. Select **Add File** and add a Cyclone II SRAM Object File(s) (**.sof**).
5. Select the name of the file you added to the SOF Data area and click on **Properties**.
6. Check the **Compression** check box.

Single SOF

The second method configures both the master and slave Cyclone II devices with the same SOF. The serial configuration device stores one copy of the SOF file. This setup is shown in Figure 13–6 where the master is setup in AS mode, and the slave devices are setup in PS mode (MSEL=01). You could setup one or more slave devices in the chain and all the slave devices are setup in the same way as shown in Figure 13–6.

Figure 13–6. Multiple Device AS Configuration When FPGAs Receive the Same Data with a Single SOF



Notes to Figure 13–6:

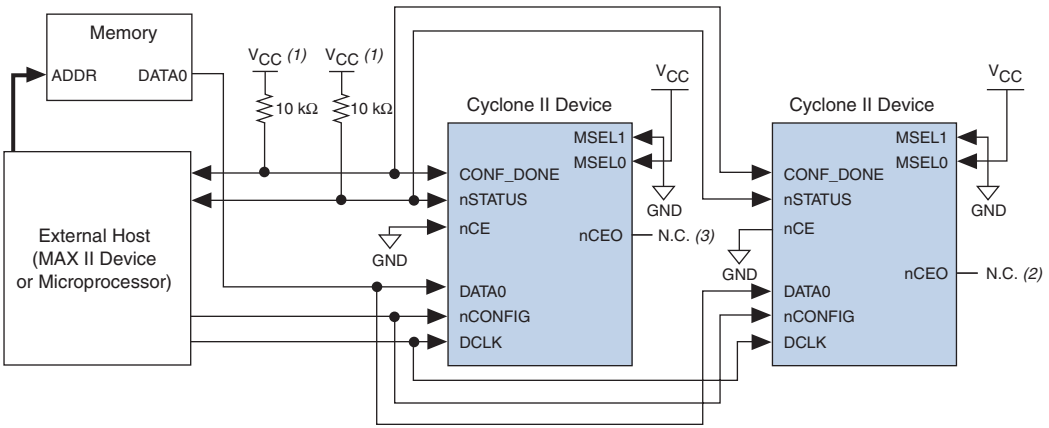
(1) Connect the pull-up resistors to a 3.3-V supply.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

In this setup, all the Cyclone II devices in the chain are connected for concurrent configuration. This can reduce the AS configuration time because all the Cyclone II devices are configured in one configuration cycle. Connect the nCE input pins of all the Cyclone II devices to ground. You can either leave the nCEO output pins on all the Cyclone II devices unconnected or use the nCEO output pins as normal user I/O pins. The DATA and DCLK pins are connected in parallel to all the Cyclone II devices.

If your system has multiple Cyclone II devices (in the same density and package) with the same configuration data, you can configure them in one configuration cycle by connecting all device's nCE pins to ground and connecting all the Cyclone II device's configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) together. You can also use the nCEO pin as a user I/O pin after configuration. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Make sure the DCLK and DATA lines are buffered for every fourth device. All devices start and complete configuration at the same time. Figure 13–11 shows multiple device PS configuration when both Cyclone II devices are receiving the same configuration data.

Figure 13–11. Multiple Device PS Configuration When Both FPGAs Receive the Same Data



Notes to Figure 13–11:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

(2) The nCEO pins of both devices can be left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

You can use a single configuration chain to configure Cyclone II devices with other Altera devices. Connect all the Cyclone II device's and all other Altera device's CONF_DONE and nSTATUS pins together so all devices in the chain complete configuration at the same time or that an error reported by one device initiates reconfiguration in all devices.

For more information on configuring multiple Altera devices in the same configuration chain, see *Configuring Mixed Altera FPGA Chains* in the *Configuration Handbook*.

When designing a Cyclone II board for JTAG configuration, use the guidelines in Table 13–10 for the placement of the dedicated configuration pins.

Table 13–10. Dedicated Configuration Pin Connections During JTAG Configuration

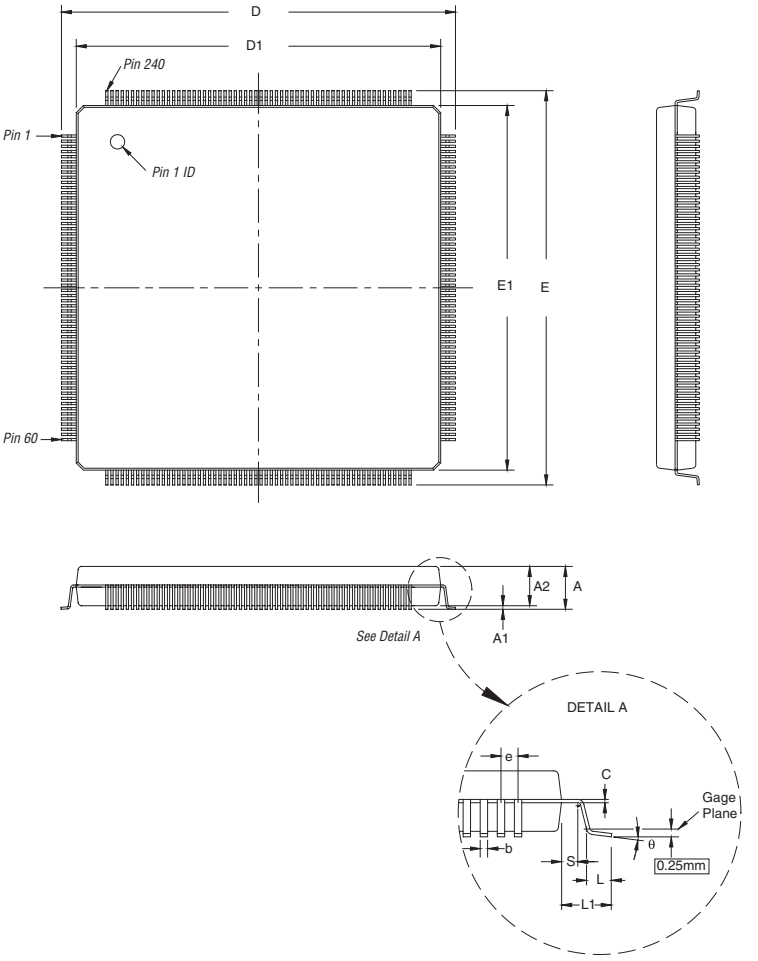
Signal	Description
nCE	On all Cyclone II devices in the chain, nCE should be driven low by connecting it to ground, pulling it low via a resistor, or driving it by some control circuitry. For devices that are also in multiple device AS, or PS configuration chains, the nCE pins should be connected to GND during JTAG configuration or JTAG configured in the same order as the configuration chain.
nCEO	On all Cyclone II devices in the chain, nCEO can be used as a user I/O or connected to the nCE of the next device. If nCEO is connected to the nCE of the next device, the nCEO pin must be pulled high to V_{CCIO} by an external 10-kΩ pull-up resistor to help the internal weak pull-up resistor. If the nCEO pin is not connected to the nCE pin of the next device, you can use it as a user I/O pin after configuration.
MSEL	These pins must not be left floating. These pins support whichever non-JTAG configuration is used in production. If only JTAG configuration is used, you should tie these pins to ground.
nCONFIG	Driven high by connecting to V_{CC}, pulling up via a resistor, or driven high by some control circuitry.
nSTATUS	Pull to V_{CC} via a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each nSTATUS pin should be pulled up to V_{CC} individually. nSTATUS pulling low in the middle of JTAG configuration indicates that an error has occurred.
CONF_DONE	Pull to V_{CC} via a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each CONF_DONE pin should be pulled up to V_{CC} individually. CONF_DONE going high at the end of JTAG configuration indicates successful configuration.
DCLK	Should not be left floating. Drive low or high, whichever is more convenient on your board.

Figure 13–23 shows JTAG configuration of a Cyclone II device with a microprocessor.

Table 15–10. 240-Pin PQFP Package Outline Dimensions (Part 2 of 2)			
Symbol	Millimeter		
	Min.	Nom.	Max.
e	0.50 BSC		
θ	0°	3.5°	8°

Figure 15–3 shows a 240-pin PQFP package outline.

Figure 15–3. 240-pin PQFP Package Outline



484-Pin FineLine BGA, Option 3 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 15–13 and 15–14 show the package information and package outline figure references, respectively, for the 484-pin FineLine BGA package.

Table 15–13. 484-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAJ-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	5.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–14. 484-Pin FineLine BGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	23.00 BSC		
E	23.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		