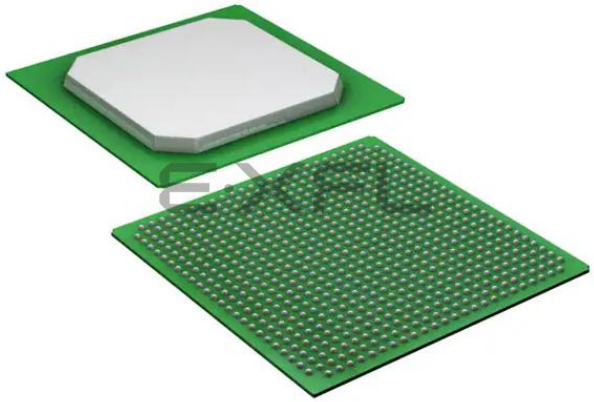

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

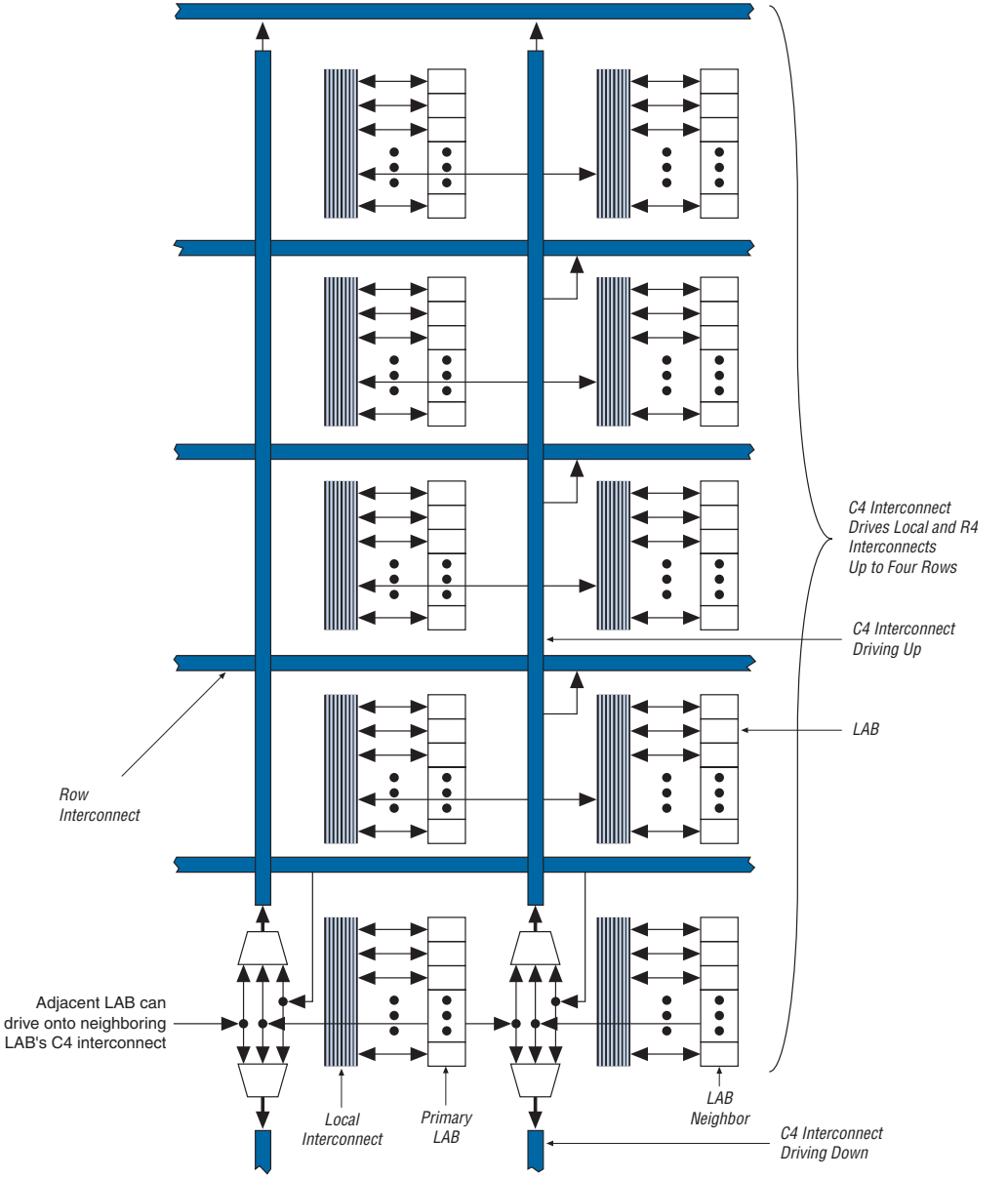
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

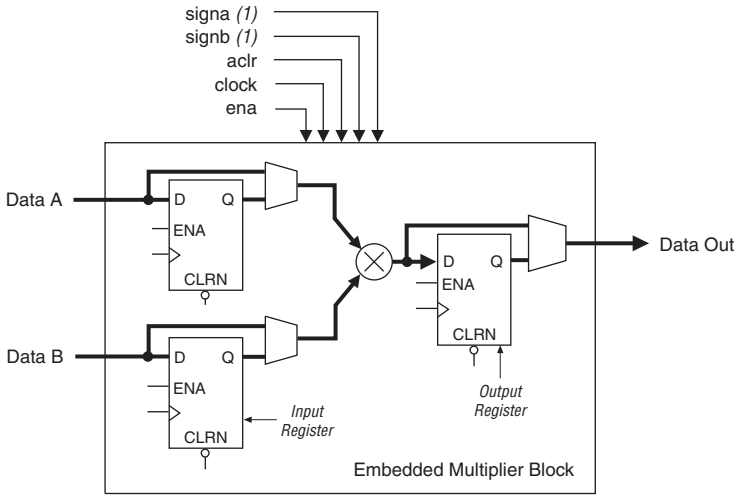
Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	475
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35f672c7

Figure 2–10. C4 Interconnect Connections *Note (1)*



Note to Figure 2–10:
(1) Each C4 interconnect can drive either up or down four rows.

Figure 2–18. Multiplier Block Architecture



Note to Figure 2–18:
(1) If necessary, these signals can be registered once to match the data signal path.

Each multiplier operand can be a unique signed or unsigned number. Two signals, `signa` and `signb`, control the representation of each operand respectively. A logic 1 value on the `signa` signal indicates that data A is a signed number while a logic 0 value indicates an unsigned number. Table 2–11 shows the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

Table 2–11. Multiplier Sign Representation

Data A (signa Value)	Data B (signb Value)	Result
Unsigned	Unsigned	Unsigned
Unsigned	Signed	Signed
Signed	Unsigned	Signed
Signed	Signed	Signed

I/O Delays

Refer to Tables 5–39 through 5–43 for I/O delays.

Table 5–39. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 1 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
LVTTL	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
2.5V	t_{PI}	624	654	1192	1238	1283	1283	ps
	t_{PCOUT}	410	430	730	793	855	855	ps
1.8V	t_{PI}	725	760	1372	1428	1484	1484	ps
	t_{PCOUT}	511	536	910	983	1056	1056	ps
1.5V	t_{PI}	790	828	1439	1497	1556	1556	ps
	t_{PCOUT}	576	604	977	1052	1128	1128	ps
LVCMOS	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
SSTL_2_CLASS_I	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_2_CLASS_II	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_18_CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
SSTL_18_CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 6 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.5V_DIFFERENTIAL _HSTL_CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
LVDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
RSDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
MINI_LVDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
SIMPLE_RSDS	—	t_{OP}	1221	1280	2258	2435	2605	2612	ps
		t_{DIP}	1353	1419	2428	2629	2831	2831	ps
1.2V_HSTL	—	t_{OP}	2403	2522	4635	5344	6046	6053	ps
		t_{DIP}	2535	2661	4805	5538	6272	6272	ps
1.2V_DIFFERENTIAL _HSTL	—	t_{OP}	2403	2522	4635	5344	6046	6053	ps
		t_{DIP}	2535	2661	4805	5538	6272	6272	ps

Notes to Table 5–42:

(1) This is the default setting in the Quartus II software.
(2) These numbers are for commercial devices.
(3) These numbers are for automotive devices.

Table 5–53 shows the JTAG timing parameters and values for Cyclone II devices.

Table 5–53. Cyclone II JTAG Timing Parameters and Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU}	JTAG port setup time *(2)*	5	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(2)*	—	13	ns
t_{JPZX}	JTAG port high impedance to valid output *(2)*	—	13	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2)*	—	13	ns
t_{JSSU}	Capture register setup time *(2)*	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5–53:

(1) This information is preliminary.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the JTAG port and capture register clock setup time is 3 ns and port clock to output time is 15 ns.

Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Cyclone II devices are in the 18th position or after they will fail configuration. This does not affect the SignalTap® II logic analyzer.

For more information on JTAG, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in the *Cyclone II Handbook*.

Table 7–2 provides an overview of the Cyclone II PLL features.

Table 7–2. Cyclone II PLL Features

Feature	Description
Clock multiplication and division	*m* / (*n* × post-scale counter) *(1)*
Phase shift	Down to 125-ps increments *(2)*, *(3)*
Programmable duty cycle	✓
Number of internal clock outputs	Up to three per PLL *(4)*
Number of external clock outputs	One per PLL *(4)*
Locked port can feed logic array	✓
PLL clock outputs can feed logic array	✓
Manual clock switchover	✓
Gated lock	✓

Notes to Table 7–2:

(1) *m* and post-scale counter values range from 1 to 32. *n* ranges from 1 to 4.

(2) The smallest phase shift is determined by the voltage control oscillator (VCO) period divided by 8.

(3) For degree increments, Cyclone II devices can shift output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the VCO frequency.

(4) The Cyclone II PLL has three output counters that drive the global clock network. One of these output counters (c2) can also drive a dedicated external I/O pin (single ended or differential). This counter output can also drive the external clock output (`PLL<#>_OUT`) and internal global clock network at the same time.

Cyclone II PLL Hardware Overview

Cyclone II devices contain up to four PLLs that are arranged in the four corners of the Cyclone II device as shown in Figure 7–1, which shows a top-level diagram of the Cyclone II device and the PLL locations.

The loop filter converts these up and down signals to a voltage that is used to bias the VCO. If the charge pump receives a logic high on the up signal, current is driven into the loop filter. If the charge pump receives a logic high on the down signal, current is drawn from the loop filter. The loop filter filters out glitches from the charge pump and prevents voltage over-shoot, which minimizes the jitter on the VCO.

The voltage from the charge pump determines how fast the VCO operates. The VCO is implemented as an four-stage differential ring oscillator. A divide counter, *m*, is inserted in the feedback loop to increase the VCO frequency above the input reference frequency, making the VCO frequency $f_{VCO} = m \times f_{REF}$. Therefore, the feedback clock, f_{FB}, applied to one input of the PFD, is locked to the input reference clock, f_{REF} (f_{IN}/n), applied to the other input of the PFD.

The VCO output can feed up to three post-scale counters (c0, c1, and c2). These post-scale counters allow a number of harmonically related frequencies to be produced by the PLL.

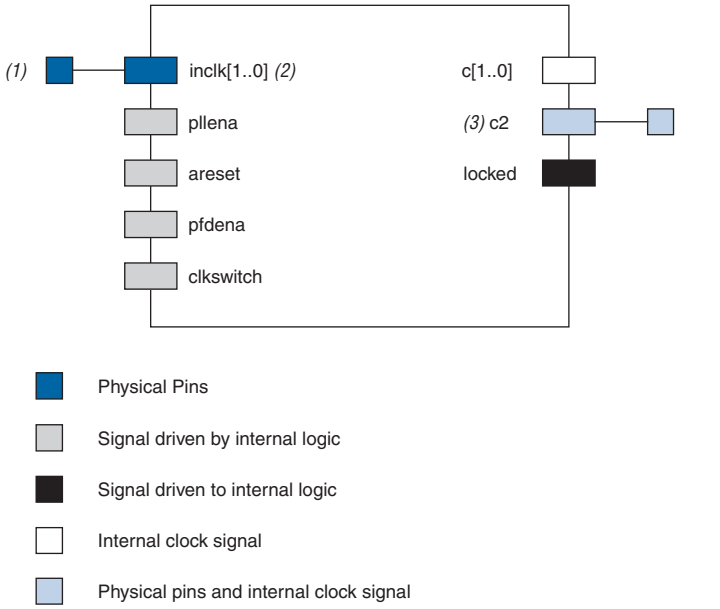
Additionally, Cyclone II PLLs have internal delay elements to compensate for routing on the global clock networks and I/O buffers. These internal delays are fixed and not accessible to the user.

Figure 7–2 shows a simplified block diagram of the major components of a Cyclone II device PLL.

Software Overview

You can use the altpll megafunction in the Quartus II software to enable Cyclone II PLLs. Figure 7–3 shows the available ports in Cyclone II PLLs and their sources and destinations. The c0 and c1 counters feed the internal global clock networks and the c2 counter can feed the global clock network and a dedicated external clock output pin (PLL<#>_OUT) at the same time.

Figure 7–3. Cyclone II PLL Signals



Notes to Figure 7–3:

(1) These signals can be assigned to either a single-ended or differential I/O standard.
(2) The inclk must be driven by one of two dedicated clock input pins.
(3) This counter output can drive both a dedicated external clock output (PLL<#>_OUT) and the global clock network.

locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals

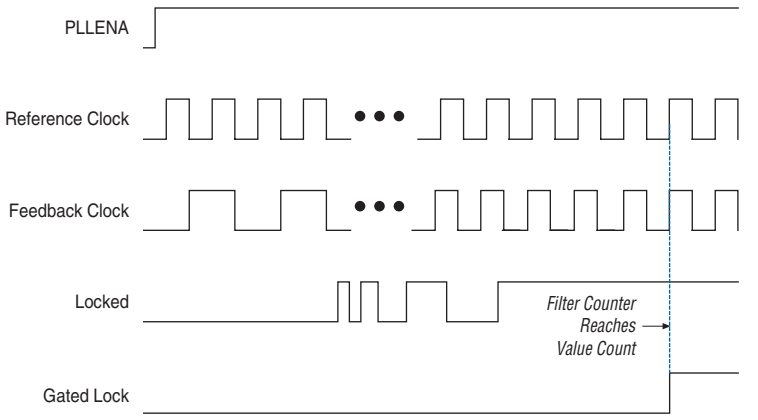
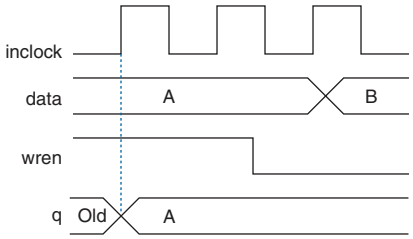


Figure 8–22. Cyclone II Same-Port Read-During-Write Functionality *Note (1)*



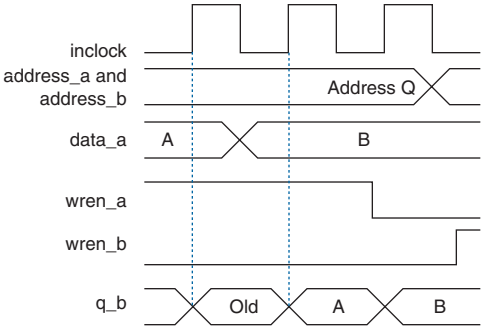
Note to Figure 8–22:
(1) Outputs are not registered.

Mixed-Port Read-During-Write Mode

This mode applies to a RAM in simple or true dual-port mode, which has one port reading and the other port writing to the same address location with the same clock.

In this mode, you also have two output choices: old data or don't care. In Old Data Mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In Don't Care Mode, the same operation results in a "don't care" or unknown value on the RAM outputs.

Figure 8–23. Cyclone II Mixed-Port Read-During-Write: Old Data Mode *Note (1)*



Note to Figure 8–23:
(1) Outputs are not registered.

Phase Lock Loop (PLL)

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two outputs is needed to generate the system clock and the write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock shifts by –90° from the system clock and generates the DQ signals during writes.

Clock Delay Control

Clock delay control circuit on each DQS pin allows a phase shift that center-aligns the incoming DQS signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal then clocks the DQ signals on internal LE registers. The clock delay control circuitry is used during the read operations where the DQS signals are acting as input clocks or strobes.

Figure 9–8 illustrates DDR SDRAM interfacing from the I/O pins through the dedicated circuitry to the logic array.

Figure 9–8. DDR SDRAM Interfacing

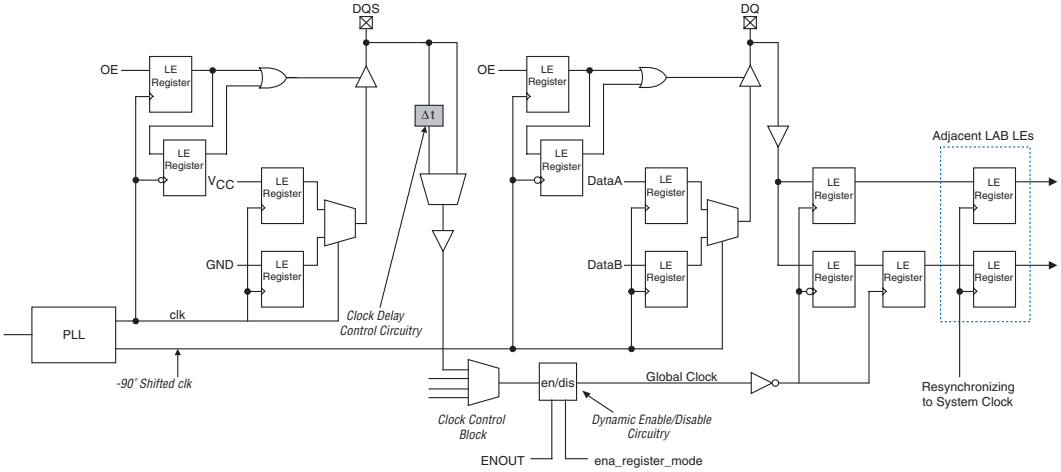


Figure 9–1 on page 9–4 shows an example where the DQS signal is shifted by 90°. The DQS signal goes through the 90° shift delay set by the clock delay control circuitry and global clock routing delay from the clock delay control circuitry to the DQ LE registers. The DQ signals only goes through routing delays from the DQ pin to the DQ LE registers. The delay from

10. Selectable I/O Standards in Cyclone II Devices

CII51010-2.4

Introduction

The proliferation of I/O standards and the need for improved I/O performance have made it critical that low-cost devices have flexible I/O capabilities. Selectable I/O capabilities such as SSTL-18, SSTL-2, and LVDS compatibility allow Cyclone® II devices to connect to other devices on the same printed circuit board (PCB) that may require different operating and I/O voltages. With these aspects of implementation easily manipulated using the Altera® Quartus® II software, the Cyclone II device family allows you to use low cost FPGAs while keeping pace with increasing design complexity.

This chapter is a guide to understanding the input and output capabilities of the Cyclone II devices, including:

- Supported I/O standards
- Cyclone II I/O banks
- Programmable current drive strength
- I/O termination
- Pad placement and DC guidelines

For information on hot socketing, refer to the *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information on ESD specifications, refer to the *Altera Reliability Report*.

Supported I/O Standards

Cyclone II devices support the I/O standards shown in Table 10–1.

For more details on the I/O standards discussed in this section, including target data rates and voltage values for each I/O standard, refer to the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*.

11. High-Speed Differential Interfaces in Cyclone II Devices

CII51011-2.2

Introduction

From high-speed backplane applications to high-end switch boxes, low-voltage differential signaling (LVDS) is the technology of choice. LVDS is a low-voltage differential signaling standard, allowing higher noise immunity than single-ended I/O technologies. Its low-voltage swing allows for high-speed data transfers, low power consumption, and reduced electromagnetic interference (EMI). LVDS I/O signaling is a data interface standard defined in the TIA/EIA-644 and IEEE Std. 1596.3 specifications.

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced EMI. National Semiconductor Corporation and Texas Instruments introduced the RSDS and mini-LVDS specifications, respectively. Currently, many designers use these specifications for flat panel display links between the controller and the drivers that drive display column drivers. Cyclone® II devices support the RSDS and mini-LVDS I/O standards at speeds up to 311 megabits per second (Mbps) at the transmitter.

Altera® Cyclone II devices can transmit and receive data through LVDS signals at a data rate of up to 640 Mbps and 805 Mbps, respectively. For the LVDS transmitter and receiver, the Cyclone II device's input and output pins support serialization and deserialization through internal logic.

This chapter describes how to use Cyclone II I/O pins for differential signaling and contains the following topics:

- Cyclone II high-speed I/O banks
- Cyclone II high-speed I/O interface
- LVDS, RSDS, mini-LVDS, LVPECL, differential HSTL, and differential SSTL I/O standards support in Cyclone II devices
- High-speed I/O timing in Cyclone II devices
- Design guidelines

Cyclone II High-Speed I/O Banks

Cyclone II device I/O banks are shown in Figures 11–1 and 11–2. The EP2C5 and EP2C8 devices offer four I/O banks and EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices offer eight I/O banks. A subset of

Table 13–1. Cyclone II Configuration Schemes		
Configuration Scheme	**MSEL1**	**MSEL0**
AS (20 MHz)	0	0
PS	0	1
Fast AS (40 MHz) *(1)*	1	0
JTAG-based Configuration *(2)*	*(3)*	*(3)*

Notes to Table 13–1:

(1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

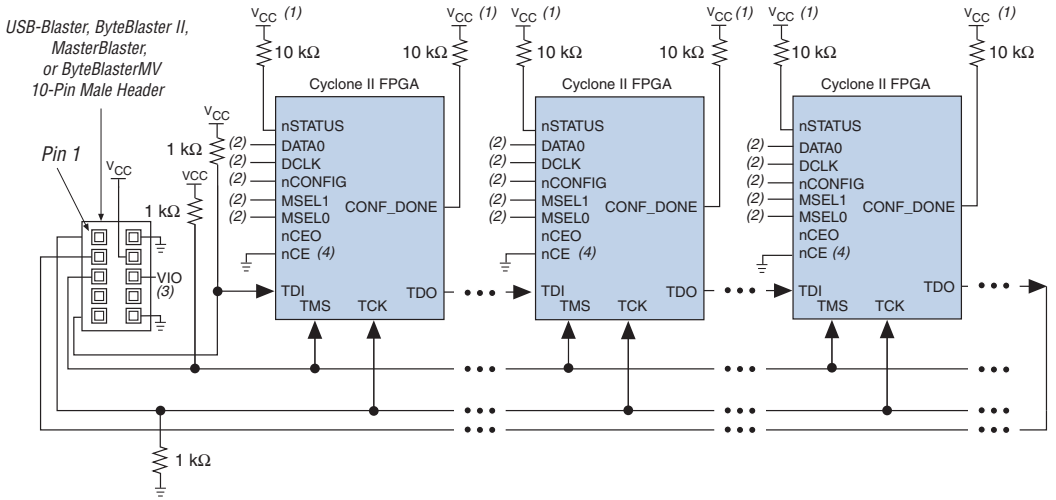
(2) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

(3) Do not leave the MSEL pins floating; connect them to V_{CCIO} or ground. These pins support the non-JTAG configuration scheme used in production. If you are only using JTAG configuration, you should connect the MSEL pins to ground.

You can download configuration data to Cyclone II FPGAs with the AS, PS, or JTAG interfaces using the options in Table 13–2.

Table 13–2. Cyclone II Device Configuration Schemes	
Configuration Scheme	**Description**
AS configuration	Configuration using serial configuration devices (EPCS1, EPCS4, EPCS16 or EPCS64 devices)
PS configuration	Configuration using enhanced configuration devices (EPC4, EPC8, and EPC16 devices), EPC2 and EPC1 configuration devices, an intelligent host (microprocessor), or a download cable
JTAG-based configuration	Configuration via JTAG pins using a download cable, an intelligent host (microprocessor), or the Jam™ Standard Test and Programming Language (STAPL)

Figure 13–24. JTAG Configuration of Multiple Devices Using a Download Cable



Notes to Figure 13–24:

(1) The pull-up resistor should be connected to the same supply voltage as the USB-Blaster, MasterBlaster (VIO pin), ByteBlaster II or ByteBlasterMV cable.

(2) Connect the nCONFIG and MSEL[1..0] pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the nCONFIG pin to V_{CC}, and the MSEL[1..0] pins to ground. In addition, pull DCLK and DATA0 to either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cable, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) nCE must be connected to ground or driven low for successful JTAG configuration.

Connect the nCE pin to GND or pull it low during JTAG configuration. In multiple device AS and PS configuration chains, connect the first device's nCE pin to GND and connect its nCEO pin to the nCE pin of the next device in the chain or you can use it as a user I/O pin after configuration.

After the first device completes configuration in a multiple device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, you should make sure the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multiple device configuration chain, the nCEO pin of the previous device drives the nCE pin of the next device low when it has successfully been JTAG configured.

frequency (up to 40 MHz), which reduces your configuration time. In addition, Cyclone II devices can receive a compressed configuration bitstream and decompress this data on-the-fly in the AS or PS configuration scheme, which further reduces storage requirements and configuration time.

Section VII. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. The chapters in this section contain the required PCB layout guidelines and package specifications.

This section includes the following chapters:

- Chapter 15, Package Information for Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.