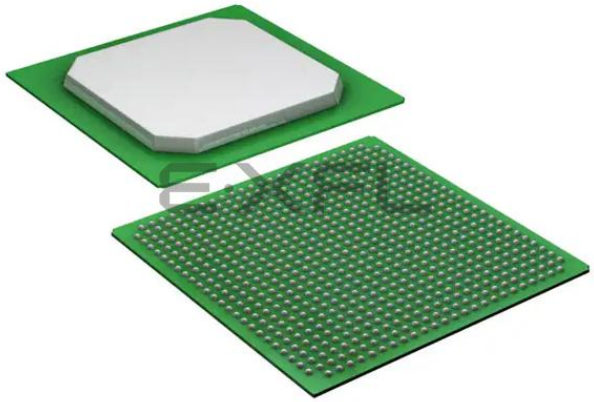

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	475
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35f672i8

Chapter 10. Selectable I/O Standards in Cyclone II Devices
Revised: *February 2008*
Part number: *CII51010-2.4*

Chapter 11. High-Speed Differential Interfaces in Cyclone II Devices
Revised: *February 2007*
Part number: *CII51011-2.2*

Chapter 12. Embedded Multipliers in Cyclone II Devices
Revised: *February 2007*
Part number: *CII51012-1.2*

Chapter 13. Configuring Cyclone II Devices
Revised: *February 2007*
Part number: *CII51013-3.1*

Chapter 14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices
Revised: *February 2007*
Part number: *CII51014-2.1*

Chapter 15. Package Information for Cyclone II Devices
Revised: *February 2007*
Part number: *CII51015-2.3*

Table 1–2. Cyclone II Package Options & Maximum User I/O Pins *Notes (1) (2)*

Device	144-Pin TQFP *(3)*	208-Pin PQFP *(4)*	240-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA	896-Pin FineLine BGA
EP2C5 *(6) (8)*	89	142	—	158 *(5)*	—	—	—	—
EP2C8 *(6)*	85	138	—	182	—	—	—	—
EP2C8A *(6)*, *(7)*	—	—	—	182	—	—	—	—
EP2C15A *(6)*, *(7)*	—	—	—	152	315	—	—	—
EP2C20 *(6)*	—	—	142	152	315	—	—	—
EP2C20A *(6)*, *(7)*	—	—	—	152	315	—	—	—
EP2C35 *(6)*	—	—	—	—	322	322	475	—
EP2C50 *(6)*	—	—	—	—	294	294	450	—
EP2C70 *(6)*	—	—	—	—	—	—	422	622

Notes to Table 1–2:

(1) Cyclone II devices support vertical migration within the same package (for example, you can migrate between the EP2C20 device in the 484-pin FineLine BGA package and the EP2C35 and EP2C50 devices in the same package).

(2) The Quartus® II software I/O pin counts include four additional pins, `TDI`, `TDO`, `TMS`, and `TCK`, which are not available as general purpose I/O pins.

(3) TQFP: thin quad flat pack.

(4) PQFP: plastic quad flat pack.

(5) Vertical migration is supported between the EP2C5F256 and the EP2C8F256 devices. However, not all of the DQ and DQS groups are supported. Vertical migration between the EP2C5 and the EP2C15 in the F256 package is not supported.

(6) The I/O pin counts for the EP2C5, EP2C8, and EP2C15A devices include 8 dedicated clock pins that can be used for data inputs. The I/O counts for the EP2C20, EP2C35, EP2C50, and EP2C70 devices include 16 dedicated clock pins that can be used for data inputs.

(7) EP2C8A, EP2C15A, and EP2C20A have a Fast On feature that has a faster POR time. The EP2C15A is only available with the Fast On option.

(8) The EP2C5 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. Refer to the Cyclone II section in the *Automotive-Grade Device Handbook*.

Cyclone II devices support vertical migration within the same package (for example, you can migrate between the EP2C35, EPC50, and EP2C70 devices in the 672-pin FineLine BGA package). The exception to vertical migration support within the Cyclone II family is noted in Table 1–3.

Programmable delays can increase the register-to-pin delays for output registers. Table 2–13 shows the programmable delays for Cyclone II devices.

Table 2–13. Cyclone II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to internal LE registers that reside in two different areas of the device. You set the two combinational input delays by selecting different delays for two different paths under the **Input delay from pin to internal cells logic** option in the Quartus II software. However, if the pin uses the input register, one of delays is disregarded because the IOE only has two paths to internal logic. If the input register is used, the IOE uses one input path. The other input path is then available for the combinational path, and only one input delay assignment is applied.

The IOE registers in each I/O block share the same source for clear or preset. You can program preset or clear for each individual IOE, but both features cannot be used simultaneously. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available for the IOE registers.

External Memory Interfacing

Cyclone II devices support a broad range of external memory interfaces such as SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature dedicated high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The programmable DQS delay chain allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Advanced I/O Standard Support

Table 2–17 shows the I/O standards supported by Cyclone II devices and which I/O pins support them.

Table 2–17. Cyclone II Supported I/O Standards & Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top & Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS *(1)*	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(2)*	*(2)*	*(2)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(2)*	*(2)*	*(2)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(2)*	*(2)*	*(2)*
PCI and PCI-X *(1) (3)*	Single ended	3.3 V	3.3 V			✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(4)*	*(5)*	2.5 V				✓	
		2.5 V	*(5)*	✓ *(6)*		✓ *(6)*		
Differential SSTL-18 class I or class II	Pseudo differential *(4)*	*(5)*	1.8 V				✓ *(7)*	
		1.8 V	*(5)*	✓ *(6)*		✓ *(6)*		

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI). Cyclone II devices support the RSDS and mini-LVDS I/O standards at data rates up to 311 Mbps at the transmitter.

A subset of pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. The dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry. Therefore, internal logic performs serialization and deserialization functions.

Cyclone II pin tables list the pins that support the high-speed I/O interface. The number of LVDS channels supported in each device family member is listed in Table 2–18.

Table 2–18. Cyclone II Device LVDS Channels (Part 1 of 2)

Device	Pin Count	Number of LVDS Channels *(1)*
EP2C5	144	31 (35)
	208	56 (60)
	256	61 (65)
EP2C8	144	29 (33)
	208	53 (57)
	256	75 (79)
EP2C15	256	52 (60)
	484	128 (136)
EP2C20	240	45 (53)
	256	52 (60)
	484	128 (136)
EP2C35	484	131 (139)
	672	201 (209)
EP2C50	484	119 (127)
	672	189 (197)

Table 5–13 shows the Cyclone II device pin capacitance for different I/O pin types.

Table 5–13. Device Capacitance *Note (1)*

Symbol	Parameter	Typical	Unit
C_{IO}	Input capacitance for user I/O pin.	6	pF
C_{LVDS}	Input capacitance for dual-purpose LVDS/user I/O pin.	6	pF
C_{VREF}	Input capacitance for dual-purpose VREF pin when used as VREF or user I/O pin.	21	pF
C_{CLK}	Input capacitance for clock pin.	5	pF

Note to Table 5–13:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflectometry (TDR). Measurement accuracy is within ±0.5 pF.

Power Consumption

You can calculate the power usage for your design using the PowerPlay Early Power Estimator and the PowerPlay Power Analyzer feature in the Quartus® II software.

The interactive PowerPlay Early Power Estimator is typically used during the early stages of FPGA design, prior to finalizing the project, to get a magnitude estimate of the device power. The Quartus II software PowerPlay Power Analyzer feature is typically used during the later stages of FPGA design. The PowerPlay Power Analyzer also allows you to apply test vectors against your design for more accurate power consumption modeling.

In both cases, only use these calculations as an estimation of power, not as a specification. For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *Power Estimation and Analysis* section in volume 3 of the *Quartus II Handbook*.

You can obtain the Excel-based PowerPlay Early Power Estimator at www.altera.com. Refer to Table 5–3 on page 5–3 for typical I_{CC} standby specifications.

The power-up current required by Cyclone II devices does not exceed the maximum static current. The rate at which the current increases is a function of the system power supply. The exact amount of current consumed varies according to the process, temperature, and power ramp rate. The duration of the I_{CCINT} power-up requirement depends on the V_{CCINT} voltage supply rise time.

Table 5–15. Cyclone II Performance (Part 4 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
Larger Designs	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Buffered Burst, 3 Mults/5 Adders FFT function	8053	60	36	200.0	195.0	149.23	163.02
	8-bit, 1024 pt, Quad Output, 4 Parallel FFT Engines, Buffered Burst, 4 Mults/2 Adders FFT function	7453	60	48	200.0	195.0	151.28	163.02

Notes to Table 5–15 :

(1) This application uses registered inputs and outputs.
(2) This application uses registered multiplier input and output stages within the DSP block.
(3) This application uses the same clock source for both A and B ports.
(4) This application uses independent clock sources for A and B ports.
(5) This application uses PLL clock outputs that are globally routed to connect and drive M4K clock ports. Use of non-PLL clock sources or local routing to drive M4K clock ports may result in lower performance numbers than shown here. Refer to the Quartus II timing report for actual performance numbers.
(6) These numbers are for commercial devices.
(7) These numbers are for automotive devices.

Internal Timing

Refer to Tables 5–16 through 5–19 for the internal timing parameters.

Table 5–16. LE_FF Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade *(1)*		–7 Speed Grade *(2)*		–8 Speed Grade *(3)*		Unit
	Min	Max	Min	Max	Min	Max	
TSU	–36	—	–40	—	–40	—	ps
	—	—	–38	—	–40	—	ps
TH	266	—	306	—	306	—	ps
	—	—	286	—	306	—	ps
TCO	141	250	135	277	135	304	ps
	—	—	141	—	141	—	ps
TCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Table 5–30. EP2C35 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.410	1.476	2.514	2.724	2.986	ns
t_{COUT}	1.412	1.478	2.530	2.737	2.994	ns
t_{PLLCIN}	–0.117	–0.127	0.134	0.162	0.241	ns
$t_{PLLCOUT}$	–0.115	–0.125	0.15	0.175	0.249	ns

EP2C50 Clock Timing Parameters

Tables 5–31 and 5–32 show the clock timing parameters for EP2C50 devices.

Table 5–31. EP2C50 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.759	2.940	3.174	ns
t_{COUT}	1.589	1.666	2.793	2.972	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.113	0.075	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.147	0.107	0.118	ns

Table 5–32. EP2C50 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.624	2.791	3.010	ns
t_{COUT}	1.465	1.535	2.640	2.804	3.018	ns
t_{PLLCIN}	–0.261	–0.276	–0.022	–0.074	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	–0.006	–0.061	–0.067	ns

In addition, the clock networks in the Cyclone II device support dynamic selection of the clock source and also support a power-down mode where clock networks that are not being used can easily be turned off, reducing the overall power consumption of the device.

ROM Mode

Cyclone II memory blocks support ROM mode. A MIF initializes the ROM contents of these blocks. The address lines of the ROM are registered. The outputs can be registered or unregistered. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Buffer Mode

A single clock or dual clock FIFO buffer may be implemented in the memory blocks. Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain. All FIFO memory configurations have synchronous inputs. However, the FIFO buffer outputs are always combinational (i.e., not registered). Simultaneous read and write from an empty FIFO buffer is not supported.

For more information on FIFO buffers, refer to the *Single- & Dual-Clock FIFO Megafunctions User Guide*.

Clock Modes

Depending on which memory mode is selected, the following clock modes are available:

- Independent
- Input/output
- Read/write
- Single-clock

Table 8–7 shows these clock modes supported by all memory blocks when configured in each respective memory modes.

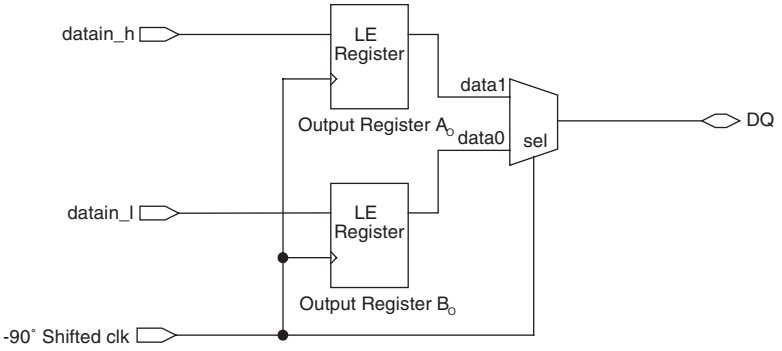
Table 8–7. Cyclone II Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

DDR Output Registers

Figure 9–14 shows a schematic representation of DDR output implemented in a Cyclone II device. The DDR output logic is implemented using LEs in the LAB adjacent to the output pin. Two registers synchronize two serial data streams. The registered outputs are then multiplexed by the common clock to drive the DDR output pin at two times the data rate.

Figure 9–14. DDR Output Implementation for DDR Memory Interfaces



While the clock signal is logic-high, the output from output register A_O is driven onto the DDR output pin. While the clock signal is logic-low, the output from output register B_O is driven onto the DDR output pin. The DDR output pin can be any available user I/O pin. Altera recommends the use of `altdq` and `altdqs` megafunctions to implement this output logic. This automatically provides the required tight placement and routing constraints on the LE registers and the output multiplexer.

Figure 9–15 shows examples of functional waveforms from a DDR output implementation.

Table 10–5 shows I/O standards supported when a pin is used as a regular I/O pin in the I/O banks of Cyclone II devices.

Table 11–1. LVDS I/O Specifications (Part 2 of 2) *Note (1)*

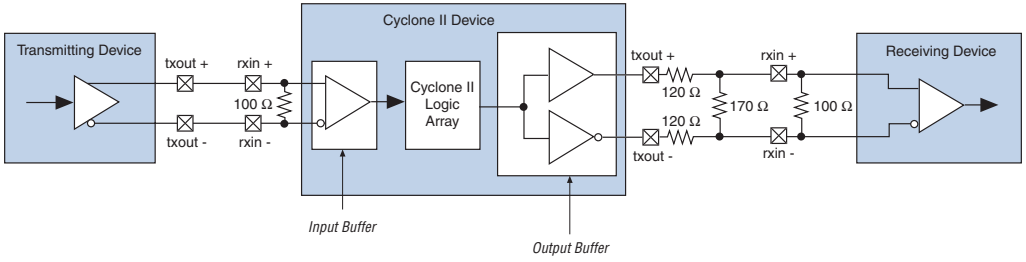
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{ID}	Input differential voltage (single-ended)		0.1		0.65	V
V_{ICM}	Input common mode voltage		0.1		2.0	V
ΔV_{OS}	Change in V_{OS} between H and L	R_L = 100 Ω			50	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Note to Table 11–1:
(1) The specifications apply at the resistor network output.

LVDS Receiver & Transmitter

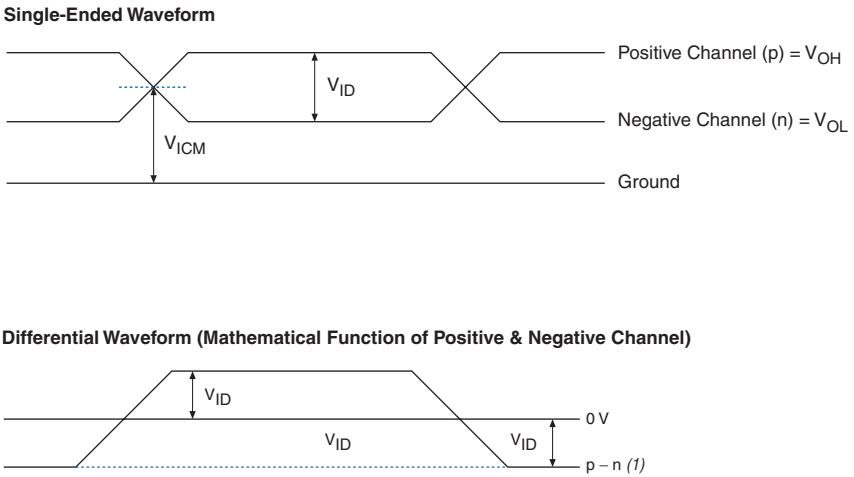
Figure 11–3 shows a simple point-to-point LVDS application where the source of the data is an LVDS transmitter. These LVDS signals are typically transmitted over a pair of printed circuit board (PCB) traces, but a combination of a PCB trace, connectors, and cables is a common application setup.

Figure 11–3. Typical LVDS Application



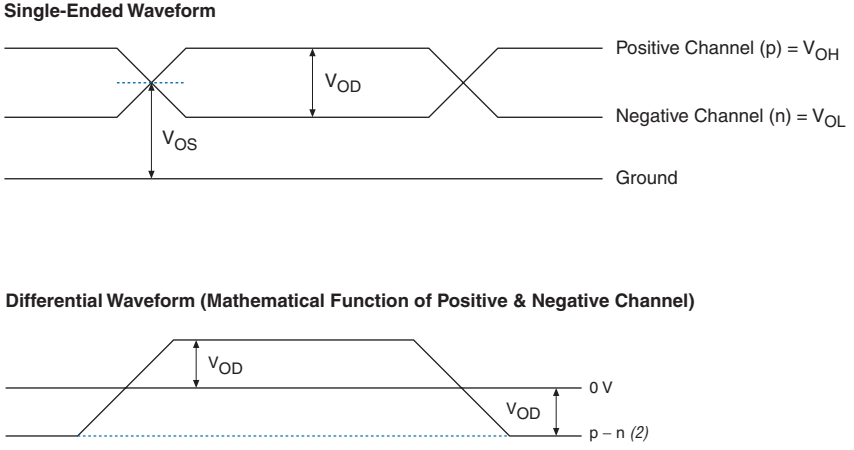
Figures 11–4 and 11–5 show the signaling levels for LVDS receiver inputs and transmitter outputs, respectively.

Figure 11–4. Receiver Input Waveforms for the LVDS Differential I/O Standard



Note to Figure 11–4:
(1) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 11–5. Transmitter Output Waveform for the LVDS Differential I/O Standard *Note (2)*



Notes to Figure 11–5:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

When the `signa` and `signb` signals are unused, the Quartus® II software sets the multiplier to perform unsigned multiplication by default.

Output Registers

You can choose to register the embedded multiplier output using the output registers in 18- or 36-bit sections depending on the operational mode of the multiplier. The following control signals are available to each output register within the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers within a single embedded multiplier are fed by the same clock, clock enable, or asynchronous clear signal.

See the *Cyclone II Architecture* chapter in Volume 1 of the ***Cyclone II Device Handbook*** for more information on the embedded multiplier routing and interface.

Operational Modes

The embedded multiplier can be used in one of two operational modes, depending on the application needs:

- One 18-bit multiplier
- Up to two 9-bit independent multipliers

The Quartus II software includes megafunctions used to control the mode of operation of the multipliers. After you have made the appropriate parameter settings using the megafunction's MegaWizard® Plug-In Manager, the Quartus II software automatically configures the embedded multiplier.

The Cyclone II embedded multipliers can also be used to implement multiplier adder and multiplier accumulator functions where the multiplier portion of the function is implemented using embedded multipliers and the adder or accumulator function is implemented in logic elements (LEs).

For more information on megafunction and Quartus II support for Cyclone II embedded multipliers, see the "Software Support" section.

Section VI. Configuration & Test

This section provides configuration information for all of the supported configuration schemes for Cyclone® II devices. These configuration schemes use either a microprocessor, configuration device, or download cable. There is detailed information on how to design with Altera® configuration devices. The last chapter provides information on JTAG support in Cyclone II devices.

This section includes the following chapters:

- Chapter 13, Configuring Cyclone II Devices
- Chapter 14, IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

A device operating in JTAG mode uses the TDI, TDO, TMS, and TCK pins. The TCK pin has a weak internal pull-down resistor while the other JTAG input pins, TDI and TMS, have weak internal pull-up resistors. All user I/O pins are tri-stated during JTAG configuration. Table 13–9 explains each JTAG pin's function.

Table 13–9. Dedicated JTAG Pins

Pin Name	Pin Type	Description
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to GND.

The TDO output is powered by the V_{CCIO} power supply. If V_{CCIO} is tied to 3.3-V, both the I/O pins and the JTAG TDO port drive at 3.3-V levels.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the nCEO pin inputs to the next device's nCE pin, make sure that the nCEO pin is not used as a user I/O pin after configuration.

Other Altera devices that have JTAG support can be placed in the same JTAG chain for device programming and configuration.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP). Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information on JTAG and Jam STAPL in embedded environments, see *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*. To download the Jam player, go to the Altera web site (**www.altera.com**).

Configuring Cyclone II FPGAs with JRunner

JRunner is a software driver that allows you to configure Cyclone II devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in **.rbf** format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

The RBF file used by the JRunner software driver can not be a compressed RBF file because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

For more information on the JRunner software driver, see *JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site.

Figure 15–1 shows a 144-pin TQFP package outline.

Figure 15–1. 144-Pin TQFP Package Outline