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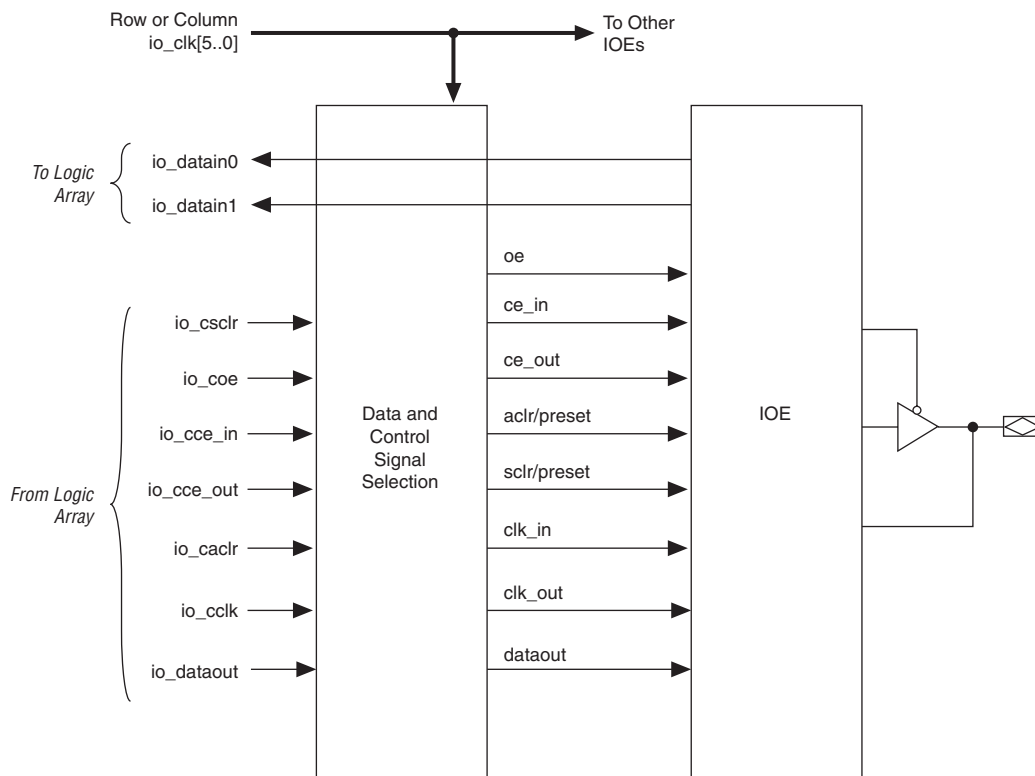
Details

Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	322
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35u484c6n

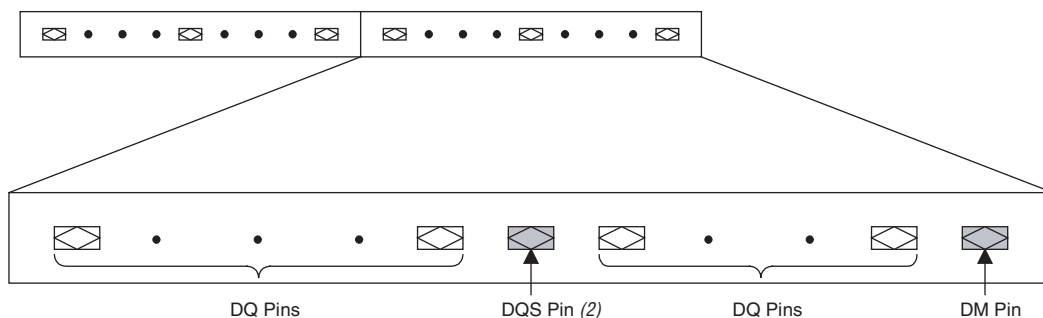
The pin's data in signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks, `io_clk[5..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions (see “Global Clock Network & Phase-Locked Loops” on page 2-16).

Figure 2-23 illustrates the signal paths through the I/O block.

Figure 2-23. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 2-24 illustrates the control signal selection.

Figure 2–26. Cyclone II Device DQ & DQS Groups in $\times 8/\times 9$ Mode *Notes (1), (2)***Notes to Figure 2–26:**

- (1) Each DQ group consists of a DQS pin, DM pin, and up to nine DQ pins.
- (2) This is an idealized pin layout. For actual pin layout, refer to the pin table.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR and DDR2 SDRAM. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. The dedicated external memory interface in Cyclone II devices also includes programmable delay circuitry that can shift the incoming DQS signals to center align the DQS signals within the data window.

The DQS signal is usually associated with a group of data (DQ) pins. The phase-shifted DQS signals drive the global clock network, which is used to clock the DQ signals on internal LE registers.

Table 2–15 shows the number of DQ pin groups per device.

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of $\times 8$ Groups	Number of $\times 9$ Groups (5), (6)	Number of $\times 16$ Groups	Number of $\times 18$ Groups (5), (6)
EP2C5	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
EP2C8	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
	256-pin FineLine BGA®	8 (3)	4	4	4
EP2C15	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8
EP2C20	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8

Introduction

Cyclone® II devices offer hot socketing (also known as hot plug-in, hot insertion, or hot swap) and power sequencing support without the use of any external devices. You can insert or remove a Cyclone II board in a system during system operation without causing undesirable effects to the board or to the running system bus.

The hot-socketing feature lessens the board design difficulty when using Cyclone II devices on printed circuit boards (PCBs) that also contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices. With the Cyclone II hot-socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Cyclone II hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Cyclone II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Cyclone II Hot-Socketing Specifications

Cyclone II devices offer hot-socketing capability with all three features listed above without any external components or special design requirements. The hot-socketing feature in Cyclone II devices offers the following:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer- -cial					
1.2V_DIFFERENTIAL_HSTL	t _{PI}	570	597	1263	1324	1385	1385	ps
	t _{PCOUT}	356	373	801	879	957	957	ps

Notes to Table 5–40 :

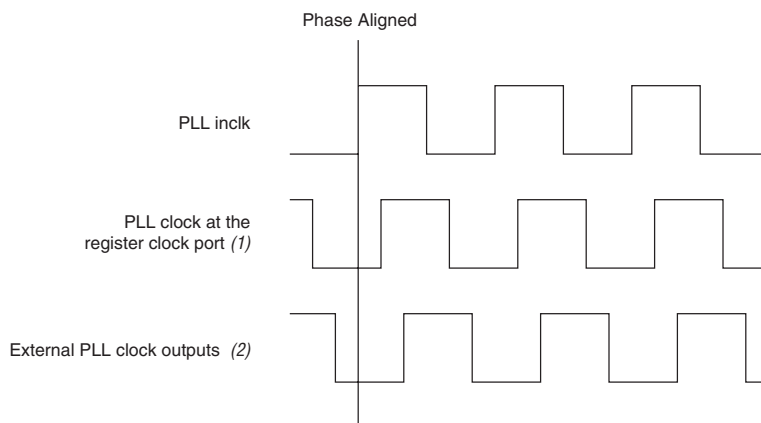
(1) These numbers are for commercial devices.

(2) These numbers are for automotive devices.

Table 5–41. Cyclone II I/O Input Delay for Row Pins (Part 1 of 2)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer- -cial					
LVTTTL	t _{PI}	583	611	1129	1160	1240	1240	ps
	t _{PCOUT}	366	384	762	784	855	855	ps
2.5V	t _{PI}	629	659	1099	1171	1244	1244	ps
	t _{PCOUT}	412	432	732	795	859	859	ps
1.8V	t _{PI}	729	764	1278	1360	1443	1443	ps
	t _{PCOUT}	512	537	911	984	1058	1058	ps
1.5V	t _{PI}	794	832	1345	1429	1513	1513	ps
	t _{PCOUT}	577	605	978	1053	1128	1128	ps
LVCMOS	t _{PI}	583	611	1129	1160	1240	1240	ps
	t _{PCOUT}	366	384	762	784	855	855	ps
SSTL_2_CLASS_I	t _{PI}	536	561	896	947	998	998	ps
	t _{PCOUT}	319	334	529	571	613	613	ps
SSTL_2_CLASS_II	t _{PI}	536	561	896	947	998	998	ps
	t _{PCOUT}	319	334	529	571	613	613	ps
SSTL_18_CLASS_I	t _{PI}	581	609	933	967	1004	1004	ps
	t _{PCOUT}	364	382	566	591	619	619	ps
SSTL_18_CLASS_II	t _{PI}	581	609	933	967	1004	1004	ps
	t _{PCOUT}	364	382	566	591	619	619	ps
1.5V_HSTL_CLASS_I	t _{PI}	593	621	1051	1109	1167	1167	ps
	t _{PCOUT}	376	394	684	733	782	782	ps

Figure 7–6. Phase Relationship between Cyclone II PLL Clocks in No Compensation Mode



Notes to Figure 7–6:

- (1) Internal clocks fed by the PLL are in phase with each other.
- (2) The external clock outputs can lead or lag the PLL internal clocks.

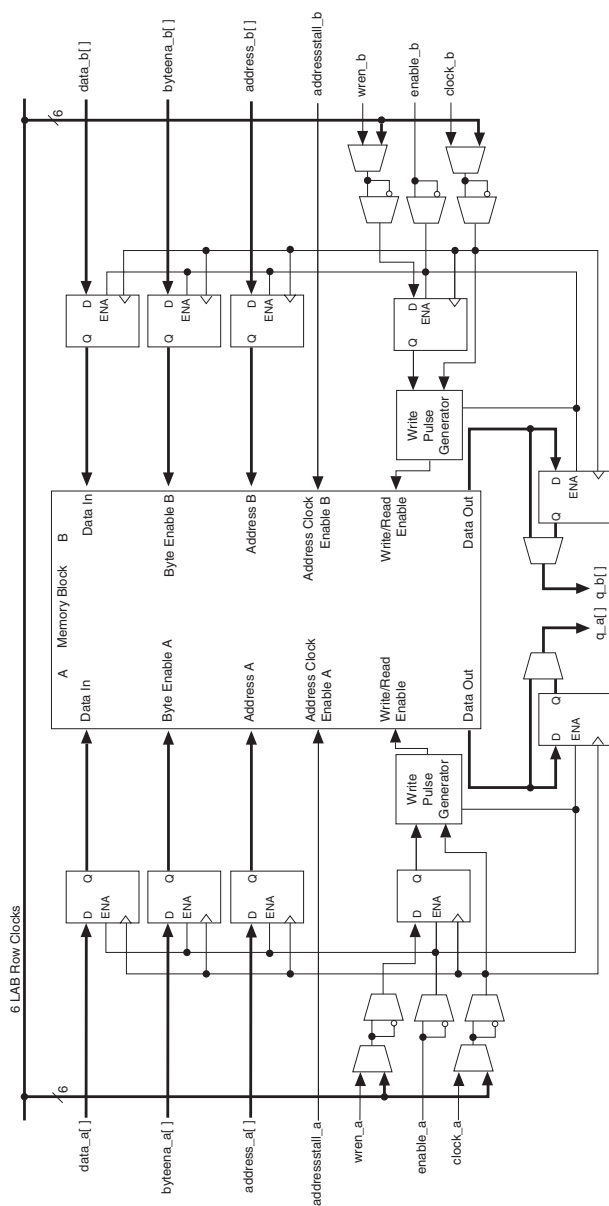
Source-Synchronous Mode

If data and clock arrive at the same time at the input pins, they are guaranteed to keep the same phase relationship at the clock and data ports of any IOE input register. Figure 7–7 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfer. Data and clock signals at the IOE experience similar buffer delays as long as the same I/O standard is used.

Independent Clock Mode

Cyclone II memory blocks can implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables for port A and B registers. However, ports do not support asynchronous clear signals for the registers.

Figure 8–13 shows a memory block in independent clock mode.

Figure 8–13. Cyclone II Memory Block in Independent Clock Mode *Note (1)***Note to Figure 8–13:**

- (1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Cyclone II DDR Memory Support Overview

Table 9–1 shows the external memory interfaces supported in Cyclone II devices.

<i>Table 9–1. External Memory Support in Cyclone II Devices</i> <i>Note (1)</i>				
Memory Standard	I/O Standard	Maximum Bus Width	Maximum Clock Rate Supported (MHz)	Maximum Data Rate Supported (Mbps)
DDR SDRAM	SSTL-2 class I (2)	72	167	333 (1)
	SSTL-2 class II (2)	72	133	267 (1)
DDR2 SDRAM	SSTL-18 class I (2)	72	167	333 (1)
	SSTL-18 class II (3)	72	125	250 (1)
QDRII SRAM (4)	1.8-V HSTL class I (2)	36	167	667 (1)
	1.8-V HSTL class II (3)	36	100	400 (1)

Notes to Table 9–1:

- (1) The data rate is for designs using the clock delay control circuitry.
- (2) These I/O standards are supported on all the I/O banks of the Cyclone II device.
- (3) These I/O standards are supported only on the I/O banks on the top and bottom of the Cyclone II device.
- (4) For maximum performance, Altera recommends using the 1.8-V HSTL I/O standard because of higher I/O drive strength. QDRII SRAM devices also support the 1.5-V HSTL I/O standard.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR SDRAM with the clock delay control circuitry that can shift the incoming DQS signals to center them within the data window. To achieve DDR operation, the DDR input and output registers are implemented using the internal logic element (LE) registers. You should use the `altdqs` and `altdq` megafunctions in the Quartus II software to implement the DDR registers used for DQS and DQ signals, respectively.

Phase Lock Loop (PLL)

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two outputs is needed to generate the system clock and the write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock shifts by -90° from the system clock and generates the DQ signals during writes.

Clock Delay Control

Clock delay control circuit on each DQS pin allows a phase shift that center-aligns the incoming DQS signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal then clocks the DQ signals on internal LE registers. The clock delay control circuitry is used during the read operations where the DQS signals are acting as input clocks or strobes.

Figure 9–8 illustrates DDR SDRAM interfacing from the I/O pins through the dedicated circuitry to the logic array.

Figure 9–8. DDR SDRAM Interfacing

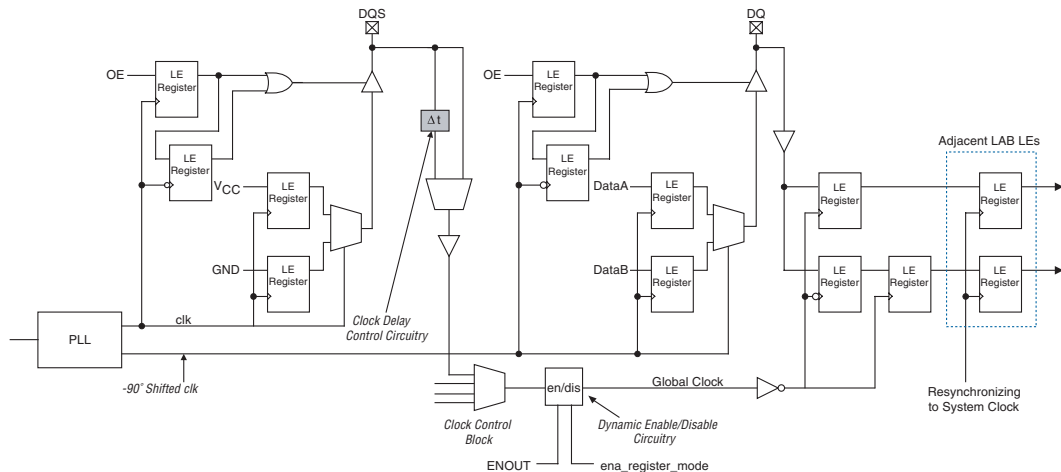


Figure 9–1 on page 9–4 shows an example where the DQS signal is shifted by 90° . The DQS signal goes through the 90° shift delay set by the clock delay control circuitry and global clock routing delay from the clock delay control circuitry to the DQ LE registers. The DQ signals only go through routing delays from the DQ pin to the DQ LE registers. The delay from

1.8-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-7)

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts.

The 1.8-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.8-V LVCMOS.

SSTL-18 Class I and II

The 1.8-V SSTL-18 standard is formulated under JEDEC Standard, JESD815: Stub Series Terminated Logic for 1.8V (SSTL-18).

The SSTL-18 I/O standard is a 1.8-V memory bus standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V V_{REF} and a 0.9-V V_{TT} , with the termination resistors connected to both. There are no class definitions for the SSTL-18 standard in the JEDEC specification. The specification of this I/O standard is based on an environment that consists of both series and parallel terminating resistors. Altera provides solutions to two derived applications in JEDEC specification and names them class I and class II to be consistent with other SSTL standards. Figures 10–5 and 10–6 show SSTL-18 class I and II termination, respectively. Cyclone II devices support both input and output levels.

Figure 10–5. 1.8-V SSTL Class I Termination

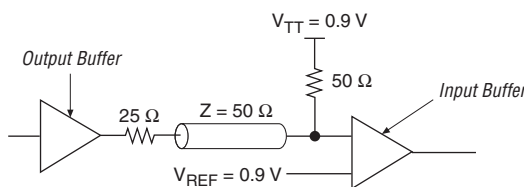
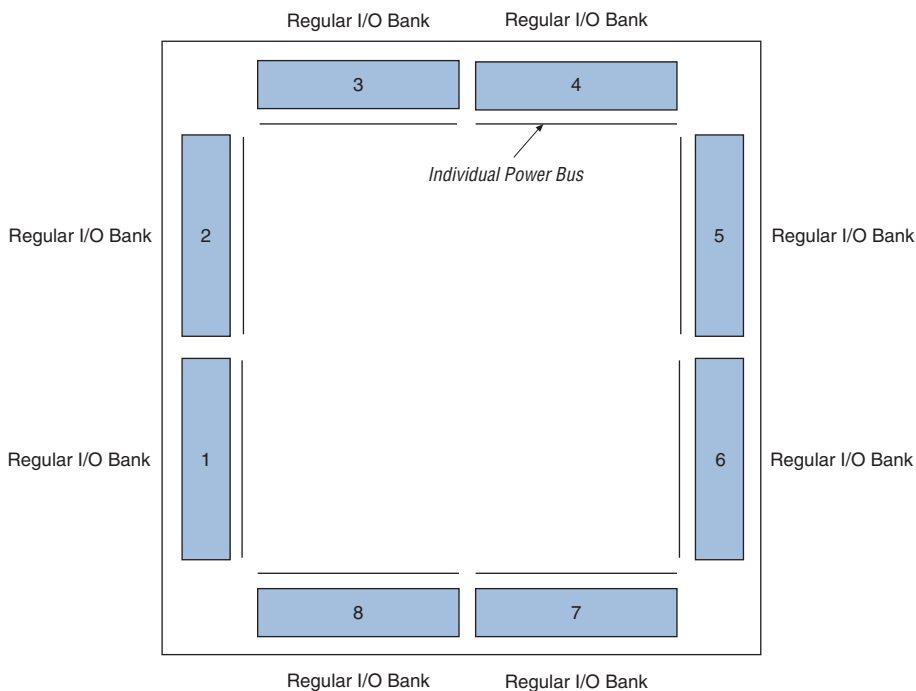


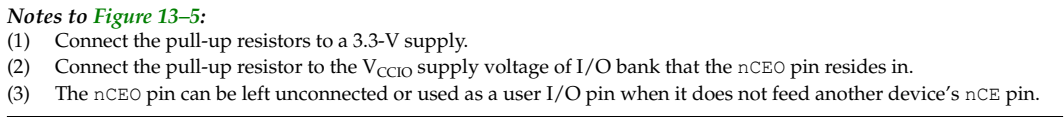
Figure 10–20. EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 Device I/O Banks *Notes (1), (2)***Notes to Figure 10–20:**

- (1) This is a top view of the silicon die.
- (2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Document Revision History

Table 11–6 shows the revision history for this document.

Table 11–6. Document Revision History		
Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	<ul style="list-style-type: none"> Added document revision history. Added <i>Note (1)</i> to Table 11–1. Updated Figure 11–5 and added <i>Note (1)</i> Added <i>Note (1)</i> to Table 11–2. Updated Figure 11–6 and added <i>Note (1)</i> Added <i>Note (1)</i> to Table 11–3. Added <i>Note (1)</i> to Figure 11–9. 	<ul style="list-style-type: none"> Added information stating LVDS/RSDS/mini-LVDS I/O standards specifications apply at the external resistors network output.
November 2005 v2.1	<ul style="list-style-type: none"> Updated Table 11–2. Updated Figures 11–7 through 11–9. Added Resistor Network Solution for RSDS. Updated note for mini-LVDS Resistor Network table. 	
July 2005 v2.0	<ul style="list-style-type: none"> Updated “I/O Standards Support” section. Updated Tables 11–1 through 11–3. 	
November 2004 v1.1	<ul style="list-style-type: none"> Updated Table 11–1. Updated Figures 11–4, 11–5, 11–7, and 11–9. 	
June 2004, v1.0	Added document to the Cyclone II Device Handbook.	





For more information on how to use the USB-Blaster, MasterBlaster, ByteBlaster II or ByteBlasterMV cables, refer to the following documents:

- *USB-Blaster USB Port Download Cable Data Sheet*
- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlaster II Parallel Port Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*

JTAG Configuration

The Joint Test Action Group (JTAG) has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture allows you to test components on PCBs with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. The JTAG circuitry can also be used to shift configuration data into the device. The Quartus II software automatically generates SOF files that can be used for JTAG configuration with a download cable in the Quartus II programmer.



For more information on JTAG boundary-scan testing, see the following documents:

- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in Volume 2 of the *Cyclone II Device Handbook*
- *Jam Programming & Testing Language Specification*

Cyclone II devices are designed such that JTAG instructions have precedence over any device configuration modes. This means that JTAG configuration can take place without waiting for other configuration modes to complete. For example, if you attempt JTAG configuration of Cyclone II devices during PS configuration, PS configuration terminates and JTAG configuration begins. If the Cyclone II MSEL pins are set to AS or fast AS mode, the Cyclone II device does not output a DCLK signal when JTAG configuration takes place.



You cannot use the Cyclone II decompression feature if you are configuring your Cyclone II device when using JTAG-based configuration.

enables the programming software to program or verify the target device. Configuration data driven into the target device appears on the TDO pin one clock cycle later.

The Quartus II software verifies successful JTAG configuration upon completion. At the end of configuration, the software checks the CONF_DONE pin through the JTAG port. When the Quartus II software generates a JAM file for a multiple device chain, it contains instructions so that all the devices in the chain are initialized at the same time. If CONF_DONE is not high, the Quartus II software indicates that configuration has failed. If the CONF_DONE pin transitions high, the software indicates that configuration was successful. After the configuration bitstream is transmitted serially via the JTAG TDI port, the TCK port is clocked an additional 299 cycles to perform Cyclone II device initialization.

The **Enable user-supplied start-up clock (CLKUSR)** option has no affect on the device initialization since this option is disabled in the SOF when configuring the FPGA in JTAG using the Quartus II programmer and download cable. Therefore, if you turn on the CLKUSR option, you do not need to provide a clock on CLKUSR when you are configuring the FPGA with the Quartus II programmer and a download cable.

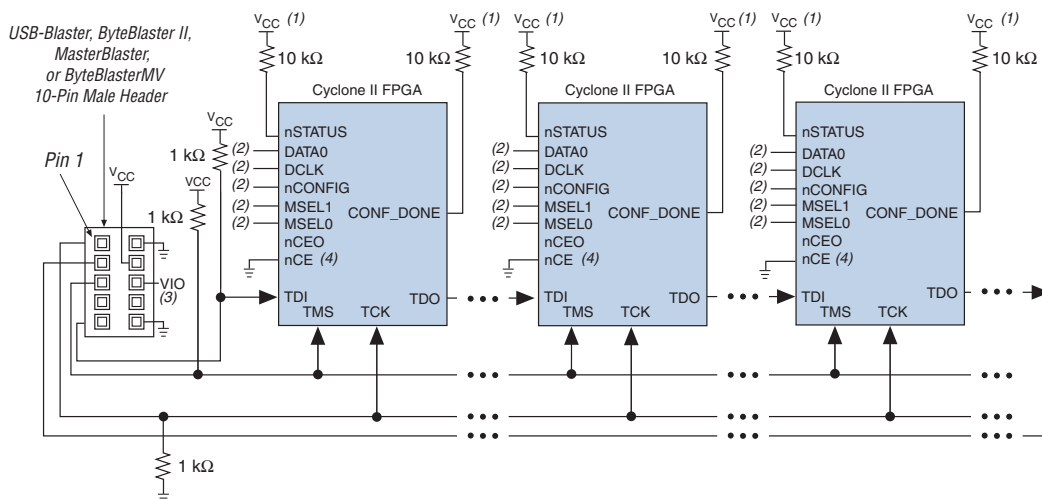
Cyclone II devices have dedicated JTAG pins that always function as JTAG pins. You can perform JTAG testing on Cyclone II devices before, after, and during configuration. Cyclone II devices support the BYPASS, IDCODE and SAMPLE instructions during configuration without interruption. All other JTAG instructions may only be issued by first interrupting configuration and reprogramming I/O pins using the CONFIG_IO instruction.

The CONFIG_IO instruction allows I/O buffers to be configured via the JTAG port. The CONFIG_IO instruction interrupts configuration. This instruction allows you to perform board-level testing before configuring the Cyclone II device or waiting for a configuration device to complete configuration. If you interrupt configuration, the Cyclone II device must be reconfigured via JTAG (PULSE_CONFIG instruction) or by pulsing nCONFIG low after JTAG testing is complete.



For more information, see the *MorphIO: An I/O Reconfiguration Solution for Altera White Paper*.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Cyclone II devices do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG operations (other than the usual boundary-scan operation).



- (1) The pull-up resistor should be connected to the same supply voltage as the USB-Blaster, MasterBlaster (VIO pin), ByteBlaster II or ByteBlasterMV cable.
- (2) Connect the nCONFIG and MSEL[1..0] pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the nCONFIG pin to VCC, and the MSEL[1..0] pins to ground. In addition, pull DCLK and DATA0 to either high or low, whichever is convenient on your board.
- (3) Pin 6 of the header is a VIO reference voltage for the MasterBlaster output driver. VIO should match the device's VCCIO. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cable, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) nCE must be connected to ground or driven low for successful JTAG configuration.

Connect the nCE pin to GND or pull it low during JTAG configuration. In multiple device AS and PS configuration chains, connect the first device's nCE pin to GND and connect its nCEO pin to the nCE pin of the next device in the chain or you can use it as a user I/O pin after configuration.

After the first device completes configuration in a multiple device configuration chain, its `nCEO` pin drives low to activate the second device's `nCE` pin, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, you should make sure the `nCE` pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multiple device configuration chain, the `nCEO` pin of the previous device drives the `nCE` pin of the next device low when it has successfully been JTAG configured.

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCEO	N/A if option is on. I/O if option is off.	All	Output	<p>This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration.</p> <p>If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor.</p> <p>Use the Quartus II software to make this pin a user I/O pin.</p>
ASDO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	<p>This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data.</p> <p>In AS mode, ASDO has an internal pull-up that is always active.</p>
nCSO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	<p>This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device.</p> <p>In AS mode, nCSO has an internal pull-up resistor that is always active.</p>

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Document
Revision History

Table 14–4 shows the revision history for this document.

Table 14–4. Document Revision History		
Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.1	<ul style="list-style-type: none">Added document revision history.Added new section “BST for Configured Devices”.	<ul style="list-style-type: none">Added information about ‘Always Enable Input Buffer’ option.
July 2005 v2.0	Moved the “JTAG Timing Specifications” section to the <i>DC Characteristics & Timing Specifications</i> chapter.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	



15. Package Information for Cyclone II Devices

CII51015-2.3

Introduction

This chapter provides package information for Altera® Cyclone® II devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Table 15–1 shows Cyclone II device package options.

Table 15–1. Cyclone II Device Package Options		
Device	Package	Pins
EP2C5	Plastic Thin Quad Flat Pack (TQFP) – Wirebond	144
	Plastic Quad Flat Pack (PQFP) – Wirebond	208
	Low profile FineLine BGA® – Wirebond	256
EP2C8	TQFP – Wirebond	144
	PQFP – Wirebond	208
	Low profile FineLine BGA – Wirebond	256
EP2C15	Low profile FineLine BGA, Option 2 – Wirebond	256
	FineLine BGA, Option 3– Wirebond	484
EP2C20	PQFP – Wirebond	240
	Low profile FineLine BGA, Option 2 – Wirebond	256
	FineLine BGA, Option 3– Wirebond	484
EP2C35	FineLine BGA, Option 3 – Wirebond	484
	Ultra FineLine BGA – Wirebond	484
	FineLine BGA, Option 3 – Wirebond	672
EP2C50	FineLine BGA, Option 3 – Wirebond	484
	Ultra FineLine BGA – Wirebond	484
	FineLine BGA, Option 3 – Wirebond	672
EP2C70	FineLine BGA, Option 3 – Wirebond	672
	FineLine BGA – Wirebond	896