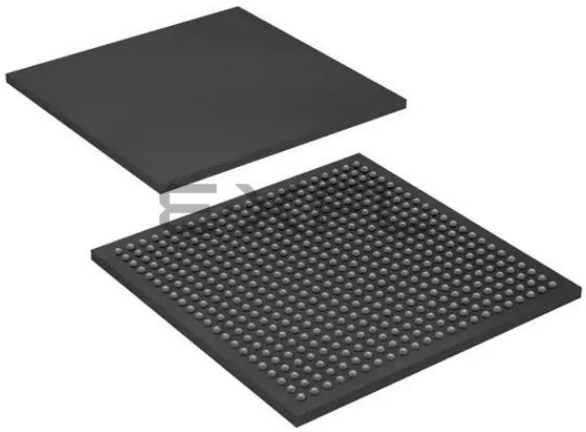

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Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	322
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35u484c7

Contents

Referenced Documents

This chapter references the following documents:

- *Hot Socketing & Power-On Reset* chapter in *Cyclone II Device Handbook*
- *Automotive-Grade Device Handbook*

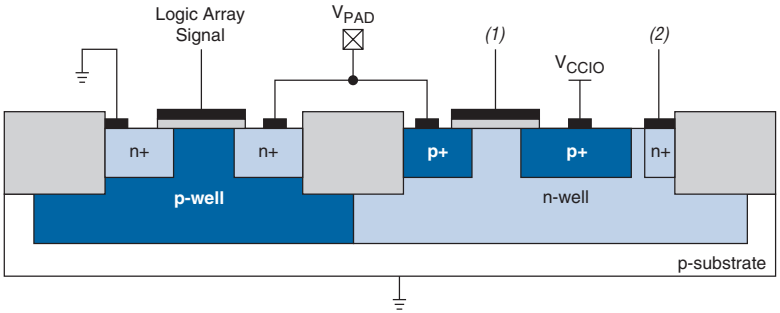
Document Revision History

Table 1–5 shows the revision history for this document.

Table 1–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v3.2	• Added "Referenced Documents". • Updated "Features" section and Table 1–1, Table 1–2, and Table 1–4 with information about EP2C5A.	—
February 2007 v3.1	• Added document revision history. • Added new *Note (2)* to Table 1–2.	Note to explain difference between I/O pin count information provided in Table 1–2 and in the Quartus II software documentation.
November 2005 v2.1	• Updated Introduction and Features. • Updated Table 1–3.	—
July 2005 v2.0	• Updated technical content throughout. • Updated Table 1–2. • Added Tables 1–3 and 1–4.	—
November 2004 v1.1	• Updated Table 1–2. • Updated bullet list in the "Features" section.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Figure 4–2. Transistor Level Diagram of FPGA Device I/O Buffers



Notes to Figure 4–2:
(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.
(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

Cyclone II devices contain POR circuitry to keep the device in a reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT} voltage levels and tri-states all user I/O pins until the V_{CC} reaches the recommended operating levels. In addition, the POR circuitry also monitors the V_{CCIO} level of the two I/O banks that contains configuration pins (I/O banks 1 and 3 for EP2C5 and EP2C8, I/O banks 2 and 6 for EP2C15A, EP2C20, EP2C35, EP2C50, and EP2C70) and tri-states all user I/O pins until the V_{CC} reaches the recommended operating levels.

After the Cyclone II device enters user mode, the POR circuit continues to monitor the V_{CCINT} voltage level so that a brown-out condition during user mode can be detected. If the V_{CCINT} voltage sags below the POR trip point during user mode, the POR circuit resets the device. If the V_{CCIO} voltage sags during user mode, the POR circuit does not reset the device.

"Wake-up" Time for Cyclone II Devices

In some applications, it may be necessary for a device to wake up very quickly in order to begin operation. The Cyclone II device family offers the Fast-On feature to support fast wake-up time applications. Devices that support the Fast-On feature are designated with an "A" in the ordering code and have stricter power up requirements compared to non-A devices.

Table 5–7. DC Characteristics of User I/O Pins Using Single-Ended Standards Notes (1), (2) **(Part 2 of 2)**

I/O Standard	Test Conditions		Voltage Thresholds	
	I_{OL} (mA)	I_{OH} (mA)	Maximum V_{OL} (V)	Minimum V_{OH} (V)
1.5-V HSTL class I	8	–8	0.4	V_{CCIO} – 0.4
1.5V HSTL class II	16	–16	0.4	V_{CCIO} – 0.4

Notes to Table 5–7:

(1) The values in this table are based on the conditions listed in Tables 5–2 and 5–6.

(2) This specification is supported across all the programmable drive settings available as shown in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

Differential I/O Standards

The RSDS and mini-LVDS I/O standards are only supported on output pins. The LVDS I/O standard is supported on both receiver input pins and transmitter output pins.

For more information on how these differential I/O standards are implemented, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook*.

Figure 5–1 shows the receiver input waveforms for all differential I/O standards (LVDS, LVPECL, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 4 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.8V_HSTL_ CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_HSTL_ CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
1.5V_HSTL_ CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 3 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_18_ CLASS_II	16 mA	260	220	180	—	—	—	—	—	—
	18 mA	270	220	180	—	—	—	—	—	—
1.8V_HSTL_ CLASS_I	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	320	270	220	320	270	220	320	270	220
1.8V_HSTL_ CLASS_II	16 mA	230	190	160	—	—	—	—	—	—
	18 mA	240	200	160	—	—	—	—	—	—
	20 mA	250	210	170	—	—	—	—	—	—
1.5V_HSTL_ CLASS_I	8 mA	210	170	140	210	170	140	210	170	140
	10 mA	220	180	150	—	—	—	—	—	—
	12 mA	230	190	160	—	—	—	—	—	—
1.5V_HSTL_ CLASS_II	16 mA	210	170	140	—	—	—	—	—	—
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
DIFFERENTIAL_ SSTL_18_CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—
DIFFERENTIAL_SSTL _18_CLASS_II	16 mA	260	220	180	—	—	—	—	—	—
	18 mA	270	220	180	—	—	—	—	—	—
1.8V_ DIFFERENTIAL_HSTL _CLASS_I	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	320	270	220	320	270	220	320	270	220
1.8V_ DIFFERENTIAL_HSTL _CLASS_II	16 mA	230	190	160	—	—	—	—	—	—
	18 mA	240	200	160	—	—	—	—	—	—
	20 mA	250	210	170	—	—	—	—	—	—

Table 5–57. Maximum for DDIO Output on Row Pins with PLL in the Clock Path Notes (1), (2) (Part 2 of 2)

Row Pins with PLL in the Clock Path	C6	C7	C8	Unit
1.5-V	280	280	280	ps
SSTL-2 Class I	150	190	230	ps
SSTL-2 Class II	155	200	230	ps
SSTL-18 Class I	180	240	260	ps
HSTL-18 Class I	180	235	235	ps
HSTL-15 Class I	205	220	220	ps
Differential SSTL-2 Class I	150	190	230	ps
Differential SSTL-2 Class II	155	200	230	ps
Differential SSTL-18 Class I	180	240	260	ps
Differential HSTL-18 Class I	180	235	235	ps
Differential HSTL-15 Class I	205	220	220	ps
LVDS	95	110	120	ps
Simple RSDS	100	155	155	ps
Mini LVDS	95	110	120	ps
PCI	285	305	335	ps
PCI-X	285	305	335	ps

Notes to Table 5–57:

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

For DDIO outputs, you can calculate actual half period from the following equation:

Actual half period = ideal half period – maximum DCD

For example, if the DDR output I/O standard is SSTL-2 Class II, the maximum DCD for a –5 device is 155 ps (refer to Table 5–57). If the clock frequency is 167 MHz, the half-clock period T/2 is:

T/2 = 1/(2* f)= 1 /(2*167 MHz) = 3 ns = 3000 ps

In ×8 and ×16 modes, one DQS pin drives up to 8 or 16 DQ pins, respectively, within the group. In the ×9 and ×18 modes, a pair of DQS pins (CQ and CQ#) drives up to 9 or 18 DQ pins within the group to support one or two parity bits and the corresponding data bits. If the parity bits or any data bits are not used, the extra DQ pins can be used as regular user I/O pins. The ×9 and ×18 modes are used to support the QDRII memory interface. Table 9–2 shows the number of DQS/DQ groups supported in each Cyclone II density/package combination.

Table 9–2. Cyclone II DQS & DQ Bus Mode Support *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups *(5)*, *(6)*	Number of ×16 Groups	Number of ×18 Groups *(5)*, *(6)*
EP2C5	144-pin TQFP *(2)*	3	3	0	0
	208-pin PQFP	7 *(3)*	4	3	3
	256-pin FineLine BGA	8 *(3)*	4 *(7)*	4	4 *(7)*
EP2C8	144-pin TQFP *(2)*	3	3	0	0
	208-pin PQFP	7 *(3)*	4 *(7)*	3	3
	256-pin FineLine BGA®	8 *(3)*	4 *(7)*	4	4 *(7)*
EP2C15	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
EP2C20	240-pin PQFP	8	4	4	4
	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
EP2C35	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
EP2C50	484-pin FineLine BGA	16 *(4)*	8 *(8)*	8	8 *(8)*
	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
EP2C70	672-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*
	896-pin FineLine BGA	20 *(4)*	8 *(8)*	8	8 *(8)*

Notes to Table 9–2:

(1) Numbers are preliminary.
(2) EP2C5 and EP2C8 devices in the 144-pin TQFP package do not have any DQ pin groups in I/O bank 1.
(3) Because of available clock resources, only a total of 6 DQ/DQS groups can be implemented.
(4) Because of available clock resources, only a total of 14 DQ/DQS groups can be implemented.
(5) The ×9 DQS/DQ groups are also used as ×8 DQS/DQ groups. The ×18 DQS/DQ groups are also used as ×16 DQS/DQ groups.
(6) For QDRII implementation, if you connect the D ports (write data) to the Cyclone II DQ pins, the total available ×9 DQS /DQ and ×18 DQS/DQ groups are half of that shown in Table 9–2.
(7) Because of available clock resources, only a total of 3 DQ/DQS groups can be implemented.
(8) Because of available clock resources, only a total of 7 DQ/DQS groups can be implemented.

For example, to implement a 72-bit wide SDRAM memory interface in Cyclone II devices, use 5 DQS/DQ groups in the top I/O bank and 4 DQS/DQ groups in the bottom I/O bank, or vice-versa. In this case, if DQS0T or DQS1T is used for the fifth DQS signal, the DQS2R or DQS2L pins become regular I/O pins and are unavailable for DQS signals in memory interface. For detailed information about the global clock network, refer to the *Global Clock Network & Phase Locked Loops* section in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

You must configure the DQ and DQS pins as bidirectional DDR pins on all the I/O banks of the device. Use the `altdq` and `altdqs` megafunctions to configure the DQ and DQS paths, respectively. If you only want to use the DQ or DQS pins as inputs, for instance in the QDRII memory interface where DQ and DQS are unidirectional read data and read clock, set the output enable of the DQ or DQS pins to ground. For further information, please refer to the section "QDRII SRAM" on page 9–5 of this handbook.

Clock, Command & Address Pins

You can use any of the user I/O pins on all the I/O banks (that support the external memory's I/O standard) of the device to generate clocks and command and address signals to the memory device.

Parity, DM & ECC Pins

You can use any of the DQ pins for the parity pins in Cyclone II devices. Cyclone II devices support parity in the ×8/×9 and ×16/×18 modes. There is one parity bit available per 8 bits of data pins.

The data mask (DM) pins are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pin indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. In Cyclone II devices, the DM pins are pre-assigned in the device pin outs, and these are the preferred pins. Each group of DQS and DQ signals requires a DM pin. Similar to the DQ output signals, the DM signals are clocked by the –90° shifted clock.

Some DDR SDRAM and DDR2 SDRAM devices support error correction coding (ECC) or parity. Parity bit checking is a way to detect errors, but it has no correction capabilities. ECC can detect and automatically correct errors in data transmission. In 72-bit DDR SDRAM, there are 8 ECC pins on top of the 64 data pins. Connect the DDR and DDR2 SDRAM ECC pins to a Cyclone II device's DQS/DQ group. The memory controller needs extra logic to encode and decode the ECC data.

- Cyclone II FPGA (EP2C15 or larger)
- Altera PCI Express Compiler ×1 MegaCore® function
- External PCI Express transceiver/PHY

2.5-V LVTTL (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVTTL.

2.5-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVCMOS.

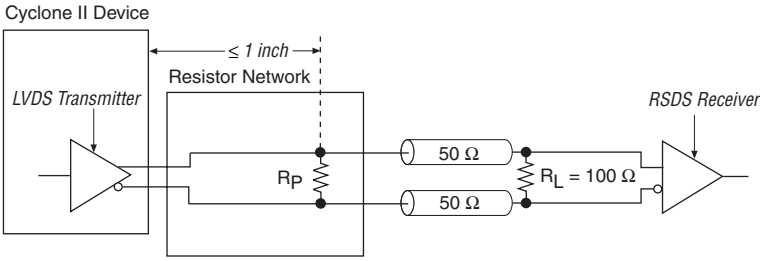
SSTL-2 Class I and II (EIA/JEDEC Standard JESD8-9A)

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operations in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of $-0.3\ V \leq V_I \leq V_{CCIO} + 0.3\ V$. SSTL-2 requires a V_{REF} value of 1.25 V and a V_{TT} value of 1.25 V connected to the termination resistors (refer to Figures 10–1 and 10–2).

Designing with RSDS

Cyclone II devices support the RSDS output standard using the LVDS I/O buffer types. For transmitters, the LVDS output buffer can be used with the external resistor network shown in Figure 11–7.

Figure 11–7. RSDS Resistor Network *Note (1)*



Note to Figure 11–7:
(1) R_S = 120 Ω and R_P = 170 Ω

For more information on the RSDS I/O standard, see the RSDS specification from the National Semiconductor web site **(www.national.com)**.

A resistor network is required to attenuate the LVDS output voltage swing to meet the RSDS specifications. The resistor network values can be modified to reduce power or improve the noise margin. The resistor values chosen should satisfy the following equation:

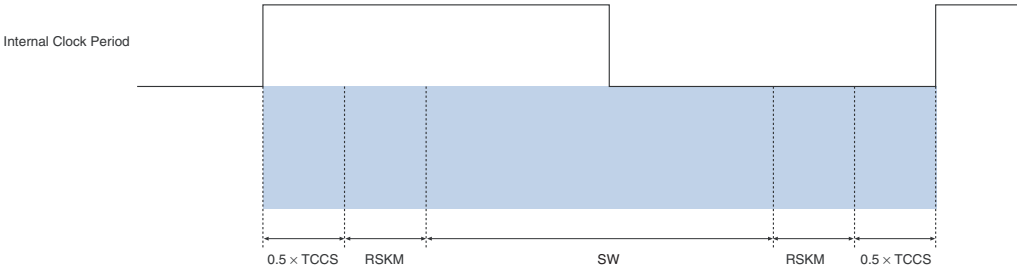
$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\,\Omega$$

Additional simulations using the IBIS models should be performed to validate that custom resistor values meet the RSDS requirements.

Single Resistor RSDS Solution

The external single resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. To transmit the RSDS signal, an external resistor (R_P) is connected in parallel between the two adjacent I/O pins on the board as shown in Figure 11–8. The recommended value of the resistor R_P is 100 Ω

Figure 11–17. Cyclone II High-Speed I/O Timing Budget *Note (1)*



Note to Figure 11–17:
(1) The equation for the high-speed I/O timing budget is: Period = 0.5/TCCS + RSKM + SW + RSKM + 0.5/TCCS.

Design Guidelines

This section provides guidelines for designing with Cyclone II devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pins in relation to differential pads.

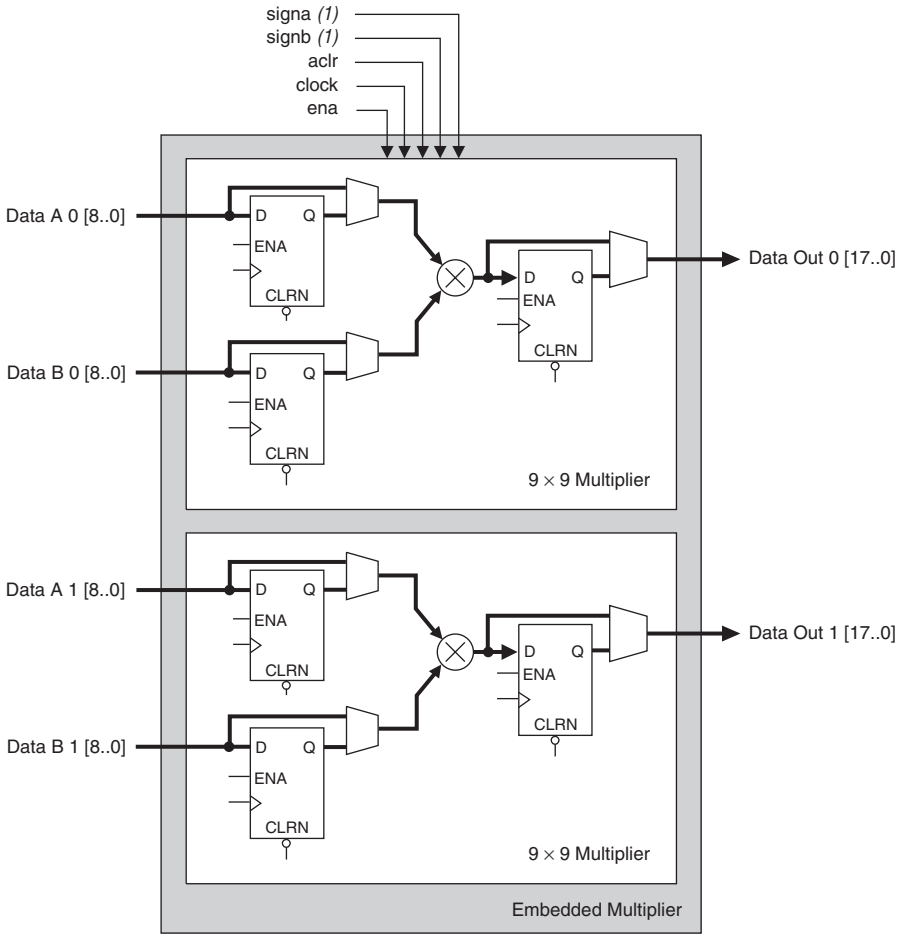
See the guidelines in the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook* for placing single-ended pads with respect to differential pads in Cyclone II devices.

Board Design Considerations

This section explains how to get the optimal performance from the Cyclone II I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. The critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques must be considered to get the best performance from the IC. The Cyclone II device generates signals that travel over the media at frequencies as high as 805 Mbps. Use the following general guidelines for improved signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.

Figure 12–4. 9-Bit Multiplier Mode



Note to Figure 12–4:
(1) If necessary, you can send these signals through one register to match the data signal path.

All 9-bit multiplier inputs and results can be independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Each embedded multiplier only has one `signa` signal to control the sign representation of both data A inputs (one for each 9 × 9 multiplier) and one `signb` signal to control the sign representation of both data B inputs. Therefore, all of the data A inputs feeding the same embedded multiplier must have the same sign representation. Similarly, all of the data B inputs feeding the same embedded multiplier must have the same sign representation.

Table 13–1. Cyclone II Configuration Schemes		
Configuration Scheme	**MSEL1**	**MSEL0**
AS (20 MHz)	0	0
PS	0	1
Fast AS (40 MHz) *(1)*	1	0
JTAG-based Configuration *(2)*	*(3)*	*(3)*

Notes to Table 13–1:

(1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

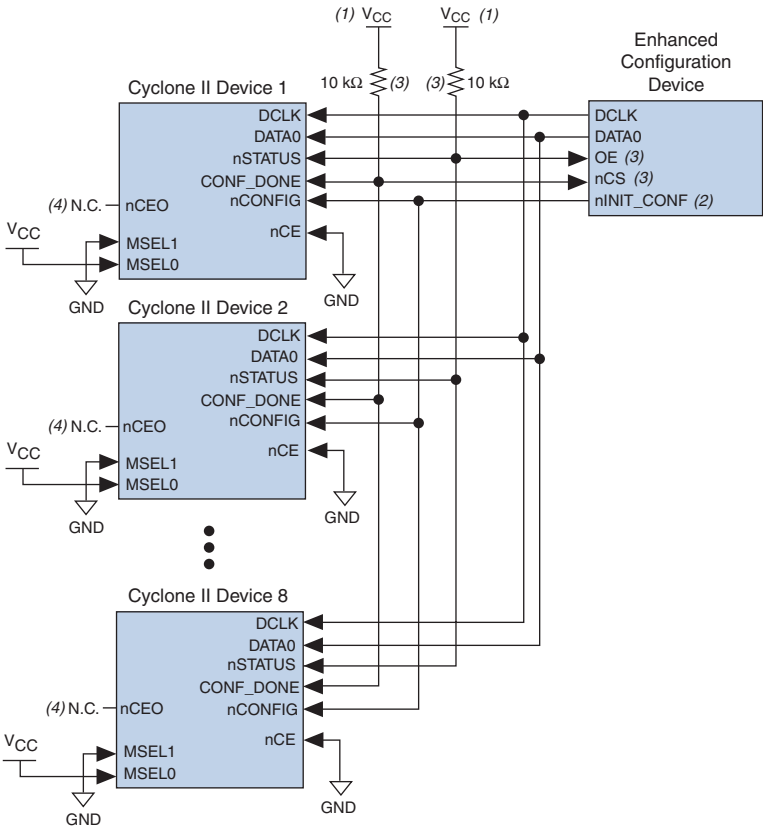
(2) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

(3) Do not leave the MSEL pins floating; connect them to V_{CCIO} or ground. These pins support the non-JTAG configuration scheme used in production. If you are only using JTAG configuration, you should connect the MSEL pins to ground.

You can download configuration data to Cyclone II FPGAs with the AS, PS, or JTAG interfaces using the options in Table 13–2.

Table 13–2. Cyclone II Device Configuration Schemes	
Configuration Scheme	**Description**
AS configuration	Configuration using serial configuration devices (EPCS1, EPCS4, EPCS16 or EPCS64 devices)
PS configuration	Configuration using enhanced configuration devices (EPC4, EPC8, and EPC16 devices), EPC2 and EPC1 configuration devices, an intelligent host (microprocessor), or a download cable
JTAG-based configuration	Configuration via JTAG pins using a download cable, an intelligent host (microprocessor), or the Jam™ Standard Test and Programming Language (STAPL)

Figure 13–16. Multiple Device PS Configuration Using an Enhanced Configuration Device When FPGAs Receive the Same Data



Notes to Figure 13–16:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

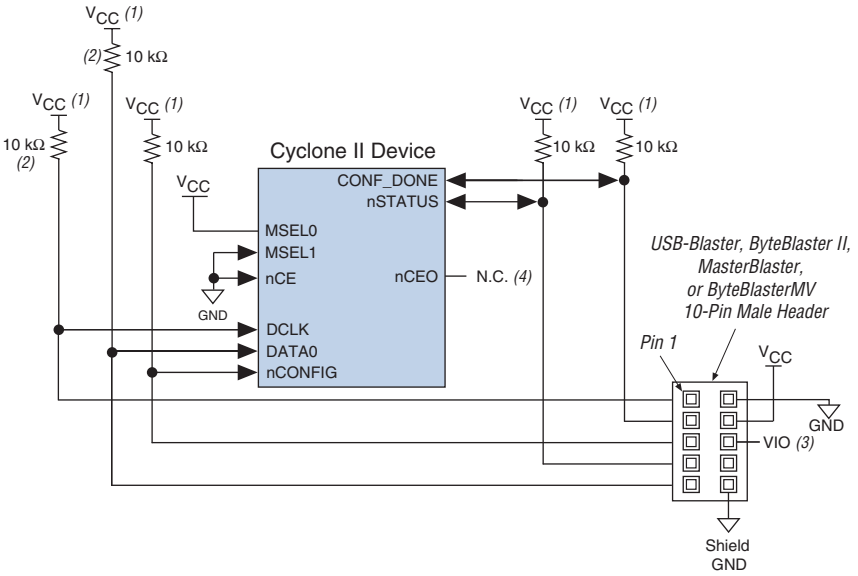
(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

You can cascade several EPC2 or EPC1 devices to configure multiple Cyclone II devices. The first configuration device in the chain is the master configuration device, and the subsequent devices are the slave devices. The master configuration device sends DCLK to the Cyclone II

Quartus II programmer and a download cable. Figure 13–19 shows the PS configuration for Cyclone II devices using a USB-Blaster, MasterBlaster, ByteBlaster II or ByteBlasterMV cable.

Figure 13–19. PS Configuration Using a USB-Blaster, MasterBlaster, ByteBlaster II or ByteBlasterMV Cable



Notes to Figure 13–19:

(1) The pull-up resistor should be connected to the same supply voltage as the USB-Blaster, MasterBlaster (VIO pin), ByteBlaster II, or ByteBlasterMV cable.

(2) The pull-up resistors on DATA0 and DCLK are only needed if the download cable is the only configuration scheme used on your board. This is to ensure that DATA0 and DCLK are not left floating after configuration. For example, if you are also using a configuration device, the pull-up resistors on DATA0 and DCLK are not needed.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

You can use a download cable to configure multiple Cyclone II devices by connecting each device's nCEO pin to the subsequent device's nCE pin. Connect the first Cyclone II device's nCE pin to GND and connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO pin high to V_{CCIO} when it feeds next device's nCE pin. Connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) on every device in the chain together. Because all CONF_DONE pins are connected, all devices in the chain initialize and enter user mode at the same time.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the nCEO pin inputs to the next device's nCE pin, make sure that the nCEO pin is not used as a user I/O pin after configuration.

Other Altera devices that have JTAG support can be placed in the same JTAG chain for device programming and configuration.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP). Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information on JTAG and Jam STAPL in embedded environments, see *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*. To download the Jam player, go to the Altera web site (**www.altera.com**).

Configuring Cyclone II FPGAs with JRunner

JRunner is a software driver that allows you to configure Cyclone II devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in **.rbf** format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

The RBF file used by the JRunner software driver can not be a compressed RBF file because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

For more information on the JRunner software driver, see *JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site.

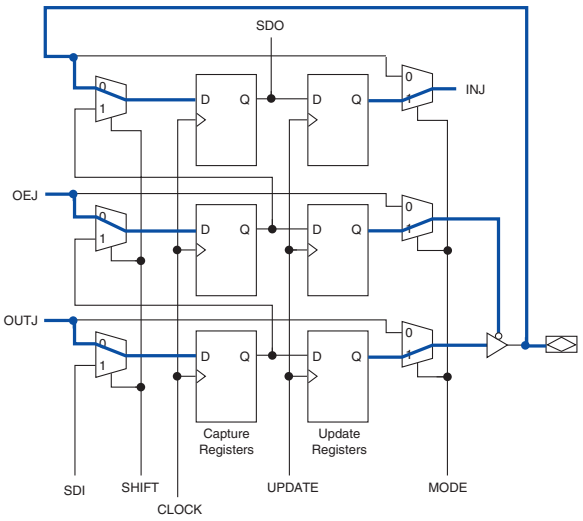
Figure 14–10 shows the capture, shift, and update phases of the EXTEST mode.

Figure 14–10. IEEE Std. 1149.1 BST EXTEST Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals are supplied by the TAP controller's CLOCKDR output. Previously retained data in the update registers drive the PIN_IN, INJ, and allows the I/O pin to tri-state or drive a signal out.

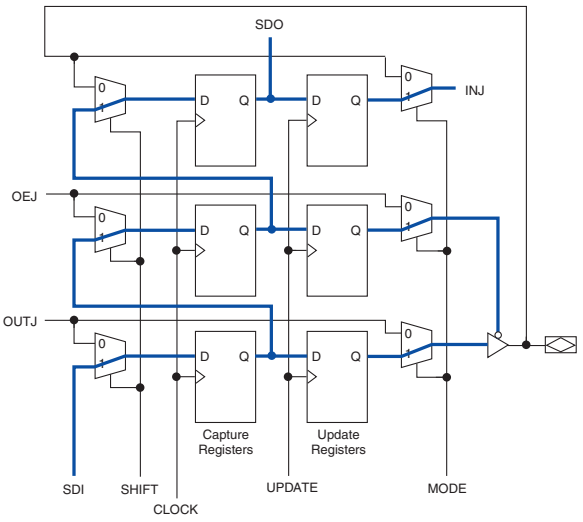
A "1" in the OEJ update register tri-states the output buffer.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

In the update phase, data is transferred from the capture registers to the update registers using the UPDATE clock. The update registers then drive the PIN_IN, INJ, and allow the I/O pin to tri-state or drive a signal out.



208-Pin Plastic Quad Flat Pack (PQFP) – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin 1 may be indicated by an ID dot in its proximity on package surface.

Tables 15–7 and 15–8 show the package information and package outline figure references, respectively, for the 208-pin PQFP package.

Table 15–7. 208-Pin PQFP Package Information

Description	Specification
Ordering code reference	Q
Package acronym	PQFP
Lead material	Copper
Lead finish (plating)	Regular: 85Sn:15Pb (Typ.) Pb-free: Matte Sn
JEDEC Outline Reference	MS-029 Variation: FA-1
Maximum lead coplanarity	0.003 inches (0.08 mm)
Weight	5.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–8. 208-Pin PQFP Package Outline Dimensions (Part 1 of 2)

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	4.10
A1	0.25	–	0.50
A2	3.20	3.40	3.60
D	30.60 BSC		
D1	28.00 BSC		
E	30.60 BSC		
E1	28.00 BSC		
L	0.50	0.60	0.75
L1	1.30 REF		
S	0.20	–	–
b	0.17	–	0.27
c	0.09	–	0.20

Figure 15–4 shows a 256-pin FineLine BGA package outline.

Figure 15–4. 256-Pin FineLine BGA Package Outline