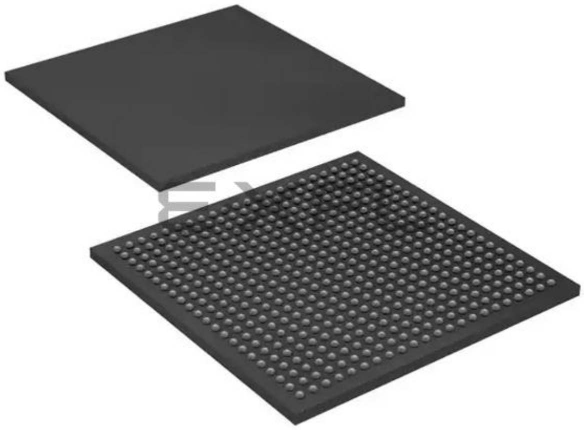
Intel - EP2C35U484C8N Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	322
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35u484c8n

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC Characteristics and Timing Specifications

Memory Modes

Table 2–7 summarizes the different memory modes supported by the M4K memory blocks.

Table 2–7. M4K Memory Modes

Memory Mode	Description
Single-port memory	M4K blocks support single-port mode, used when simultaneous reads and writes are not required. Single-port memory supports non-simultaneous reads and writes.
Simple dual-port memory	Simple dual-port memory supports a simultaneous read and write.
Simple dual-port with mixed width	Simple dual-port memory mode with different read and write port widths.
True dual-port memory	True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies.
True dual-port with mixed width	True dual-port mode with different read and write port widths.
Embedded shift register	M4K memory blocks are used to implement shift registers. Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock.
ROM	The M4K memory blocks support ROM mode. A MIF initializes the ROM contents of these blocks.
FIFO buffers	A single clock or dual clock FIFO may be implemented in the M4K blocks. Simultaneous read and write from an empty FIFO buffer is not supported.

☞ Embedded Memory can be inferred in your HDL code or directly instantiated in the Quartus II software using the MegaWizard® Plug-in Manager Memory Compiler feature.

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes

Clock Mode	Description
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`.
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

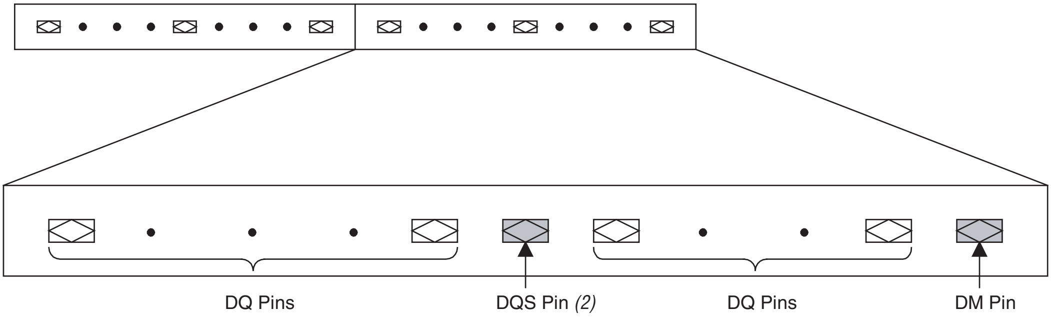
Table 2–9. Cyclone II M4K Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Figure 2–26. Cyclone II Device DQ & DQS Groups in ×8/×9 Mode Notes (1), (2)



Notes to Figure 2–26:

(1) Each DQ group consists of a DQS pin, DM pin, and up to nine DQ pins.

(2) This is an idealized pin layout. For actual pin layout, refer to the pin table.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR and DDR2 SDRAM. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. The dedicated external memory interface in Cyclone II devices also includes programmable delay circuitry that can shift the incoming DQS signals to center align the DQS signals within the data window.

The DQS signal is usually associated with a group of data (DQ) pins. The phase-shifted DQS signals drive the global clock network, which is used to clock the DQ signals on internal LE registers.

Table 2–15 shows the number of DQ pin groups per device.

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 1 of 2) Note (1)

Device	Package	Number of ×8 Groups	Number of ×9 Groups (5), (6)	Number of ×16 Groups	Number of ×18 Groups (5), (6)
EP2C5	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
EP2C8	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
	256-pin FineLine BGA®	8 (3)	4	4	4
EP2C15	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8
EP2C20	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8

Table 5–48. RSDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max (1)	Min	Typ	Max (1)	Min	Typ	Max (1)	
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	80–20%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	—	—		100	—		100	—	—	100	µs

Note to Table 5–48:

(1) These specifications are for a three-resistor RSDS implementation. For single-resistor RSDS in ×10 through ×2 modes, the maximum data rate is 170 Mbps and the corresponding maximum input clock frequency is 85 MHz. For single-resistor RSDS in ×1 mode, the maximum data rate is 170 Mbps, and the maximum input clock frequency is 170 MHz. For more information about the different RSDS implementations, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the Cyclone II Device Handbook.

In order to determine the transmitter timing requirements, RSDS receiver timing requirements on the other end of the link must be taken into consideration. RSDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for RSDS are shown in Figure 5–5.

6. Reference & Ordering Information

CII51006-1.4

Software

Cyclone® II devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Quartus II Handbook* for more information on the Quartus II software features.

The free Quartus II Web Edition software, available at **www.Altera.com**, supports Microsoft Windows XP and Windows 2000. The full version of Quartus II software is available through the Altera subscription program. The full version of Quartus II software supports all Altera devices, is available for Windows XP, Windows 2000, Sun Solaris, and Red Hat Linux operating systems, and includes a free suite of popular IP MegaCore® functions for DSP applications and interfacing to external memory devices. Quartus II software and Quartus II Web Edition software support seamless integration with your favorite third party EDA tools.

Device Pin-Outs

Device pin-outs for Cyclone II devices are available on the Altera web site (**www.altera.com**). For more information contact Altera Applications.

Ordering Information

Figure 6–1 describes the ordering codes for Cyclone II devices. For more information on a specific package, contact Altera Applications.

Table 7–5. PLL Output signals

Port	Description	Source	Destination
`c[2..0]`	PLL clock outputs driving the internal global clock network or external clock output pin (`PLL<#>_OUT`)	PLL post-scale counter	Global clock network or external I/O pin
Locked	Gives the status of the PLL lock. When the PLL is locked, this port drives V_{CC}. When the PLL is out of lock, this port drives GND. The locked port may pulse high and low during the PLL lock process.	PLL lock detect circuit	Logic array or output pin

Table 7–6 shows a list of I/O standards supported in Cyclone II device PLLs.

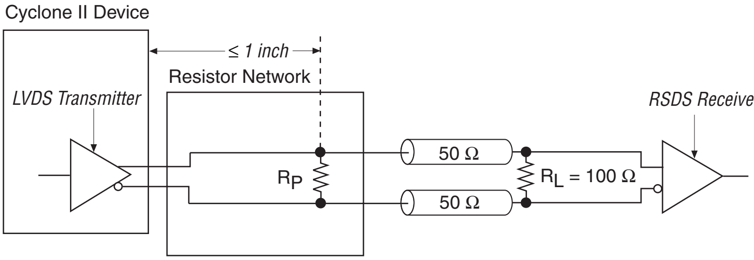
Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 1 of 2)

I/O Standard	Input	Output	
	inclk	lock	pll_out
LVTTL (3.3, 2.5, and 1.8 V)	✓	✓	✓
LVCMOS (3.3, 2.5, 1.8, and 1.5 V)	✓	✓	✓
3.3-V PCI	✓	✓	✓
3.3-V PCI-X *(1)*	✓	✓	✓
LVPECL	✓		
LVDS	✓	✓	✓
1.5 and 1.8 V differential HSTL class I and class II	✓		✓ *(2)*
1.8 and 2.5 V differential SSTL class I and class II	✓		✓ *(2)*
1.5-V HSTL class I	✓	✓	✓
1.5-V HSTL class II *(3)*	✓	✓	✓
1.8-V HSTL class I	✓	✓	✓
1.8-V HSTL class II *(3)*	✓	✓	✓
SSTL-18 class I	✓	✓	✓
SSTL-18 class II *(3)*	✓	✓	✓
SSTL-25 class I	✓	✓	✓

Single-Clock Mode

Cyclone II memory blocks support single-clock mode for true dual-port, simple dual-port, and single-port memory. In this mode, a single clock, together with a clock enable, controls all registers of the memory block. This mode does not support asynchronous clear signals for the registers. Figures 8–18 through 8–20 show the memory block in single-clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

Figure 11–8. RSDS Single Resistor Network *Note (1)*



Note to Figure 11–8:
(1) R_p = 100 Ω

RSDS Software Support

When designing for the RSDS I/O standard, assign the RSDS I/O standard to the I/O pins intended for RSDS in the Quartus® II software. Contact Altera Applications for reference designs.

mini-LVDS Standard Support in Cyclone II Devices

The mini-LVDS specification defines its use in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the Texas Instruments mini-LVDS Interface Specification and support the mini-LVDS output standard. Table 11–3 shows the mini-LVDS electrical characteristics for Cyclone II devices.

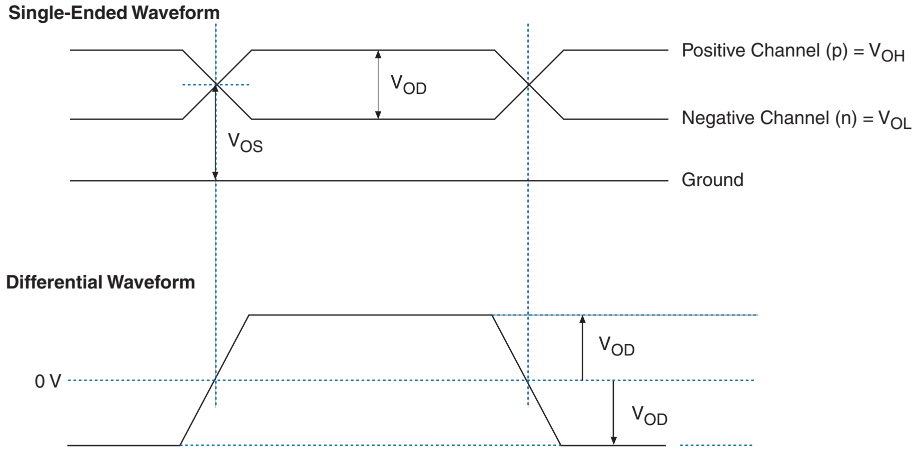
Table 11–3. mini-LVDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	300		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1125	1250	1375	mV
T_r / T_f	Transition time	20% to 80%			500	ps

Notes to Table 11–3:
(1) The V_{OD} specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

Figure 11–9 shows the mini-LVDS receiver and transmitter signal waveforms.

Figure 11–9. Transmitter Output Signal Level Waveforms for mini-LVDS Note (1)



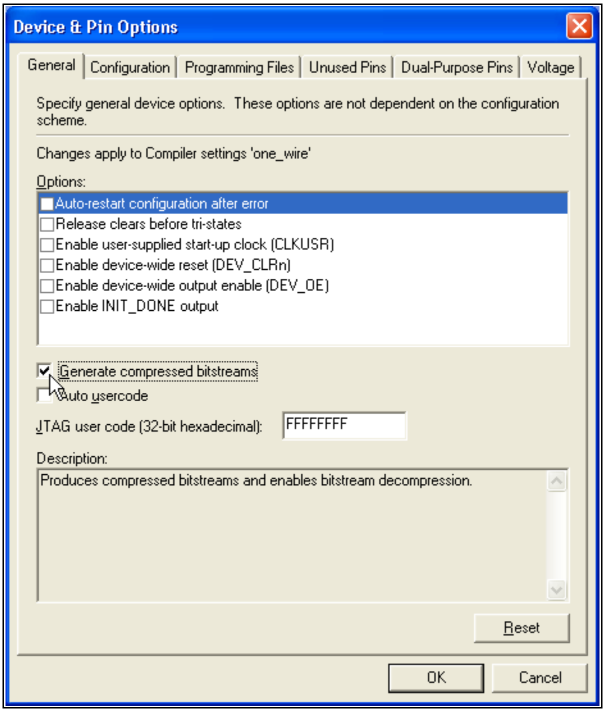
Note to Figure 11–9:

(1) The V_{OD} specifications apply at the resistor network output.

Designing with mini-LVDS

Similar to RSDS, Cyclone II devices support the mini-LVDS output standard using the LVDS I/O buffer types. For transmitters, the LVDS output buffer can be used with the external resistor network shown in Figure 11–10. The resistor values chosen should satisfy the equation on page 11-8.

Figure 13–1. Enabling Compression for Cyclone II Bitstreams in Compiler Settings



Specify general device options. These options are not dependent on the configuration scheme.

Changes apply to Compiler settings 'one_wire'

Options:

- ☐ Auto-restart configuration after error
- ☐ Release clears before tri-states
- ☐ Enable user-supplied start-up clock (CLKUSR)
- ☐ Enable device-wide reset (DEV_CLRn)
- ☐ Enable device-wide output enable (DEV_OE)
- ☐ Enable INIT_DONE output

☑ Generate compressed bitstreams

☐ Auto usercode

JTAG user code (32-bit hexadecimal): FFFFFFFF

Description:

Produces compressed bitstreams and enables bitstream decompression.

You can also use the following steps to enable compression when creating programming files from the Convert Programming Files window.

1. Click **Convert Programming Files** (File menu).
2. Select the Programming File type. Only Programmer Object Files (**.pof**), SRAM HEXOUT, RBF, or TTF files support compression.
3. For POFs, select a configuration device.
4. Select **Add File** and add a Cyclone II SRAM Object File(s) (**.sof**).
5. Select the name of the file you added to the SOF Data area and click on **Properties**.
6. Check the **Compression** check box.

Programming Serial Configuration Devices

Serial configuration devices are non-volatile, flash-memory-based devices. You can program these devices in-system using the USB-Blaster™ or ByteBlaster™ II download cable. Alternatively, you can program them using the Altera Programming Unit (APU), supported third-party programmers, or a microprocessor with the SRunner software driver.

You can use the AS programming interface to program serial configuration devices in-system. During in-system programming, the download cable disables FPGA access to the AS interface by driving the `nCE` pin high. Cyclone II devices are also held in reset by pulling the `nCONFIG` signal low. After programming is complete, the download cable releases the `nCE` and `nCONFIG` signals, allowing the pull-down and pull-up resistor to drive GND and V_{CC}, respectively. Figure 13–7 shows the download cable connections to the serial configuration device.

For more information on the USB-Blaster download cable, see the *USB-Blaster USB Port Download Cable Data Sheet*. For more information on the ByteBlaster II cable, see the *ByteBlaster II Download Cable Data Sheet*.

Configuration Stage

When the `nSTATUS` pin transitions high, the configuration device's `OE` pin also transitions high and the configuration device clocks data out serially to the FPGA using its internal oscillator. The Cyclone II device receives configuration data on its `DATA0` pin and the clock is received on the `DCLK` pin. Data is latched into the FPGA on the rising edge of `DCLK`.

After the FPGA has received all configuration data successfully, it releases the open-drain `CONF_DONE` pin, which is pulled high by a pull-up resistor. Since the Cyclone II device's `CONF_DONE` pin is tied to the configuration device's `nCS` pin, the configuration device is disabled when `CONF_DONE` goes high. Enhanced configuration and EPC2 devices have an optional internal pull-up resistor on the `nCS` pin. You can turn this option on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you do not use this internal pull-up resistor, you need to connect an external 10-kΩ pull-up resistor to the `nCS` and `CONF_DONE` line. A low-to-high transition on `CONF_DONE` indicates configuration is complete, and the device can begin initialization.

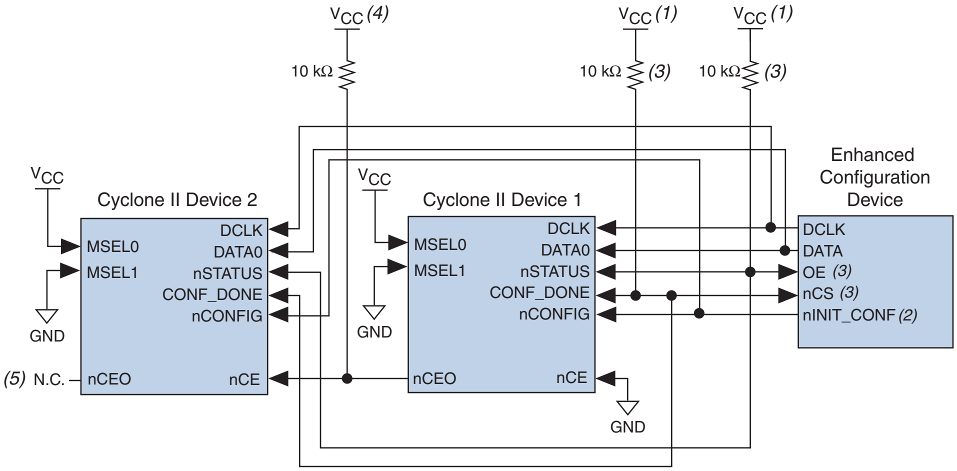
Initialization Stage

In Cyclone II devices, the default initialization clock source is the Cyclone II internal oscillator (typically 10 MHz). Cyclone II devices can also use the optional `CLKUSR` pin. If your design uses the internal oscillator, the Cyclone II device supplies itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to use another device or source to send additional clock cycles to the `CLKUSR` pin during the initialization stage. Additionally, you can use of the `CLKUSR` pin as a user I/O pin, which means you have an additional user I/O pin.

If you want to delay the initialization of the device, you can use the `CLKUSR` pin. Using the `CLKUSR` pin allows you to control when the Cyclone II device enters user mode. You can delay the Cyclone II devices from entering user mode for an indefinite amount of time. You can turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. Supplying a clock on `CLKUSR` does not affect the configuration process. After all configuration data is accepted and `CONF_DONE` goes high, Cyclone II devices require 299 clock cycles to properly initialize and support a `CLKUSR` f_{MAX} of 100 MHz.

An optional `INIT_DONE` pin is available, which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you use the `INIT_DONE` pin, an external 10-kΩ pull-up resistor pulls it high when

Figure 13–14. Multiple Device PS Configuration Using an Enhanced Configuration Device



Notes to Figure 13–14:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The `nINIT_CONF` pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the `nINIT_CONF` to `nCONFIG` line. The `nINIT_CONF` pin does not need to be connected if its functionality is not used. If `nINIT_CONF` is not used, `nCONFIG` must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' `OE` and `nCS` pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(4) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the `nCEO` pin resides in.

(5) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

You cannot cascade enhanced configuration devices (EPC16, EPC8, and EPC4 devices).

When configuring multiple devices, you must generate the configuration device's POF from each project's SOF. You can combine multiple SOFs using the **Convert Programming Files** window in the Quartus II software.

For more information on how to create configuration files for multiple device configuration chains, see the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

When configuring multiple devices with the PS scheme, connect the first Cyclone II device's `nCE` pin to GND and connect its `nCEO` pin to the `nCE` pin of the Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's `nCEO` pin to the V_{CCIO} level when

Table 13–12 describes the optional configuration pins. If these optional configuration pins are not enabled in the Quartus II software, they are available as general-purpose user I/O pins. Therefore during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 13–12. Optional Configuration Pins

Pin Name	User Mode	Pin Type	Description
`CLKUSR`	N/A if option is on. I/O if option is off.	Input	This is an optional user-supplied clock input that synchronizes the initialization of one or more devices. This pin is enabled by turning on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software
`INIT_DONE`	N/A if option is on. I/O if option is off.	Output open-drain	This is a status pin that can be used to indicate when the device has initialized and is in user mode. When `nCONFIG` is low and during the beginning of configuration, the `INIT_DONE` pin is tri-stated and pulled high due to an external 10-kΩ pull-up resistor. Once the option bit to enable `INIT_DONE` is programmed into the device (during the first frame of configuration data), the `INIT_DONE` pin goes low. When initialization is complete, the `INIT_DONE` pin is released and pulled high and the FPGA enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the **Enable INIT_DONE output** option in the Quartus II software.
`DEV_OE`	N/A if option is on. I/O if option is off.	Input	Optional pin that allows the user to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated. When this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the **Enable device-wide output enable (DEV_OE)** option in the Quartus II software.
`DEV_CLRn`	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared. When this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the **Enable device-wide reset (DEV_CLRn)** option in the Quartus II software.

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Document Revision History

Table 14–4 shows the revision history for this document.

Table 14–4. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.1	- Added document revision history. - Added new section "BST for Configured Devices".	- Added infomation about 'Always Enable Input Buffer' option.
July 2005 v2.0	Moved the "JTAG Timing Specifications" section to the *DC Characteristics & Timing Specifications* chapter.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

208-Pin Plastic Quad Flat Pack (PQFP) – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin 1 may be indicated by an ID dot in its proximity on package surface.

Tables 15–7 and 15–8 show the package information and package outline figure references, respectively, for the 208-pin PQFP package.

Table 15–7. 208-Pin PQFP Package Information

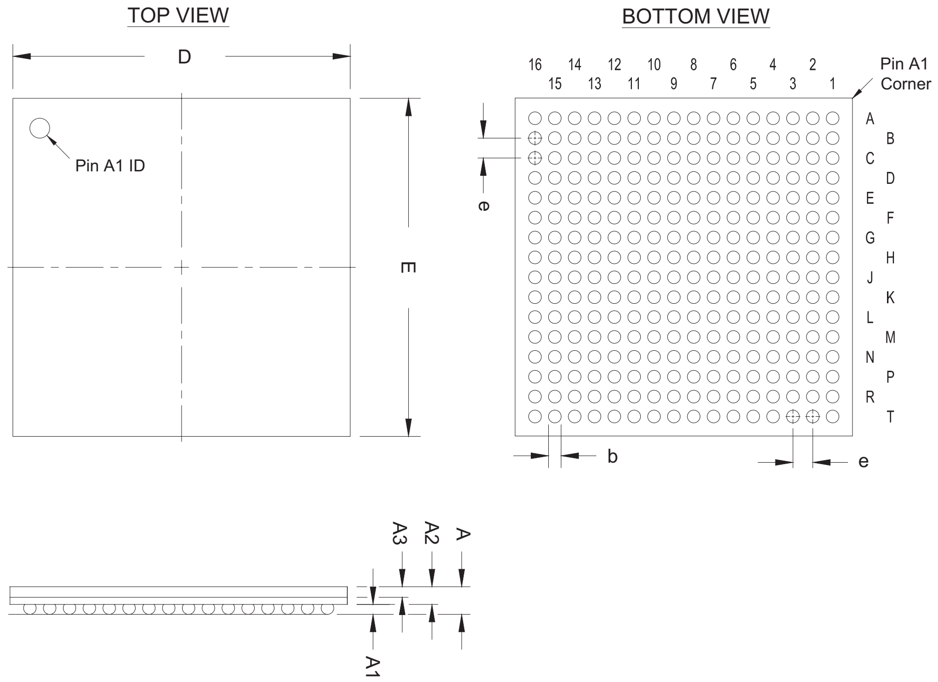
Description	Specification
Ordering code reference	Q
Package acronym	PQFP
Lead material	Copper
Lead finish (plating)	Regular: 85Sn:15Pb (Typ.) Pb-free: Matte Sn
JEDEC Outline Reference	MS-029 Variation: FA-1
Maximum lead coplanarity	0.003 inches (0.08 mm)
Weight	5.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–8. 208-Pin PQFP Package Outline Dimensions (Part 1 of 2)

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	4.10
A1	0.25	–	0.50
A2	3.20	3.40	3.60
D	30.60 BSC		
D1	28.00 BSC		
E	30.60 BSC		
E1	28.00 BSC		
L	0.50	0.60	0.75
L1	1.30 REF		
S	0.20	–	–
b	0.17	–	0.27
c	0.09	–	0.20

Figure 15–4 shows a 256-pin FineLine BGA package outline.

Figure 15–4. 256-Pin FineLine BGA Package Outline



672-Pin FineLine BGA Package, Option 3 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

Tables 15–17 and 15–18 show the package information and package outline figure references, respectively, for the 672-pin FineLine BGA package.

Table 15–17. 672-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAL-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	7.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–18. 672-Pin FineLine BGA Package Outline Dimensions

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	27.00 BSC		
E	27.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		