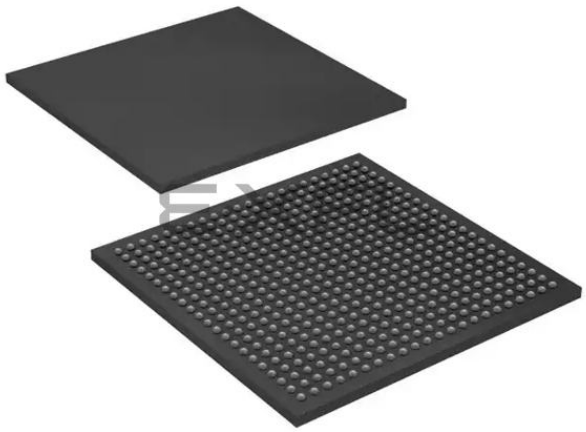

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Details	
Product Status	Active
Number of LABs/CLBs	2076
Number of Logic Elements/Cells	33216
Total RAM Bits	483840
Number of I/O	322
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c35u484i8

About This Handbook

This handbook provides comprehensive information about the Altera® Cyclone® II family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Altera literature services	Email	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

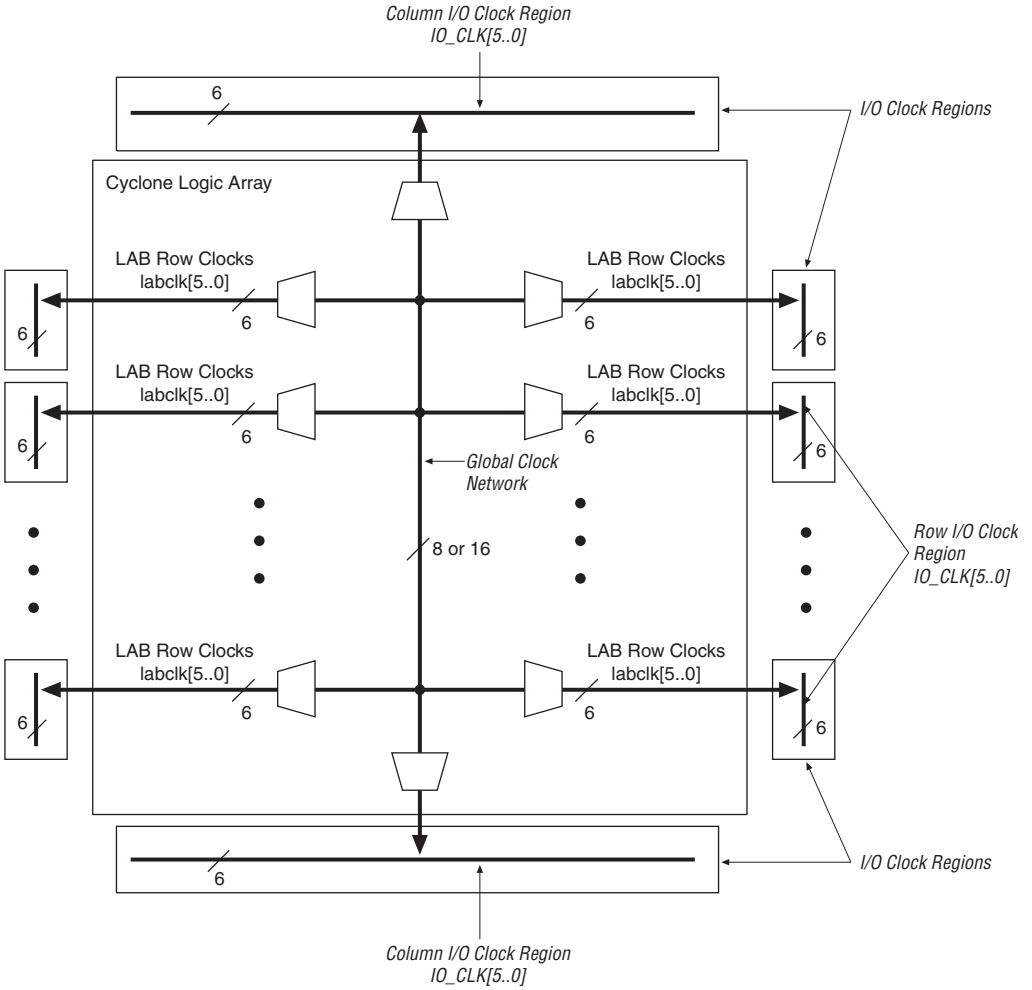
Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*

Figure 2–15. LAB & I/O Clock Regions



For more information on the global clock network and the clock control block, see the *PLLs in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Each M4K block can implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and first-in first-out (FIFO) buffers. The M4K blocks support the following features:

- 4,608 RAM bits
- 250-MHz performance
- True dual-port memory
- Simple dual-port memory
- Single-port memory
- Byte enable
- Parity bits
- Shift register
- FIFO buffer
- ROM
- Various clock modes
- Address clock enable

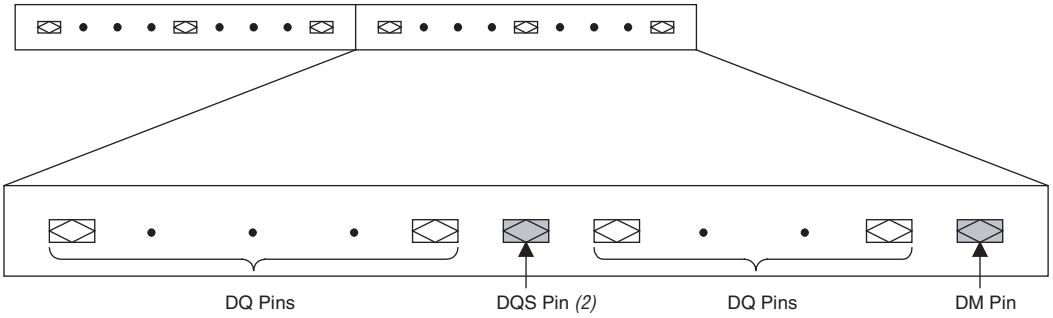
Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Table 2–5 shows the capacity and distribution of the M4K memory blocks in each Cyclone II device.

Table 2–5. M4K Memory Capacity & Distribution in Cyclone II Devices

Device	M4K Columns	M4K Blocks	Total RAM Bits
EP2C5	2	26	119,808
EP2C8	2	36	165,888
EP2C15	2	52	239,616
EP2C20	2	52	239,616
EP2C35	3	105	483,840
EP2C50	3	129	594,432
EP2C70	5	250	1,152,000

Figure 2–26. Cyclone II Device DQ & DQS Groups in ×8/×9 Mode *Notes (1), (2)*



Notes to Figure 2–26:
(1) Each DQ group consists of a DQS pin, DM pin, and up to nine DQ pins.
(2) This is an idealized pin layout. For actual pin layout, refer to the pin table.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR and DDR2 SDRAM. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. The dedicated external memory interface in Cyclone II devices also includes programmable delay circuitry that can shift the incoming DQS signals to center align the DQS signals within the data window.

The DQS signal is usually associated with a group of data (DQ) pins. The phase-shifted DQS signals drive the global clock network, which is used to clock the DQ signals on internal LE registers.

Table 2–15 shows the number of DQ pin groups per device.

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups (5), (6)	Number of ×16 Groups	Number of ×18 Groups (5), (6)
EP2C5	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
EP2C8	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
	256-pin FineLine BGA®	8 (3)	4	4	4
EP2C15	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8
EP2C20	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8

Document Revision History

Table 3–5 shows the revision history for this document.

Table 3–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	• Added document revision history. • Added new handpara nore in "IEEE Std. 1149.1 (JTAG) Boundary Scan Support" section. • Updated "Cyclone II Automated Single Event Upset Detection" section.	• Added information about limitation of cascading multi devices in the same JTAG chain. • Corrected information on CRC calculation.
July 2005 v2.0	Updated technical content.	
February 2005 v1.2	Updated information on JTAG chain limitations.	
November 2004 v1.1	Updated Table 3–4.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Table 5–27. EP2C20/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.337	–0.357	0.079	0.04	0.075	0.045	ns

Notes to Table 5–27:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–28. EP2C20/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.542	1.615	2.490	2.651	2.886	2.866	ns
t_{COUT}	1.544	1.617	2.506	2.664	2.894	2.874	ns
t_{PLLCIN}	–0.424	–0.448	–0.057	–0.107	–0.077	–0.107	ns
$t_{PLLCOUT}$	–0.422	–0.446	–0.041	–0.094	–0.069	–0.099	ns

Notes to Table 5–28:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C35 Clock Timing Parameters

Tables 5–29 and 5–30 show the clock timing parameters for EP2C35 devices.

Table 5–29. EP2C35 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.499	1.569	2.652	2.878	3.155	ns
t_{COUT}	1.513	1.584	2.686	2.910	3.184	ns
t_{PLLCIN}	–0.026	–0.032	0.272	0.316	0.41	ns
$t_{PLLCOUT}$	–0.012	–0.017	0.306	0.348	0.439	ns

Table 5–41. Cyclone II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.5V_HSTL_CLASS_II	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
1.8V_HSTL_CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_HSTL_CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
DIFFERENTIAL_SSTL_2_ CLASS_I	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
DIFFERENTIAL_SSTL_2_ CLASS_II	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
DIFFERENTIAL_SSTL_18_ CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
DIFFERENTIAL_SSTL_18_ CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
LVDS	t_{PI}	651	682	1036	1075	1113	1113	ps
	t_{PCOUT}	434	455	669	699	728	728	ps
PCI	t_{PI}	595	623	1113	1156	1232	1232	ps
	t_{PCOUT}	378	396	746	780	847	847	ps
PCI-X	t_{PI}	595	623	1113	1156	1232	1232	ps
	t_{PCOUT}	378	396	746	780	847	847	ps

Notes to Table 5–41 :

(1) These numbers are for commercial devices.

(2) These numbers are for automotive devices.

Each output port has a unique post-scale counter to divide down the high-frequency VCO. There are three post-scale counters (c0, c1, and c2), which range from 1 to 32. The following equations show the frequencies for the three post-scale counters:

$$f_{C0} = \frac{f_{VCO}}{C0} = f_{IN} \frac{m}{n \times C0}$$

$$f_{C1} = \frac{f_{VCO}}{C1} = f_{IN} \frac{m}{n \times C1}$$

$$f_{C2} = \frac{f_{VCO}}{C2} = f_{IN} \frac{m}{n \times C2}$$

All three output counters can drive the global clock network. The c2 output counter can also drive a dedicated external I/O pin (single ended or differential). This counter output can drive a dedicated external clock output pin (`PLL<#>_OUT`) and the global clock network at the same time.

For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets the VCO frequency specifications. Then, the post-scale counters scale down the VCO frequency for each PLL clock output port. For example, if clock output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least common multiple in the VCO's range).

Programmable Duty Cycle

The programmable duty cycle feature allows you to set the PLL clock output duty cycles. The duty cycle is the ratio of the clock output high and low time to the total clock cycle time, expressed as a percentage of high time. This feature is supported on all three PLL post-scale counters, c0, c1, and c2, and when using all clock feedback modes.

The duty cycle is set by using a low- and high-time count setting for the post-scale counters. The Quartus II software uses the input frequency and target multiply/divide ratio to select the post-scale counter. The granularity of the duty cycle is determined by the post-scale counter value chosen on a PLL clock output and is defined as 50% ÷ post-scale counter value. For example, if the post-scale counter value is 3, then the allowable duty cycle precision would be 50% ÷ 3 = 16.67%. Because the `altpll` megafunction does not accept non-integer values for the duty cycle values, the allowable duty cycles are 17% 33% 50% and 67%. For example, if the c0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

areset

The PLL areset signal is the reset and resynchronization input for each PLL. The areset signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL input and output clocks. You should include the areset signal in designs if any of the following conditions are true:

- Manual clock switchover is enabled in the design
- Phase relationships between input and output clocks need to be maintained after a loss of lock condition
- If the input clock to the PLL is not toggling or is unstable upon powerup, assert the areset signal after the input clock is toggling, staying within the input jitter specification

Altera recommends using the areset and locked signals in your designs to control and observe the status of your PLL.

The areset signal is an active high signal and, when driven high, the PLL counters reset, clearing the PLL output and causing the PLL to lose lock. The VCO is also set back to its nominal frequency. The clock outputs from the PLL are driven to ground as long as areset is active. When areset transitions low, the PLL resynchronizes to its input clock as the PLL relocks. If the target VCO frequency is below this nominal frequency, then the PLL clock output frequency starts at a higher value than desired during the lock process. In this case, Altera recommends monitoring the gated locked signal to ensure the PLL is fully in lock before enabling the clock outputs from the PLL. The Cyclone II device can drive this PLL input signal from LEs or any general-purpose I/O pin. The areset signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to GND.

pfdena

The pfdena signal is an active high signal that controls the PFD output in the PLL with a programmable gate. If you disable the PFD by transitioning pfdena low, the VCO operates at its last set control voltage and frequency value with some long-term drift to a lower frequency. Even though the PLL clock outputs continue to toggle regardless of the input clock, the PLL could lose lock. The system continues running when the PLL goes out of lock or if the input clock is disabled. By maintaining the current frequency, the system has time to store its current settings before shutting down. If the pfdena signal transitions high, the PLL relocks and resynchronizes to the input clock. The pfdena input signal can be driven by any general-purpose I/O pin or from LEs. This signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to V_{CC}.

locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals

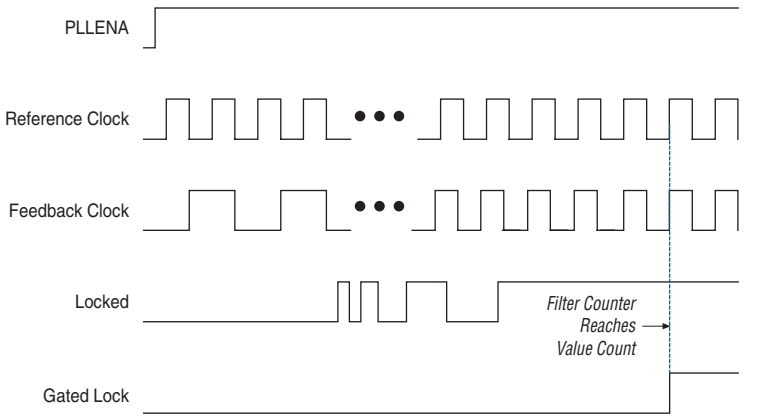
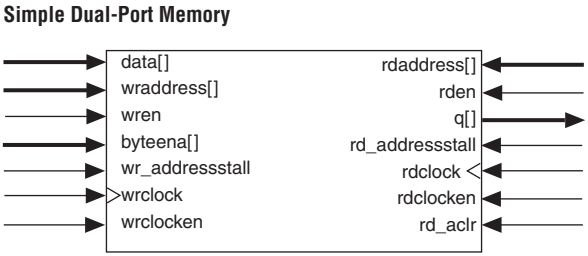


Figure 8–8. Cyclone II Simple Dual-Port Mode *Note (1)*



Note to Figure 8–8:
(1) Simple dual-port RAM supports input and output clock mode in addition to the read and write clock mode shown.

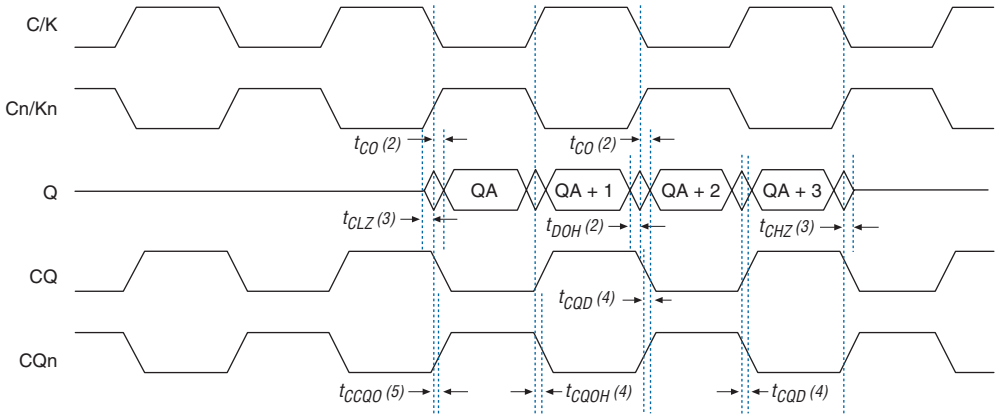
Cyclone II memory blocks support mixed-width configurations, allowing different read and write port widths. Tables 8–5 and 8–6 show the mixed-width configurations.

Table 8–5. Cyclone II Memory Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

In simple dual-port mode, the memory blocks have one write enable and one read enable signal. They do not support a clear port on the write enable and read enable registers. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is the old data stored at the memory

Figure 9–5. Data & Clock Relationship During a QDRII SRAM Report



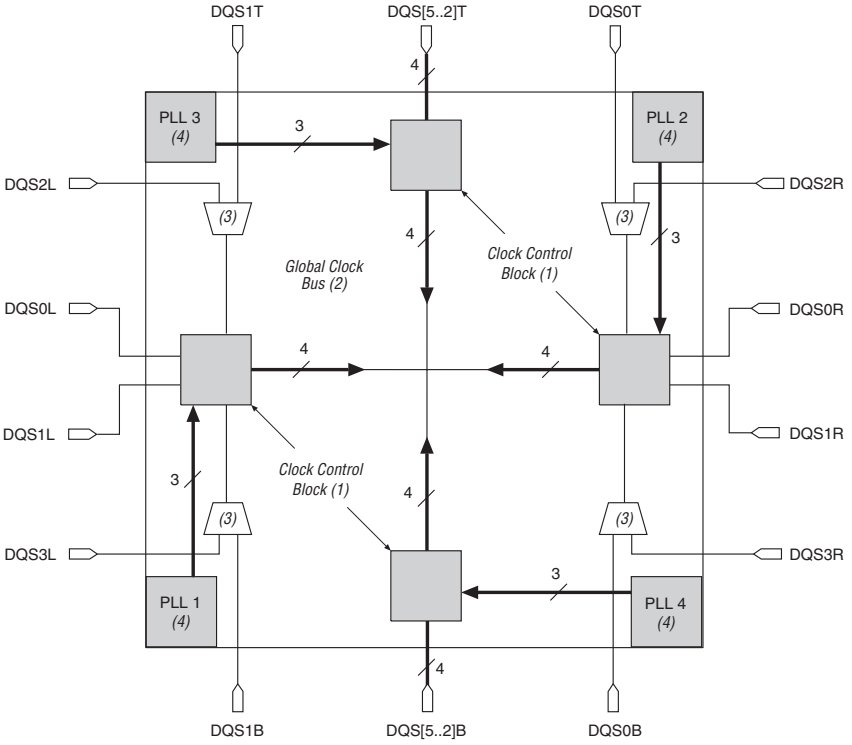
Notes to Figure 9–5:

(1) The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
(2) t_{CO} is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
(3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times, respectively.
(4) t_{CQD} is the skew between CQn and data edges.
(5) t_{CCQO} and t_{CQOH} are skew measurements between the C or C# clocks (or the K or K# clocks in single-clock mode) and the CQ or CQn clocks.

When writing to QDRII SRAM devices, the write clock generates the data while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

directly to the clock control block. For the larger Cyclone II devices, the corner DQS signals are multiplexed before they are routed to the clock control block. When you use the corner DQS pins for DDR implementation, there is a degradation in the performance of the memory interface. The clock control block is used to select from a number of input clock sources, in this case either PLL clock outputs or DQS pins, to drive onto the global clock bus. Figure 9–7 shows the corner DQS signal mappings for EP2C15 through EP2C70 devices.

Figure 9–7. Corner DQS Signal Mapping for EP2C15–EP2C70 Devices



Notes to Figure 9–7:

(1) There are four control blocks on each side.
(2) There are a total of 16 global clocks available.
(3) Only one of the corner DQS pins in each corner can feed the clock control block at a time. The other DQS pins can be used as general purpose I/O pins.
(4) PLL resource can be lost if all DQS pins from one side are used at the same time.
(5) Top/bottom and side IOE have different timing.

Figure 9–13 shows waveforms of the circuit shown in Figure 9–11. The first set of waveforms in Figure 9–13 shows the edge-aligned relationship between the DQ and DQS signals at the Cyclone II device pins. The second set of waveforms in Figure 9–13 shows what happens if the shifted DQS signal is not inverted. In this case, the last data, Q_n, does not get latched into the logic array as DQS goes to tri-state after the read postamble time. The third set of waveforms in Figure 9–13 shows a proper read operation with the DQS signal inverted after the 90° shift. The last data, Q_n, does get latched. In this case the outputs of register A_I and register C_I, which correspond to `dataout_h` and `dataout_l` ports, are now switched because of the DQS inversion. Register A_I, register B_I, and register C_I refer to the nomenclature in Figure 9–11.

Figure 9–13. DQ Captures With Noninverted & Inverted Shifted DQS

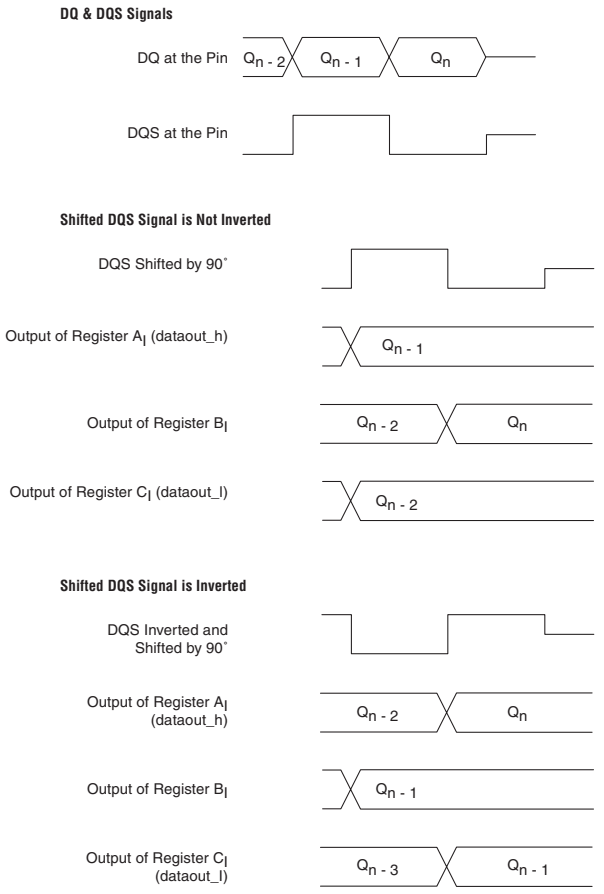
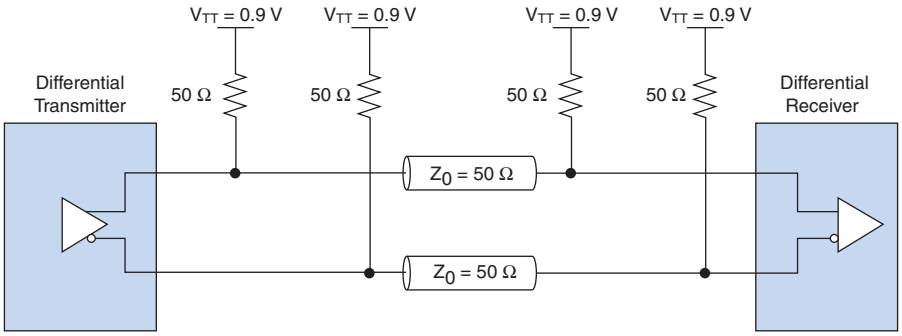


Figure 10–12. 1.8-V Differential HSTL Class II Termination



1.5-V LVCMOS (EIA/JEDEC Standard JESD8-11)

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices.

The 1.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.5-V LVCMOS.

1.5-V HSTL Class I and II

The 1.5-V HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic nominal switching range. This standard defines single-ended input and output specifications for all HSTL-compliant digital integrated circuits. The 1.5-V HSTL I/O standard in Cyclone II devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE, APEX 20KC, Stratix® II, Stratix GX, Stratix, and in Cyclone II devices themselves because the input and output voltage thresholds are compatible. Refer to Figures 10–13 and 10–14. Cyclone II devices support both input and output levels with V_{REF} and V_{TT}.

Table 10–5. Cyclone II Regular I/O Standards Support

I/O Standard	I/O Banks for EP2C15, EP2C20, EP2C35, EP2C50 and EP2C70 Devices								I/O Banks for EP2C5 and EP2C8 Devices			
	1	2	3	4	5	6	7	8	1	2	3	4
LVTTL	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
2.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5 V	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
3.3-V PCI	✓	✓	—	—	✓	✓	—	—	✓	—	✓	—
3.3-V PCI-X	✓	✓	—	—	✓	✓	—	—	✓	—	✓	—
SSTL-2 class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 class II	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
1.8-V HSTL class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.8-V HSTL class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
1.5-V HSTL class I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V HSTL class II	*(1)*	*(1)*	✓	✓	*(1)*	*(1)*	✓	✓	*(1)*	✓	*(1)*	✓
Pseudo-differential SSTL-2	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
Pseudo-differential SSTL-18	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
1.8-V pseudo-differential HSTL	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
1.5-V pseudo-differential HSTL	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*
LVDS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RSDS and mini-LVDS	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*
Differential LVPECL	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*

Notes to Table 10–5:

(1) These I/O banks support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.

(2) Pseudo-differential I/O standards are only supported for clock inputs and dedicated `PLL_OUT` outputs. Refer to Table 10–1 for more information.

(3) This I/O standard is only supported for outputs.

(4) This I/O standard is only supported for the clock inputs.

Table 10–12. Cyclone II I/O Standard DC Current Specification (Preliminary) (Part 2 of 2)

I/O Standard	I_{PIN} (mA)	
	Top and Bottom Banks	Side Banks
1.5-V differential HSTL class II *(3)*	16 *(4)*	
LVDS, RSDS and mini-LVDS	12	12

Notes to Table 10–12:

(1) The DC power specification of each I/O standard depends on the current sourcing and sinking capabilities of the I/O buffer programmed with that standard, as well as the load being driven. LVTTL and LVCMOS, and 2.5-, 1.8-, and 1.5-V outputs are not included in the static power calculations because they normally do not have resistor loads in real applications. The voltage swing is rail-to-rail with capacitive load only. There is no DC current in the system.

(2) This I_{PIN} value represents the DC current specification for the default current strength of the I/O standard. The I_{PIN} varies with programmable drive strength and is the same as the drive strength as set in Quartus II software. Refer to the *Cyclone II Architecture* chapter in volume 1 of the *Cyclone II Device Handbook* for more information on the programmable drive strength feature of voltage referenced I/O standards.

(3) The current value obtained for differential HSTL and differential SSTL standards is per pin and not per differential pair, as opposed to the per-pair current value of LVDS standard.

(4) This I/O standard is only supported for clock input pins and `PLL_OUT` pins.

Table 10–12 only shows the limit on the static power consumed by an I/O standard. The amount of total power used at any moment could be much higher, and is based on the switching activities.

5.0-V Device Compatibility

A Cyclone II device may not correctly interoperate with a 5.0-V device if the output of the Cyclone II device is connected directly to the input of the 5.0-V device. If V_{OUT} of the Cyclone II device is greater than V_{CCIO}, the PMOS pull-up transistor still conducts if the pin is driving high, preventing an external pull-up resistor from pulling the signal to 5.0-V.

A Cyclone II device can drive a 5.0-V LVTTL device by connecting the V_{CCIO} pins of the Cyclone II device to 3.3 V. This is because the output high voltage (V_{OH}) of a 3.3-V interface meets the minimum high-level voltage of 2.4-V of a 5.0-V LVTTL device. (A Cyclone II device cannot drive a 5.0-V LVCMOS device.)

Because the Cyclone II devices are 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI and 64-bit 133-MHz PCI-X compliant, the input circuitry accepts a maximum high-level input voltage (V_{IH}) of 4.1-V. To drive a Cyclone II device with a 5.0-V device, you must connect a resistor (R_2) between the Cyclone II device and the 5.0-V device. Refer to Figure 10–21.

If your design has multiple Cyclone II devices of the same density and package that contain the same configuration data, connect the nCE inputs to GND and leave the nCEO pins floating. You can also use the nCEO pin as a user I/O pin. Connect the configuration device nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE pins to each Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Make sure that the DCLK and DATA lines are buffered for every fourth device. All devices start and complete configuration at the same time. Figure 13–16 shows multiple device PS configuration when the Cyclone II devices are receiving the same configuration data.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the nCEO pin inputs to the next device's nCE pin, make sure that the nCEO pin is not used as a user I/O pin after configuration.

Other Altera devices that have JTAG support can be placed in the same JTAG chain for device programming and configuration.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP). Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information on JTAG and Jam STAPL in embedded environments, see *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*. To download the Jam player, go to the Altera web site (**www.altera.com**).

Configuring Cyclone II FPGAs with JRunner

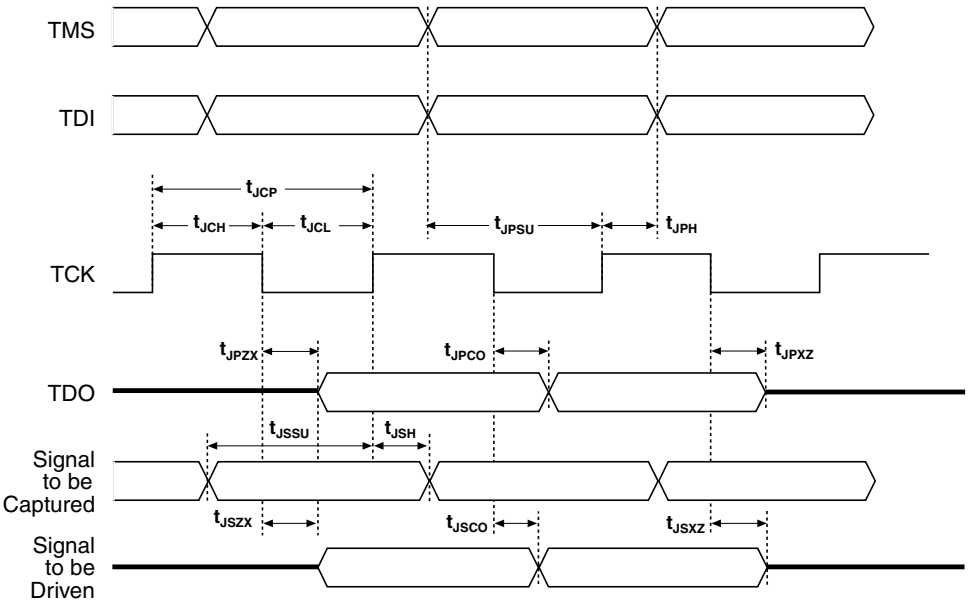
JRunner is a software driver that allows you to configure Cyclone II devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in **.rbf** format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

The RBF file used by the JRunner software driver can not be a compressed RBF file because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

For more information on the JRunner software driver, see *JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site.

When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with IDCODE as the initial instruction. At device power-up, the TAP controller starts in this TEST_LOGIC/RESET state. In addition, forcing the TAP controller to the TEST_LOGIC/RESET state is done by holding TMS high for five TCK clock cycles. Once in the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS is held high (while TCK is clocked). Figure 14–6 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 14–6. IEEE Std. 1149.1 Timing Waveforms



To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin. The waveform diagram in Figure 14–7 represents the entry of the instruction code into the instruction register. It shows the values of TCK, TMS, TDI, TDO, and the states of the TAP controller. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP controller to SHIFT_IR.