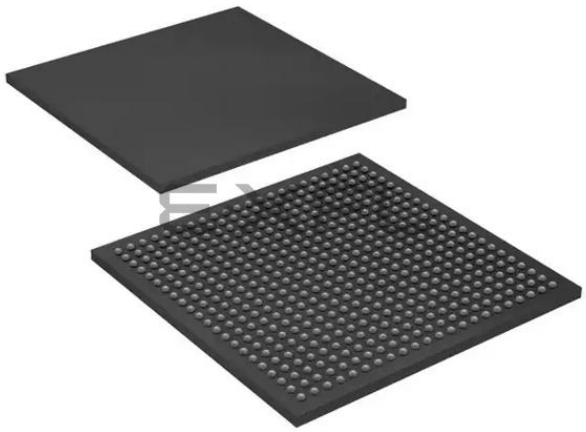

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	294
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f484c6

Cyclone II devices are available in up to three speed grades: –6, –7, and –8, with –6 being the fastest. Table 1–4 shows the Cyclone II device speed-grade offerings.

Table 1–4. Cyclone II Device Speed Grades

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA	896-Pin FineLine BGA
EP2C5 *(1)*	–6, –7, –8	–7, –8	—	–6, –7, –8	—	—	—	—
EP2C8	–6, –7, –8	–7, –8	—	–6, –7, –8	—	—	—	—
EP2C8A *(2)*	—	—	—	–8	—	—	—	—
EP2C15A	—	—	—	–6, –7, –8	–6, –7, –8	—	—	—
EP2C20	—	—	–8	–6, –7, –8	–6, –7, –8	—	—	—
EP2C20A *(2)*	—	—	—	–8	–8	—	—	—
EP2C35	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	—
EP2C50	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	—
EP2C70	—	—	—	—	—	—	–6, –7, –8	–6, –7, –8

Notes to Table 1–4:

(1) The EP2C5 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. Refer to the Cyclone II section in the *Automotive-Grade Device Handbook* for detailed information.

(2) EP2C8A and EP2C20A are only available in industrial grade.

5. DC Characteristics and Timing Specifications

CII51005-4.0

Operating Conditions

Cyclone® II devices are offered in commercial, industrial, automotive, and extended temperature grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the parameter values in this chapter apply to all Cyclone II devices. AC and DC characteristics are specified using the same numbers for commercial, industrial, and automotive grades. All parameters representing voltages are measured with respect to ground.

Tables 5–1 through 5–4 provide information on absolute maximum ratings.

Table 5–1. Cyclone II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Output supply voltage		–0.5	4.6	V
V_{CCA_PLL} [1..4]	PLL supply voltage		–0.5	1.8	V
V_{IN}	DC input voltage *(3)*	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	—	125	°C

Notes to Table 5–1:

(1) Conditions beyond those listed in this table cause permanent damage to a device. These are stress ratings only. Functional operation at these levels or any other conditions beyond those specified in this chapter is not implied. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effect on the device reliability.

(2) Refer to the *Operating Requirements for Altera Devices Data Sheet* for more information.

(3) During transitions, the inputs may overshoot to the voltage shown in Table 5–4 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transition, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5–41. Cyclone II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.5V_HSTL_CLASS_II	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
1.8V_HSTL_CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_HSTL_CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
DIFFERENTIAL_SSTL_2_ CLASS_I	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
DIFFERENTIAL_SSTL_2_ CLASS_II	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
DIFFERENTIAL_SSTL_18_ CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
DIFFERENTIAL_SSTL_18_ CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.8V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_I	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
1.5V_DIFFERENTIAL_HSTL_ CLASS_II	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps
LVDS	t_{PI}	651	682	1036	1075	1113	1113	ps
	t_{PCOUT}	434	455	669	699	728	728	ps
PCI	t_{PI}	595	623	1113	1156	1232	1232	ps
	t_{PCOUT}	378	396	746	780	847	847	ps
PCI-X	t_{PI}	595	623	1113	1156	1232	1232	ps
	t_{PCOUT}	378	396	746	780	847	847	ps

Notes to Table 5–41 :

(1) These numbers are for commercial devices.

(2) These numbers are for automotive devices.

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 2 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
2.5V	4 mA	t_{OP}	1208	1267	2478	2614	2743	2750	ps
		t_{DIP}	1340	1406	2648	2808	2969	2969	ps
	8 mA	t_{OP}	1190	1248	2307	2434	2554	2561	ps
		t_{DIP}	1322	1387	2477	2628	2780	2780	ps
	12 mA	t_{OP}	1154	1210	2192	2314	2430	2437	ps
		t_{DIP}	1286	1349	2362	2508	2656	2656	ps
	16 mA (1)	t_{OP}	1140	1195	2152	2263	2375	2382	ps
		t_{DIP}	1272	1334	2322	2457	2601	2601	ps
1.8V	2 mA	t_{OP}	1682	1765	3988	4279	4563	4570	ps
		t_{DIP}	1814	1904	4158	4473	4789	4789	ps
	4 mA	t_{OP}	1567	1644	3301	3538	3768	3775	ps
		t_{DIP}	1699	1783	3471	3732	3994	3994	ps
	6 mA	t_{OP}	1475	1547	2993	3195	3391	3398	ps
		t_{DIP}	1607	1686	3163	3389	3617	3617	ps
	8 mA	t_{OP}	1451	1522	2882	3074	3259	3266	ps
		t_{DIP}	1583	1661	3052	3268	3485	3485	ps
	10 mA	t_{OP}	1438	1508	2853	3041	3223	3230	ps
		t_{DIP}	1570	1647	3023	3235	3449	3449	ps
	12 mA (1)	t_{OP}	1438	1508	2853	3041	3223	3230	ps
		t_{DIP}	1570	1647	3023	3235	3449	3449	ps
1.5V	2 mA	t_{OP}	2083	2186	4477	4870	5256	5263	ps
		t_{DIP}	2215	2325	4647	5064	5482	5482	ps
	4 mA	t_{OP}	1793	1881	3649	3965	4274	4281	ps
		t_{DIP}	1925	2020	3819	4159	4500	4500	ps
	6 mA	t_{OP}	1770	1857	3527	3823	4112	4119	ps
		t_{DIP}	1902	1996	3697	4017	4338	4338	ps
	8 mA (1)	t_{OP}	1703	1787	3537	3827	4111	4118	ps
		t_{DIP}	1835	1926	3707	4021	4337	4337	ps

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 3 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_18_ CLASS_II	16 mA	260	220	180	—	—	—	—	—	—
	18 mA	270	220	180	—	—	—	—	—	—
1.8V_HSTL_ CLASS_I	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	320	270	220	320	270	220	320	270	220
1.8V_HSTL_ CLASS_II	16 mA	230	190	160	—	—	—	—	—	—
	18 mA	240	200	160	—	—	—	—	—	—
	20 mA	250	210	170	—	—	—	—	—	—
1.5V_HSTL_ CLASS_I	8 mA	210	170	140	210	170	140	210	170	140
	10 mA	220	180	150	—	—	—	—	—	—
	12 mA	230	190	160	—	—	—	—	—	—
1.5V_HSTL_ CLASS_II	16 mA	210	170	140	—	—	—	—	—	—
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
DIFFERENTIAL_ SSTL_18_CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—
DIFFERENTIAL_SSTL _18_CLASS_II	16 mA	260	220	180	—	—	—	—	—	—
	18 mA	270	220	180	—	—	—	—	—	—
1.8V_ DIFFERENTIAL_HSTL _CLASS_I	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	320	270	220	320	270	220	320	270	220
1.8V_ DIFFERENTIAL_HSTL _CLASS_II	16 mA	230	190	160	—	—	—	—	—	—
	18 mA	240	200	160	—	—	—	—	—	—
	20 mA	250	210	170	—	—	—	—	—	—

Table 5–47. High-Speed I/O Timing Definitions (Part 2 of 2)

Parameter	Symbol	Description
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. Sampling window is the sum of the setup time, hold time, and jitter. The window of t_{SU} + t_H is expected to be centered in the sampling window. SW = TUI – TCCS – (2 × RSKM)
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2
Input jitter (peak to peak)	—	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak to peak)	—	Peak-to-peak output jitter on high-speed PLLs.
Signal rise time	t_{RISE}	Low-to-high transmission time.
Signal fall time	t_{FALL}	High-to-low transmission time.
Lock time	t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Figure 5–3. High-Speed I/O Timing Diagram

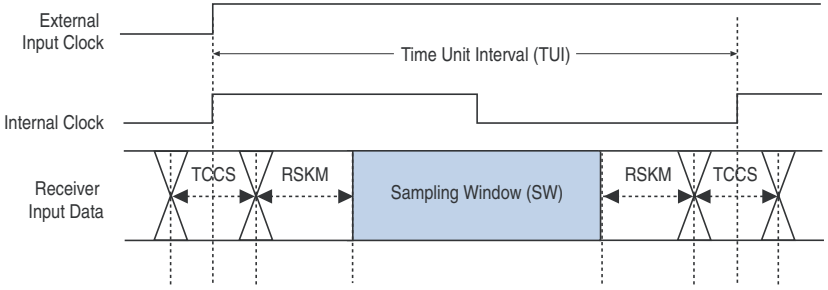


Figure 5–4 shows the high-speed I/O timing budget.

Table 7–8. Global Clock Network Connections (Part 2 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PLL4_c0													✓	✓		✓
PLL4_c1													✓		✓	✓
PLL4_c2														✓	✓	
DPCLK0 *(1)*	✓															
DPCLK1 *(1)*		✓														
DPCLK10 *(1)*, *(2)* CDPCLK0 or CDPCLK7 *(3)*			✓													
DPCLK2 *(1)*, *(2)* CDPCLK1 or CDPCLK2 *(3)*				✓												
DPCLK7 *(1)*					✓											
DPCLK6 *(1)*						✓										
DPCLK8 *(1)*, *(2)* CDPCLK5 or CDPCLK6 *(3)*							✓									
DPCLK4 *(1)*, *(2)* CDPCLK4 or CDPCLK3 *(3)*								✓								
DPCLK8 *(1)*									✓							
DPCLK11 *(1)*										✓						
DPCLK9 *(1)*											✓					
DPCLK10 *(1)*												✓				
DPCLK5 *(1)*													✓			
DPCLK2 *(1)*														✓		
DPCLK4 *(1)*															✓	

Table 7–8. Global Clock Network Connections (Part 3 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DPCLK3 *(1)*																✓

Notes to Table 7–8:
(1) See the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook* for more information on DPCLK pins.
(2) This pin only applies to EP2C5 and EP2C8 devices.
(3) These pins only apply to EP2C15 devices and larger. Only one of the two CDPCLK pins can feed the clock control block. The other pin can be used as a regular I/O pin.

If the dedicated clock pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the logic array using the MultiTrack interconnect. However, if they are used as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Clock Control Block

Every global clock network is driven by a clock control block residing either on the top, bottom, left, or right side of the Cyclone II device. The global clock network has been optimized for minimum clock skew and delay.

Table 7–9 lists the sources that can feed the clock control block, which in turn feeds the global clock networks.

Table 7–9. Clock Control Block Inputs (Part 1 of 2)

Input	Description
Dedicated clock inputs	Dedicated clock input pins can drive clocks or global signals, such as asynchronous clears, presets, or clock enables onto a given global clock network.
Dual-purpose clock (DPCLK and CDPCLK) I/O inputs	DPCLK and CDPCLK I/O pins are bidirectional dual function pins that can be used for high fan-out control signals, such as protocol signals, TRDY and IRDY signals for PCI, or DQS for DDR, via the global clock network.

Table 7–9. Clock Control Block Inputs (Part 2 of 2)

Input	Description
PLL outputs	The PLL counter outputs can drive the global clock network.
Internal logic	The global clock network can also be driven through the logic array routing to enable internal logic (LEs) to drive a high fan-out, low skew signal path.

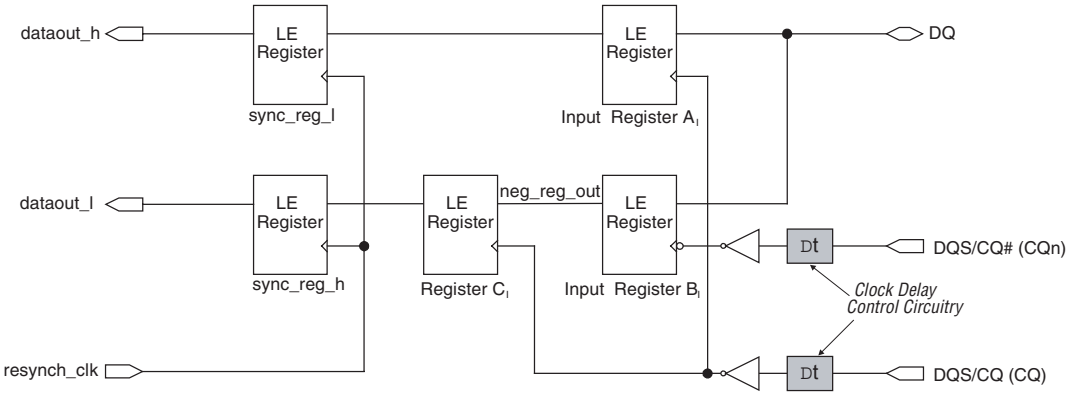
In Cyclone II devices, the dedicated clock input pins, PLL counter outputs, dual-purpose clock I/O inputs, and internal logic can all feed the clock control block for each global clock network. The output from the clock control block in turn feeds the corresponding global clock network. The clock control blocks are arranged on the device periphery and there are a maximum of 16 clock control blocks available per Cyclone II device.

The control block has two functions:

- Dynamic global clock network clock source selection
- Global clock network power-down (dynamic enable and disable)

Figure 7–11 shows the clock control block.

Figure 9–4. CQ & CQn Connection for QDRII SRAM Read



Read & Write Operation

Figure 9–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDRII SRAM devices send data within t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQn clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Cyclone II devices.

Figure 10–1. SSTL-2 Class I Termination

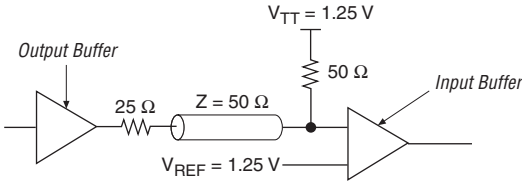
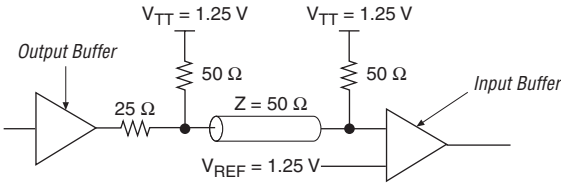


Figure 10–2. SSTL-2 Class II Termination



Cyclone II devices support both input and output SSTL-2 class I and II levels.

Pseudo-Differential SSTL-2

The differential SSTL-2 I/O standard (EIA/JEDEC standard JESD8-9A) is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard specifies an input voltage range of – 0.3 V ≤V_I ≤V_{CCIO} + 0.3 V. The differential SSTL-2 standard does not require an input reference voltage. Refer to Figures 10–3 and 10–4 for details on differential SSTL-2 terminations.

Cyclone II devices do not support true differential SSTL-2 standards. Cyclone II devices support pseudo-differential SSTL-2 outputs for `PLL_OUT` pins and pseudo-differential SSTL-2 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

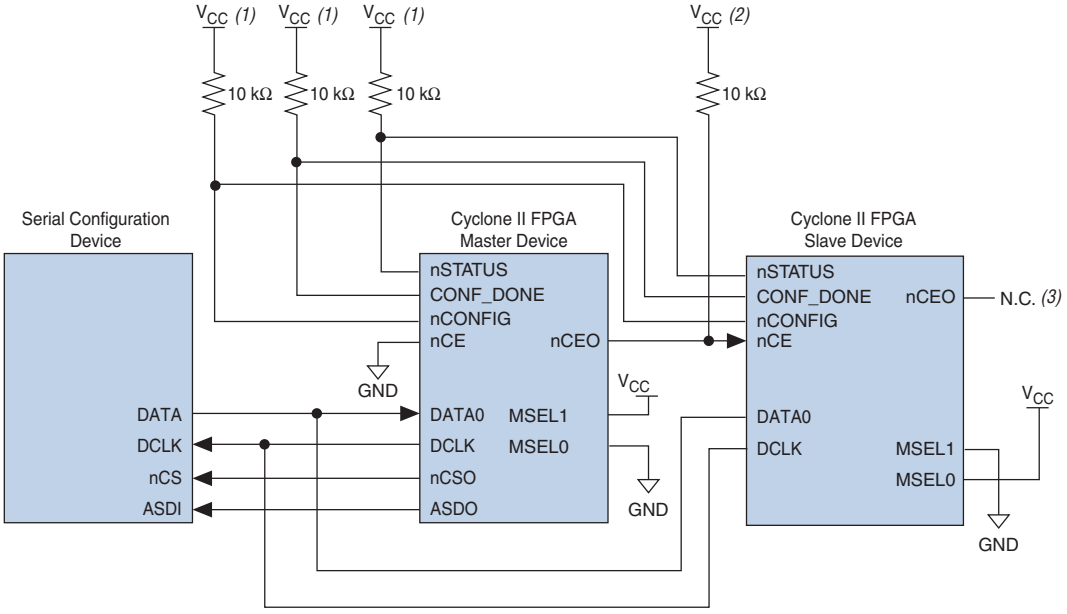
Document Revision History

Table 12–4 shows the revision history for this document.

Table 12–4. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v1.2	• Added document revision history. • Updated "Software Support" section.	• Removed reference to third-party synthesis tool: LeonardoSpectrum and Synplify.
November 2005 v2.1	Updated Introduction.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Figure 13–4. Multiple Device AS Configuration



Notes to Figure 13–4:

(1) Connect the pull-up resistors to a 3.3-V supply.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

As shown in Figure 13–4, the nSTATUS and CONF_DONE pins on all target FPGAs are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the FPGAs. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep the CONF_DONE signal low until they receive their configuration data. When all the target FPGAs in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor pulls this signal high, and all devices simultaneously enter initialization mode.

Configuration Stage

When the nSTATUS pin transitions high, the configuration device's OE pin also transitions high and the configuration device clocks data out serially to the FPGA using its internal oscillator. The Cyclone II device receives configuration data on its DATA0 pin and the clock is received on the DCLK pin. Data is latched into the FPGA on the rising edge of DCLK.

After the FPGA has received all configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by a pull-up resistor. Since the Cyclone II device's CONF_DONE pin is tied to the configuration device's nCS pin, the configuration device is disabled when CONF_DONE goes high. Enhanced configuration and EPC2 devices have an optional internal pull-up resistor on the nCS pin. You can turn this option on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you do not use this internal pull-up resistor, you need to connect an external 10-kΩ pull-up resistor to the nCS and CONF_DONE line. A low-to-high transition on CONF_DONE indicates configuration is complete, and the device can begin initialization.

Initialization Stage

In Cyclone II devices, the default initialization clock source is the Cyclone II internal oscillator (typically 10 MHz). Cyclone II devices can also use the optional CLKUSR pin. If your design uses the internal oscillator, the Cyclone II device supplies itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to use another device or source to send additional clock cycles to the CLKUSR pin during the initialization stage. Additionally, you can use of the CLKUSR pin as a user I/O pin, which means you have an additional user I/O pin.

If you want to delay the initialization of the device, you can use the CLKUSR pin. Using the CLKUSR pin allows you to control when the Cyclone II device enters user mode. You can delay the Cyclone II devices from entering user mode for an indefinite amount of time. You can turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data is accepted and CONF_DONE goes high, Cyclone II devices require 299 clock cycles to properly initialize and support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you use the INIT_DONE pin, an external 10-kΩ pull-up resistor pulls it high when

Table 13–12 describes the optional configuration pins. If these optional configuration pins are not enabled in the Quartus II software, they are available as general-purpose user I/O pins. Therefore during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 13–12. Optional Configuration Pins

Pin Name	User Mode	Pin Type	Description
CLKUSR	N/A if option is on. I/O if option is off.	Input	This is an optional user-supplied clock input that synchronizes the initialization of one or more devices. This pin is enabled by turning on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	This is a status pin that can be used to indicate when the device has initialized and is in user mode. When nCONFIG is low and during the beginning of configuration, the INIT_DONE pin is tri-stated and pulled high due to an external 10-kΩ pull-up resistor. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high and the FPGA enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the **Enable INIT_DONE output** option in the Quartus II software.
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows the user to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated. When this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the **Enable device-wide output enable (DEV_OE)** option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared. When this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the **Enable device-wide reset (DEV_CLRn)** option in the Quartus II software.

When designing a board for JTAG configuration of Cyclone II devices, the connections for the dedicated configuration pins need to be considered.

For more information on using the IEEE Std.1149.1 circuitry for device configuration, see the *Configuring Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

BST for Configured Devices

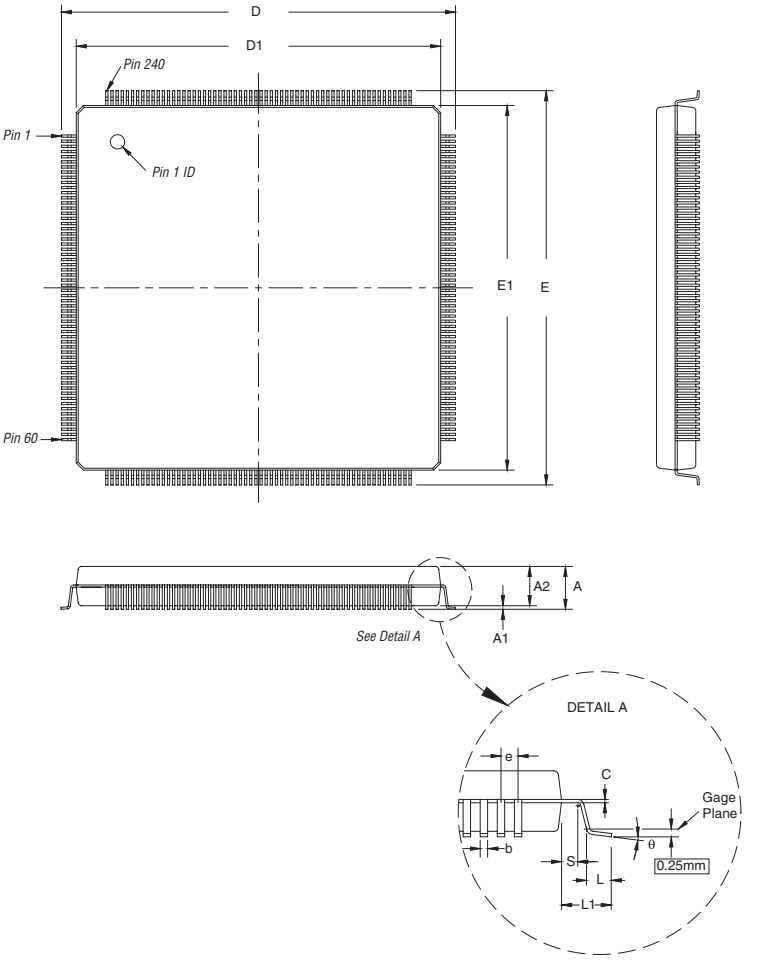
For a configured device, the input buffers are turned off by default for I/O pins that are set as output only in the design file. Nevertheless, executing the SAMPLE instruction will turn on the input buffers for the output pins. You can set the Quartus II software to always enable the input buffers on a configured device so it behaves the same as an unconfigured device for boundary-scan testing, allowing sample function on output pins in the design. This aspect can cause slight increase in standby current because the unused input buffer is always on. In the Quartus II software, do the following:

1. Choose **Settings** (Assignment menu).
2. Click **Assembler**.
3. Turn on **Always Enable Input Buffers**.
4. If you use the default setting with input disabled, you need to convert the default BSDL file to the design-specific BSDL file using the BSDLCustomizer script. For more information regarding BSDL file, refer to "Boundary-Scan Description Language (BSDL) Support".

Table 15–10. 240-Pin PQFP Package Outline Dimensions (Part 2 of 2)			
Symbol	Millimeter		
	Min.	Nom.	Max.
e	0.50 BSC		
θ	0°	3.5°	8°

Figure 15–3 shows a 240-pin PQFP package outline.

Figure 15–3. 240-pin PQFP Package Outline



484-Pin FineLine BGA, Option 3 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 15–13 and 15–14 show the package information and package outline figure references, respectively, for the 484-pin FineLine BGA package.

Table 15–13. 484-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAJ-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	5.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–14. 484-Pin FineLine BGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	23.00 BSC		
E	23.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		