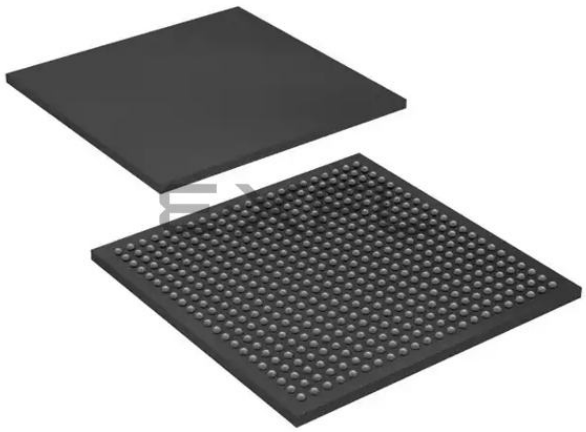

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

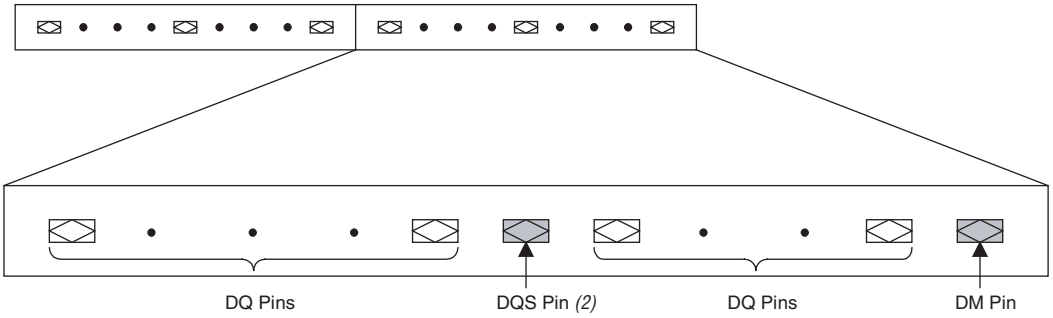
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	294
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f484c7

Figure 2–26. Cyclone II Device DQ & DQS Groups in ×8/×9 Mode *Notes (1), (2)*



Notes to Figure 2–26:
(1) Each DQ group consists of a DQS pin, DM pin, and up to nine DQ pins.
(2) This is an idealized pin layout. For actual pin layout, refer to the pin table.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR and DDR2 SDRAM. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. The dedicated external memory interface in Cyclone II devices also includes programmable delay circuitry that can shift the incoming DQS signals to center align the DQS signals within the data window.

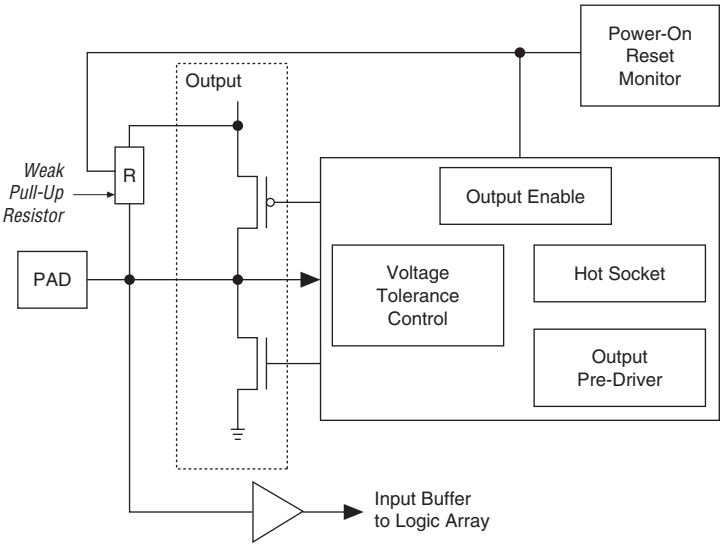
The DQS signal is usually associated with a group of data (DQ) pins. The phase-shifted DQS signals drive the global clock network, which is used to clock the DQ signals on internal LE registers.

Table 2–15 shows the number of DQ pin groups per device.

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups (5), (6)	Number of ×16 Groups	Number of ×18 Groups (5), (6)
EP2C5	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
EP2C8	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
	256-pin FineLine BGA®	8 (3)	4	4	4
EP2C15	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8
EP2C20	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8

Figure 4–1. Hot-Socketing Circuit Block Diagram for Cyclone II Devices



The POR circuit monitors V_{CCINT} voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} keeps the I/O pins from floating. The voltage tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

For more information, see the *DC Characteristics & Timing Specifications* chapter in Volume 1 of the *Cyclone II Device Handbook* for the value of the internal weak pull-up resistors.

Figure 4–2 shows a transistor level cross section of the Cyclone II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot socketing. The V_{PAD} leakage current charges the voltage tolerance control circuit capacitance.

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.337	–0.357	0.079	0.04	0.075	0.045	ns

Notes to Table 5–25:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–26. EP2C15A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.542	1.615	2.490	2.651	2.886	2.866	ns
t_{COUT}	1.544	1.617	2.506	2.664	2.894	2.874	ns
t_{PLLCIN}	–0.424	–0.448	–0.057	–0.107	–0.077	–0.107	ns
$t_{PLLCOUT}$	–0.422	–0.446	–0.041	–0.094	–0.069	–0.099	ns

Notes to Table 5–26:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C20/A Clock Timing Parameters

Tables 5–27 and 5–28 show the clock timing parameters for EP2C20/A devices.

Table 5–27. EP2C20/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

JTAG Timing Specifications

Figure 5–7 shows the timing requirements for the JTAG signals.

Figure 5–7. Cyclone II JTAG Waveform

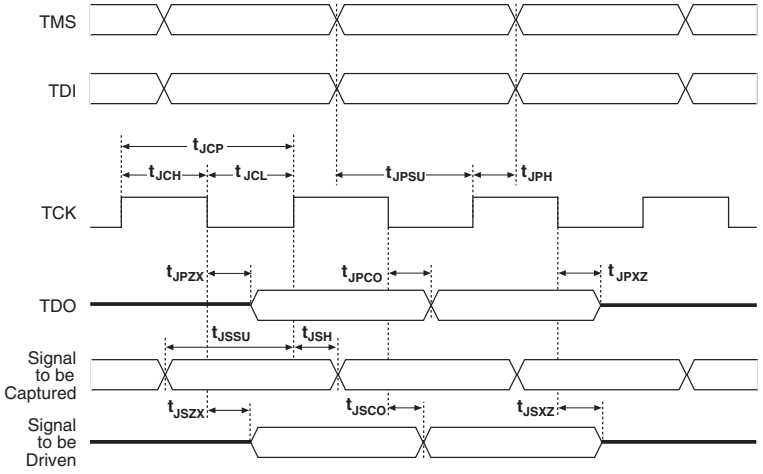


Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins *Notes (1), (2)* *(Part 2 of 2)*

Row I/O Output Standard	C6	C7	C8	Unit
Differential SSTL-2 Class I	60	90	90	ps
Differential SSTL-2 Class II	65	75	75	ps
Differential SSTL-18 Class I	90	165	165	ps
Differential HSTL-18 Class I	85	155	155	ps
Differential HSTL-15 Class I	145	145	205	ps
LVDS	60	60	60	ps
Simple RSDS	60	60	60	ps
Mini LVDS	60	60	60	ps
PCI	195	255	255	ps
PCI-X	195	255	255	ps

Notes to Table 5–55:
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Here is an example for calculating the DCD as a percentage for an SDR output on a row I/O on a –6 device:

If the SDR output I/O standard is SSTL-2 Class II, the maximum DCD is 65 ps (refer to Table 5–55). If the clock frequency is 167 MHz, the clock period T is:

$$T = 1/f = 1 / 167\ \text{MHz} = 6\ \text{ns} = 6000\ \text{ps}$$

To calculate the DCD as a percentage:

$(T/2 - DCD) / T = (6000\ \text{ps}/2 - 65\ \text{ps}) / 6000\ \text{ps} = 48.91\%$ (for low boundary)

$(T/2 + DCD) / T = (6000\ \text{ps}/2 + 65\ \text{ps}) / 6000\text{ps} = 51.08\%$ (for high boundary

Table 5–56. Maximum DCD for SDR Output on Column I/O *Notes (1), (2)* *(Part 1 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
LVCMOS	195	285	285	ps
LVTTL	210	305	305	ps

The actual half period is then = 3000 ps – 155 ps = 2845 ps

Table 5–58. Maximum DCD for DDIO Output on Column I/O Pins with PLL in the Clock Path *Notes (1), (2)*

Column I/O Pins in the Clock Path	C6	C7	C8	Unit
LVCMOS	285	400	445	ps
LVTTL	305	405	460	ps
2.5-V	175	195	285	ps
1.8-V	190	205	260	ps
1.5-V	605	645	645	ps
SSTL-2 Class I	125	210	245	ps
SSTL-2 Class II	195	195	195	ps
SSTL-18 Class I	130	240	245	ps
SSTL-18 Class II	135	270	330	ps
HSTL-18 Class I	135	240	240	ps
HSTL-18 Class II	165	240	285	ps
HSTL-15 Class I	220	335	335	ps
HSTL-15 Class II	190	210	375	ps
Differential SSTL-2 Class I	125	210	245	ps
Differential SSTL-2 Class II	195	195	195	ps
Differential SSTL-18 Class I	130	240	245	ps
Differential SSTL-18 Class II	132	270	330	ps
Differential HSTL-18 Class I	135	240	240	ps
Differential HSTL-18 Class II	165	240	285	ps
Differential HSTL-15 Class I	220	335	335	ps
Differential HSTL-15 Class II	190	210	375	ps
LVDS	110	120	125	ps
Simple RSDS	125	125	275	ps
Mini-LVDS	110	120	125	ps

Notes to Table 5–58:

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

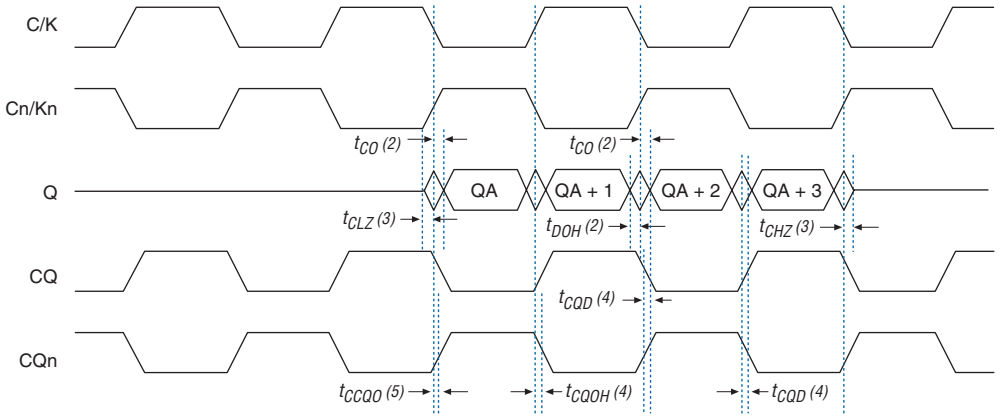
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Independent Clock Mode

Cyclone II memory blocks can implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables for port A and B registers. However, ports do not support asynchronous clear signals for the registers.

Figure 8–13 shows a memory block in independent clock mode.

Figure 9–5. Data & Clock Relationship During a QDRII SRAM Report



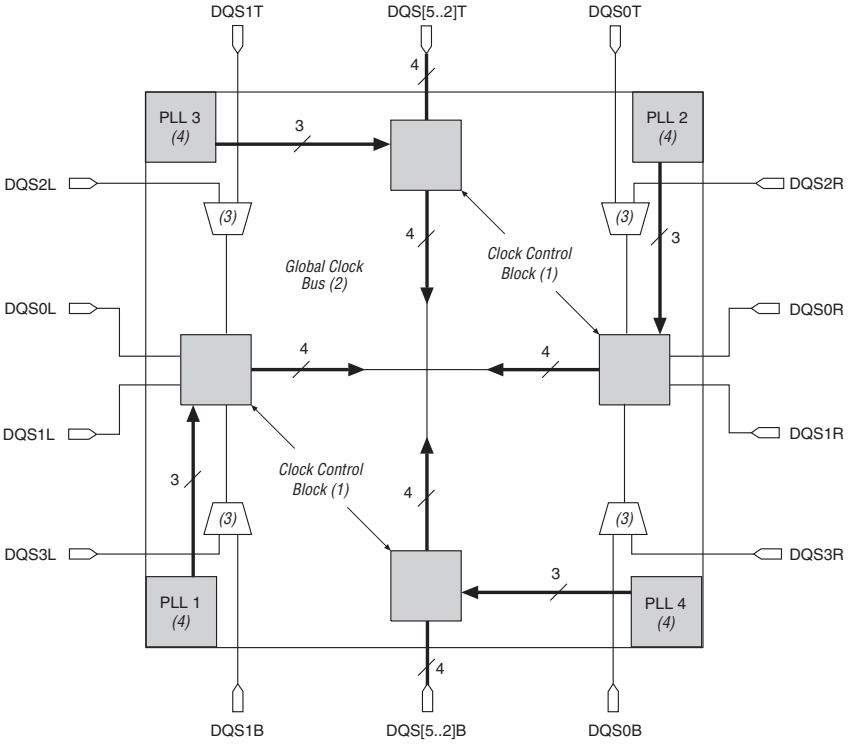
Notes to Figure 9–5:

(1) The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
(2) t_{CO} is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
(3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times, respectively.
(4) t_{CQD} is the skew between CQn and data edges.
(5) t_{CCQO} and t_{CQOH} are skew measurements between the C or C# clocks (or the K or K# clocks in single-clock mode) and the CQ or CQn clocks.

When writing to QDRII SRAM devices, the write clock generates the data while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

directly to the clock control block. For the larger Cyclone II devices, the corner DQS signals are multiplexed before they are routed to the clock control block. When you use the corner DQS pins for DDR implementation, there is a degradation in the performance of the memory interface. The clock control block is used to select from a number of input clock sources, in this case either PLL clock outputs or DQS pins, to drive onto the global clock bus. Figure 9–7 shows the corner DQS signal mappings for EP2C15 through EP2C70 devices.

Figure 9–7. Corner DQS Signal Mapping for EP2C15–EP2C70 Devices



Notes to Figure 9–7:

(1) There are four control blocks on each side.
(2) There are a total of 16 global clocks available.
(3) Only one of the corner DQS pins in each corner can feed the clock control block at a time. The other DQS pins can be used as general purpose I/O pins.
(4) PLL resource can be lost if all DQS pins from one side are used at the same time.
(5) Top/bottom and side IOE have different timing.

For example, to implement a 72-bit wide SDRAM memory interface in Cyclone II devices, use 5 DQS/DQ groups in the top I/O bank and 4 DQS/DQ groups in the bottom I/O bank, or vice-versa. In this case, if DQS0T or DQS1T is used for the fifth DQS signal, the DQS2R or DQS2L pins become regular I/O pins and are unavailable for DQS signals in memory interface. For detailed information about the global clock network, refer to the *Global Clock Network & Phase Locked Loops* section in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

You must configure the DQ and DQS pins as bidirectional DDR pins on all the I/O banks of the device. Use the `altdq` and `altdqs` megafunctions to configure the DQ and DQS paths, respectively. If you only want to use the DQ or DQS pins as inputs, for instance in the QDRII memory interface where DQ and DQS are unidirectional read data and read clock, set the output enable of the DQ or DQS pins to ground. For further information, please refer to the section "QDRII SRAM" on page 9–5 of this handbook.

Clock, Command & Address Pins

You can use any of the user I/O pins on all the I/O banks (that support the external memory's I/O standard) of the device to generate clocks and command and address signals to the memory device.

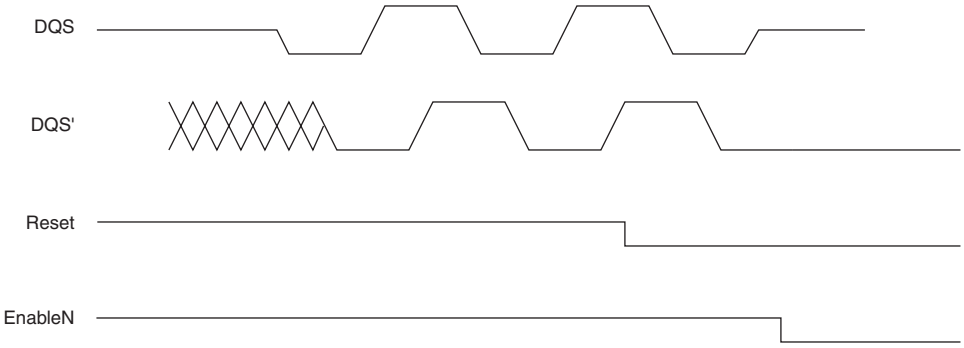
Parity, DM & ECC Pins

You can use any of the DQ pins for the parity pins in Cyclone II devices. Cyclone II devices support parity in the ×8/×9 and ×16/×18 modes. There is one parity bit available per 8 bits of data pins.

The data mask (DM) pins are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pin indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. In Cyclone II devices, the DM pins are pre-assigned in the device pin outs, and these are the preferred pins. Each group of DQS and DQ signals requires a DM pin. Similar to the DQ output signals, the DM signals are clocked by the –90° shifted clock.

Some DDR SDRAM and DDR2 SDRAM devices support error correction coding (ECC) or parity. Parity bit checking is a way to detect errors, but it has no correction capabilities. ECC can detect and automatically correct errors in data transmission. In 72-bit DDR SDRAM, there are 8 ECC pins on top of the 64 data pins. Connect the DDR and DDR2 SDRAM ECC pins to a Cyclone II device's DQS/DQ group. The memory controller needs extra logic to encode and decode the ECC data.

Figure 9–10. Cyclone II DQS Postamble Circuitry Control Timing Waveform



DDR Input Registers

In Cyclone II devices, the DDR input registers are implemented with five internal LE registers located in the logic array block (LAB) adjacent to the DDR input pin (see Figure 9–11). The DDR data is fed to the first two registers, input register A_I and input register B_I. Input register B_I captures the DDR data present during the rising edge of the clock. Input register A_I captures the DDR data present during the falling edge of the clock. Register C_I aligns the data before it is transferred to the resynchronization registers.

Figure 9–11. DDR Input Implementation

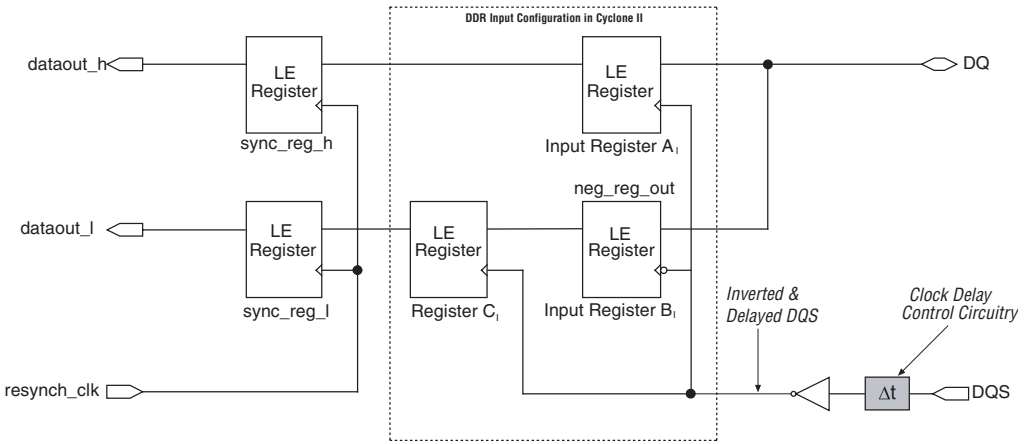
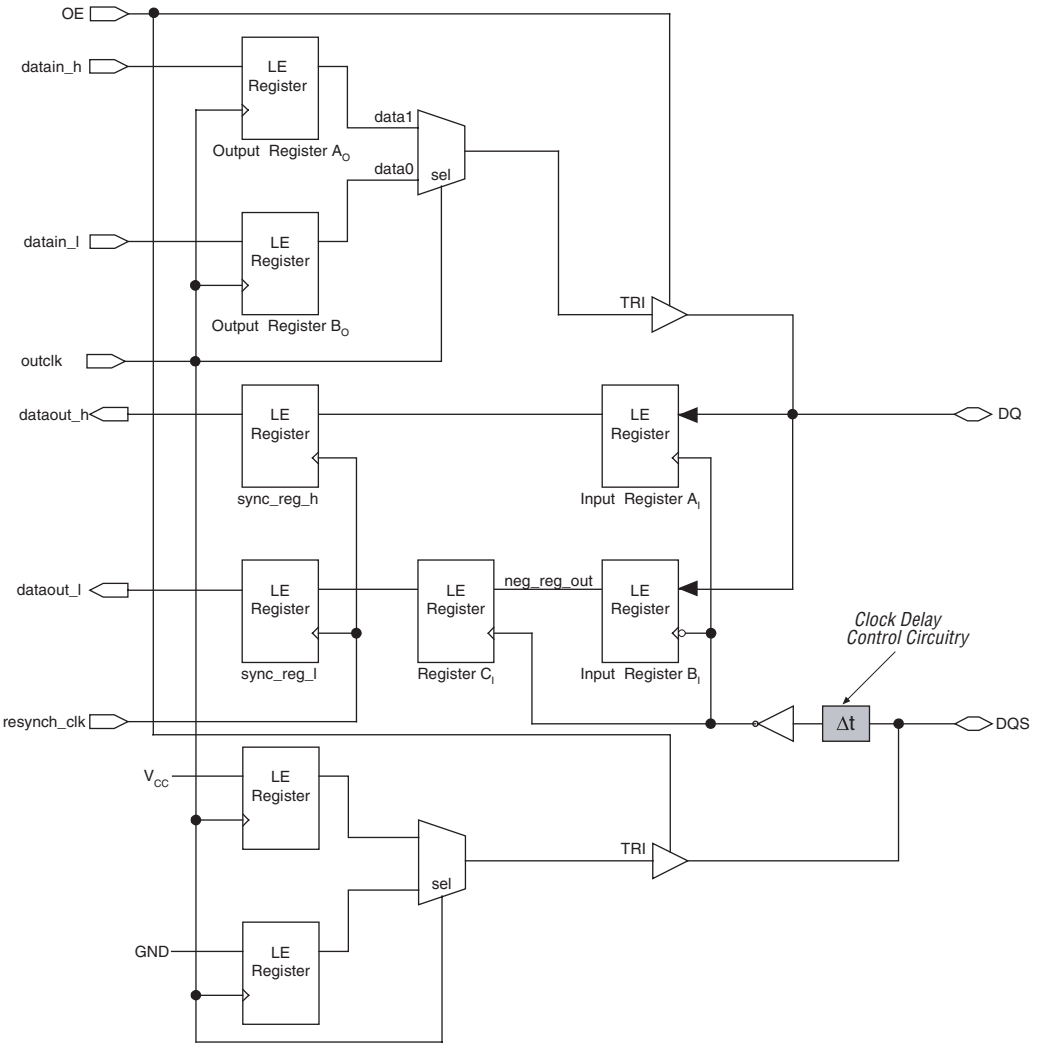


Figure 9–16. Bidirectional DDR Implementation for DDR Memory Interfaces *Note (1)*



Note to Figure 9–16:

(1) You can use the `altdq` and `altdqs` megafunctions to generate the DQ and DQS signals.

Figure 9–17 shows example waveforms from a bidirectional DDR implementation.

Figure 10–13. 1.5-V HSTL Class I Termination

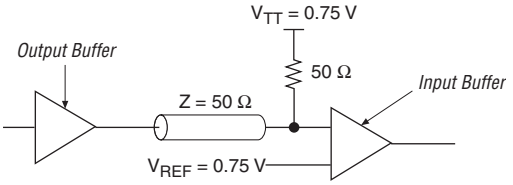
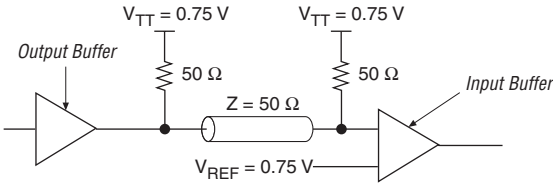


Figure 10–14. 1.5-V HSTL Class II Termination



1.5-V Pseudo-Differential HSTL Class I and II

The 1.5-V differential HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

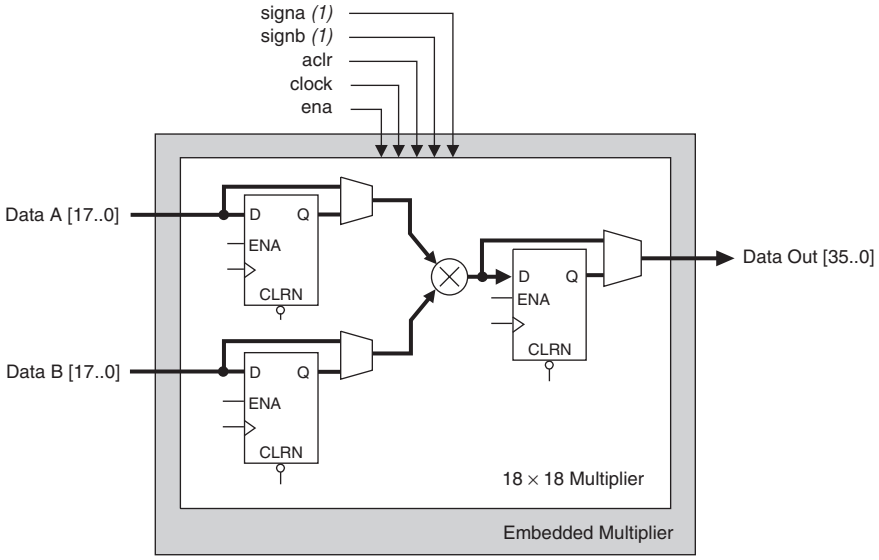
The 1.5-V differential HSTL specification is the same as the 1.5-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic switching range, such as QDR memory clock interfaces. Cyclone II devices support both input and output levels. Refer to Figures 10–15 and 10–16 for details on the 1.5-V differential HSTL termination.

Cyclone II devices do not support true 1.5-V differential HSTL standards. Cyclone II devices support pseudo-differential HSTL outputs for `PLL_OUT` pins and pseudo-differential HSTL inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential HSTL.

18-Bit Multipliers

Each embedded multiplier can be configured to support a single 18 × 18 multiplier for input widths from 10- to 18-bits. Figure 12–3 shows the embedded multiplier configured to support an 18-bit multiplier.

Figure 12–3. 18-Bit Multiplier Mode



Note to Figure 12–3:
(1) If necessary, you can send these signals through one register to match the data signal path.

All 18-bit multiplier inputs and results can be independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers or a combination of both. Additionally, you can change the `signa` and `signb` signals dynamically and can send these signals through dedicated input registers.

9-Bit Multipliers

Each embedded multiplier can also be configured to support two 9 × 9 independent multipliers for input widths up to 9-bits. Figure 12–4 shows the embedded multiplier configured to support two 9-bit multipliers.

nCONFIG low for at least 2 µs to restart configuration. The microprocessor or controller can only transition the nCONFIG pin low if the pin is under system control and not tied to V_{CC}.

The enhanced configuration devices support parallel configuration of up to eight devices. The *n*-bit (*n* = 1, 2, 4, or 8) PS configuration mode allows enhanced configuration devices to concurrently configure a chain of FPGAs. These devices do not have to be the same device family or density; they can be any combination of Altera FPGAs with different designs. An individual enhanced configuration device DATA pin is available for each targeted FPGA. Each DATA line can also feed a chain of FPGAs. Figure 13–15 shows how to concurrently configure multiple devices using an enhanced configuration device.

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 5 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
DCLK	N/A	PS, AS	Input (PS) Output (AS)	In PS configuration, DCLK is the clock input used to clock data from an external source into the target device. Data is latched into the Cyclone II device on the rising edge of DCLK. In AS mode, DCLK is an output from the Cyclone II device that provides timing for the configuration interface. In AS mode, DCLK has an internal pull-up that is always active. After configuration, this pin is tri-stated. If you are using a configuration device, it drives DCLK low after configuration is complete. If your design uses a control host, drive DCLK either high or low. Toggling this pin after configuration does not affect the configured device. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.
DATA0	N/A	All	Input	This is the data input pin. In serial configuration modes, bit-wide configuration data is presented to the target device on the DATA0 pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After configuration, EPC1 and EPC1441 devices tri-state this pin, while enhanced configuration and EPC2 devices drive this pin high. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.

- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when the EXTEST mode is entered. If the OEJ update register contains a 0, the data in the OUTJ update register is driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST testing during ICR. This instruction is supported before or after ICR, but not during ICR. Use the CONFIG_IO instruction to interrupt configuration, then perform testing, or wait for configuration to complete.
- If performing testing before configuration, hold the nCONFIG pin low.
- After configuration, any pins in a differential pin pair cannot be tested. Therefore, performing BST after configuration requires editing BSC group definitions that correspond to these differential pin pairs. The BSC group should be redefined as an internal cell. See the BSDL file for more information on editing.

For more information on boundary scan testing, contact Altera Applications.

Boundary-Scan Description Language (BSDL) Support

The Boundary-Scan Description Language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the BSDL files for test generation, analysis, and failure diagnostics. For more information, or to receive BSDL files for IEEE Std. 1149.1-compliant Cyclone II devices, visit the Altera web site at **www.altera.com**.

Conclusion

The IEEE Std. 1149.1 BST circuitry available in Cyclone II devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use the EXTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, CLAMP, and HIGHZ modes to create serial patterns that internally test the pin connections between devices and check device operation.

References

Bleeker, H., P. van den Eijnden, and F. de Jong. *Boundary-Scan Test: A Practical Approach*. Eindhoven, The Netherlands: Kluwer Academic Publishers, 1993.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard Test Access Port and Boundary-Scan Architecture* (IEEE Std 1149.1-2001). New York: Institute of Electrical and Electronics Engineers, Inc., 2001.

Section VII. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. The chapters in this section contain the required PCB layout guidelines and package specifications.

This section includes the following chapters:

- Chapter 15, Package Information for Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Tables 15–5 and 15–6 show the package information and package outline figure references, respectively, for the 144-pin TQFP package.

Table 15–5. 144-Pin TQFP Package Information

Description	Specification
Ordering code reference	T
Package acronym	TQFP
Lead frame material	Copper
Lead finish (plating)	Regular: 85Sn:15Pb (Typ.) Pb-free: Matte Sn
JEDEC Outline Reference	MS-026 Variation: BFB
Maximum lead coplanarity	0.003 inches (0.08mm)
Weight	1.3 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–6. 144-Pin TQFP Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
D	22.00 BSC		
D1	20.00 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	–	–
b	0.17	0.22	0.27
c	0.09	–	0.20
e	0.50 BSC		
θ	0°	3.5°	7°

Table 15–10. 240-Pin PQFP Package Outline Dimensions (Part 2 of 2)			
Symbol	Millimeter		
	Min.	Nom.	Max.
e	0.50 BSC		
θ	0°	3.5°	8°

Figure 15–3 shows a 240-pin PQFP package outline.

Figure 15–3. 240-pin PQFP Package Outline