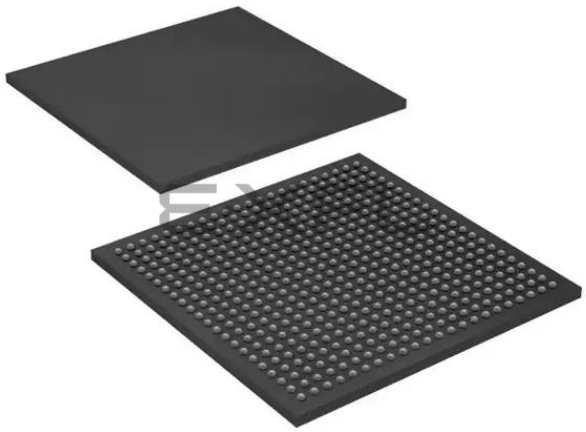

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Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	294
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f484c7n

Table 2–17. Cyclone II Supported I/O Standards & Constraints (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level		Top & Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
Differential HSTL-15 class I or class II	Pseudo differential *(4)*	*(5)*	1.5 V				✓ *(7)*	
		1.5 V	*(5)*	✓ *(6)*		✓ *(6)*		
Differential HSTL-18 class I or class II	Pseudo differential *(4)*	*(5)*	1.8 V				✓ *(7)*	
		1.8 V	*(5)*	✓ *(6)*		✓ *(6)*		
LVDS	Differential	2.5 V	2.5 V	✓	✓	✓	✓	✓
RSDS and mini-LVDS *(8)*	Differential	*(5)*	2.5 V		✓		✓	✓
LVPECL *(9)*	Differential	3.3 V/ 2.5 V/ 1.8 V/ 1.5 V	*(5)*	✓		✓		

Notes to Table 2–17:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.
(2) These pins support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.
(3) PCI-X does not meet the IV curve requirement at the linear region. PCI-clamp diode is not available on top and bottom I/O pins.
(4) Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Pseudo-differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them.
(5) This I/O standard is not supported on these I/O pins.
(6) This I/O standard is only supported on the dedicated clock pins.
(7) `PLL_OUT` does not support differential SSTL-18 class II and differential 1.8 and 1.5-V HSTL class II.
(8) mini-LVDS and RSDS are only supported on output pins.
(9) LVPECL is only supported on clock inputs.

For more information on Cyclone II supported I/O standards, see the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

High-Speed Differential Interfaces

Cyclone II devices can transmit and receive data through LVDS signals at a data rate of up to 640 Mbps and 805 Mbps, respectively. For the LVDS transmitter and receiver, the Cyclone II device's input and output pins support serialization and deserialization through internal logic.

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 4 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.8V_HSTL_ CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_HSTL_ CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
1.5V_HSTL_ CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
DIFFERENTIAL_ SSTL_2_CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
DIFFERENTIAL_ SSTL_2_CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps

Table 5–56. Maximum DCD for SDR Output on Column I/O Notes (1), (2) *(Part 2 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
2.5-V	140	140	155	ps
1.8-V	115	115	165	ps
1.5-V	745	745	770	ps
SSTL-2 Class I	60	60	75	ps
SSTL-2 Class II	60	60	80	ps
SSTL-18 Class I	60	130	130	ps
SSTL-18 Class II	60	135	135	ps
HSTL-18 Class I	60	115	115	ps
HSTL-18 Class II	75	75	100	ps
HSTL-15 Class I	150	150	150	ps
HSTL-15 Class II	135	135	155	ps
Differential SSTL-2 Class I	60	60	75	ps
Differential SSTL-2 Class II	60	60	80	ps
Differential SSTL-18 Class I	60	130	130	ps
Differential SSTL-18 Class II	60	135	135	ps
Differential HSTL-18 Class I	60	115	115	ps
Differential HSTL-18 Class II	75	75	100	ps
Differential HSTL-15 Class I	150	150	150	ps
Differential HSTL-15 Class II	135	135	155	ps
LVDS	60	60	60	ps
Simple RSDS	60	70	70	ps
Mini-LVDS	60	60	60	ps

Notes to Table 5–56:

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

Table 5–57. Maximum for DDIO Output on Row Pins with PLL in the Clock Path Notes (1), (2) *(Part 1 of 2)*

Row Pins with PLL in the Clock Path	C6	C7	C8	Unit
LVCMOS	270	310	310	ps
LVTTL	285	305	335	ps
2.5-V	180	180	220	ps
1.8-V	165	175	205	ps

7. PLLs in Cyclone II Devices

CII51007-3.1

Introduction

Cyclone® II devices have up to four phase-locked loops (PLLs) that provide robust clock management and synthesis for device clock management, external system clock management, and I/O interfaces. Cyclone II PLLs are versatile and can be used as a zero delay buffer, a jitter attenuator, a low skew fan out buffer, or a frequency synthesizer.

Each Cyclone II device has up to four PLLs, supporting advanced capabilities such as clock switchover and programmable switchover. These PLLs offer clock multiplication and division, phase shifting, and programmable duty cycle and can be used to minimize clock delay and clock skew, and to reduce or adjust clock-to-out (t_{CO}) and set-up (t_{SU}) times.

Cyclone II devices also support a power-down mode where unused clock networks can be turned off. The Altera® Quartus® II software enables the PLLs and their features without requiring any external devices.

Cyclone II PLLs have been characterized to operate in the commercial junction temperature range (0° to 85° C), the industrial junction temperature range (-40° to 100° C) and the extended temperature range (-40° to 125° C).

Table 7–1 shows the PLLs available in each Cyclone II device.

Table 7–1. Cyclone II Device PLL Availability

Device	PLL1	PLL2	PLL3	PLL4
EP2C5	✓	✓		
EP2C8	✓	✓		
EP2C15	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓

Phase-Shifting Implementation

Cyclone II devices use fine or coarse phase shifts for clock delays because they are more efficient than delay elements and are independent of process, voltage, and temperature.

Phase shift is implemented by using a combination of the VCO phase output and the counter starting time. The VCO phase taps and counter starting time are independent of process, voltage, and temperature. The VCO phase taps allow you to phase shift the Cyclone II PLL output clocks with fine resolution. The counter starting time allows you to phase shift the Cyclone II PLL output clocks with coarse resolution.

Fine-resolution phase shifting is implemented using any of the eight VCO phases for the output counters (`c[2..0]`) or the feedback counter (*m*) reference clock. This provides the finest resolution for phase shift. The minimum delay time that may be inserted using this method is defined by the equation:

$$\Delta t_{FINE} = \frac{1}{8} t_{VCO} = \frac{1}{8 \times f_{VCO}} = \frac{n}{8 \times m \times f_{IN}}$$

f_{IN} is input reference clock frequency.

For example, if f_{IN} is 100 MHz, *n* is 1 and *m* is 8, then f_{VCO} is 800 MHz and Δt is 156.25 ps. This delay time is defined by the PLL operating frequency which is governed by the reference clock and the counter settings.

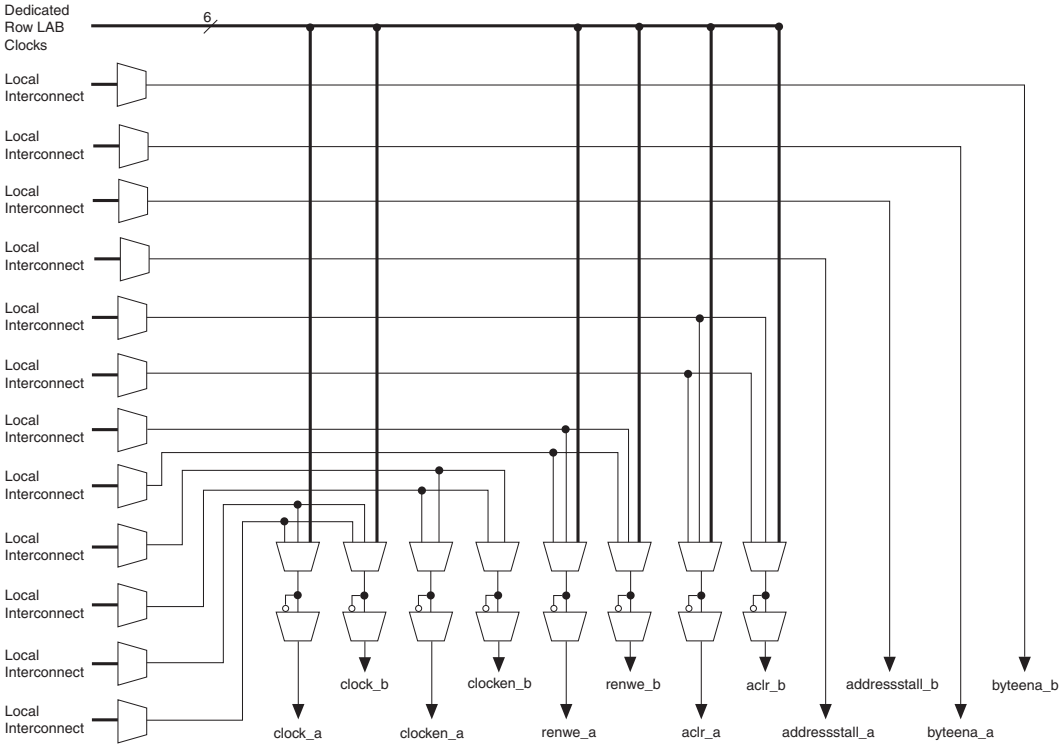
The second way to implement phase shifts is by delaying the start of the *m* and post-scale counters for a predetermined number of counter clocks. This delay time may be expressed as:

$$\Delta t_{COARSE} = \frac{S - 1}{f_{VCO}} = \frac{(S - 1) \times n}{m \times f_{IN}}$$

where S is the value set for the counter starting time. The counter starting time is called the **Initial** setting in the PLL Usage section of the compilation report in the Quartus II software.

Figure 7–8 shows an example of delay insertion using these two methods. The eight phases from the VCO are shown and labeled for reference. For this example, `OUTCLK0` is based off the 0° phase from the VCO and has the S value for the counter set to 1. It is divided by 4 (two VCO clocks for high time and two VCO clocks for low time). `OUTCLK1` is based off the 135° phase tap from the VCO and also has the S value for the counter set to 1. It is also divided by 4. In this case, the two clocks are offset by three

Figure 8–1. M4K Control Signal Selection



Parity Bit Support

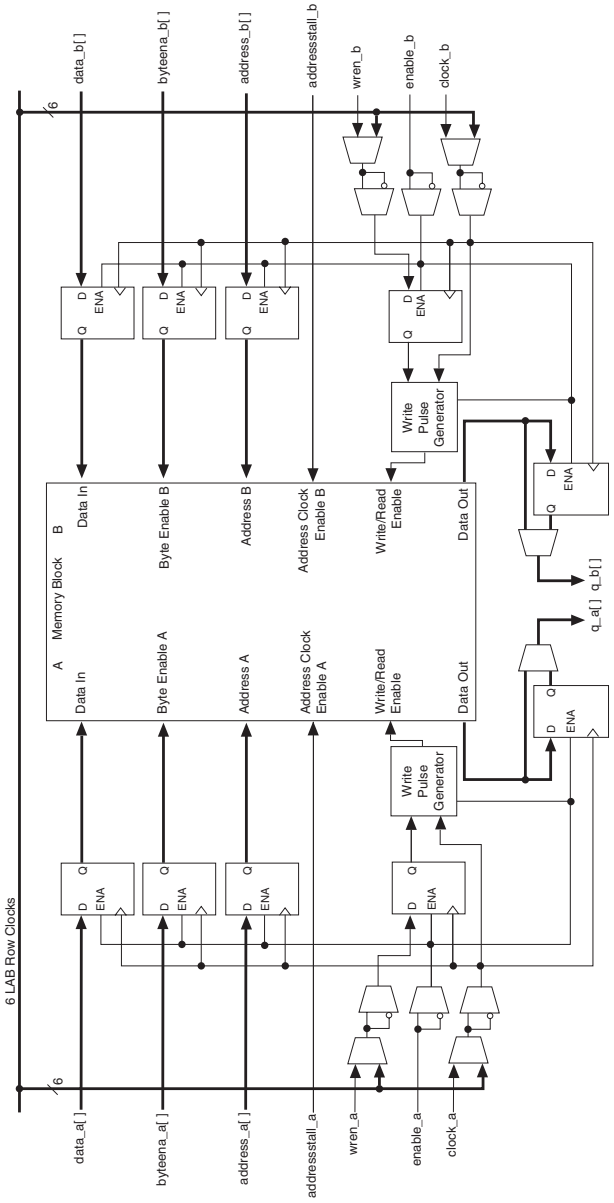
Error detection using parity check is possible using the parity bit, with additional logic implemented in LEs to ensure data integrity. Parity-size data words can also be used for other purposes such as storing user-specified control bits.

Refer to the *Using Parity to Detect Errors White Paper* for more information.

Byte Enable Support

All M4K memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable (`wren`) signals, along with the byte enable (`byteena`) signals, control the RAM block's write operations. The default value for the byte enable signals is high (enabled), in which

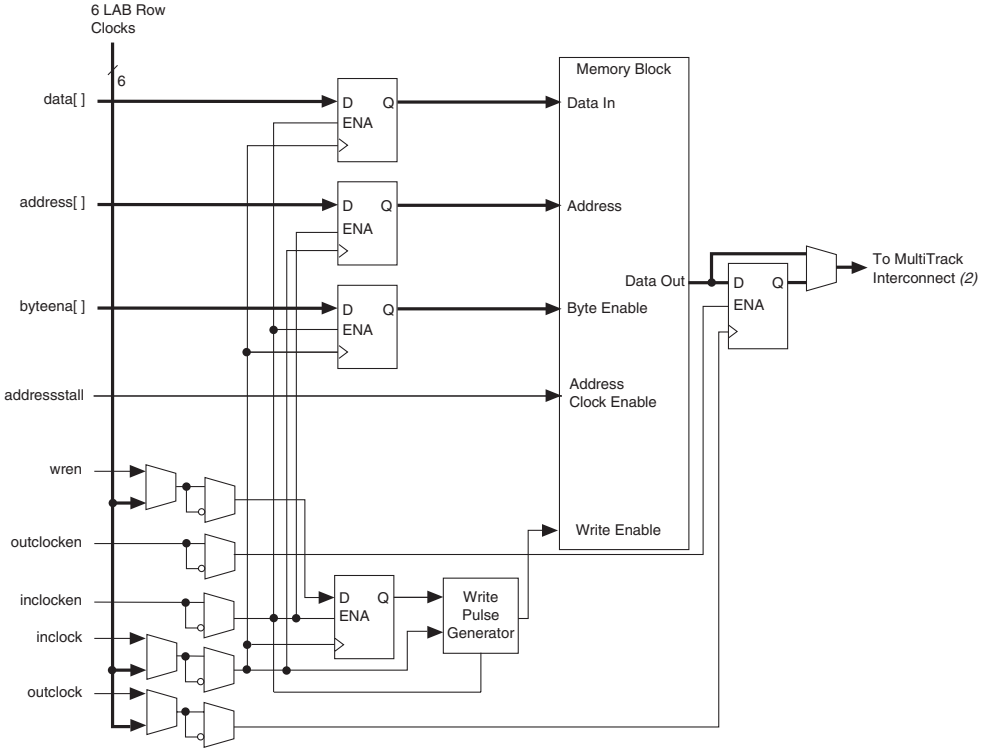
Figure 8–13. Cyclone II Memory Block in Independent Clock Mode *Note (1)*



Note to Figure 8–13:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Figure 8–16. Cyclone II Input/Output Clock Mode in Single-Port Mode *Notes (1), (2)*



Notes to Figure 8–16:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

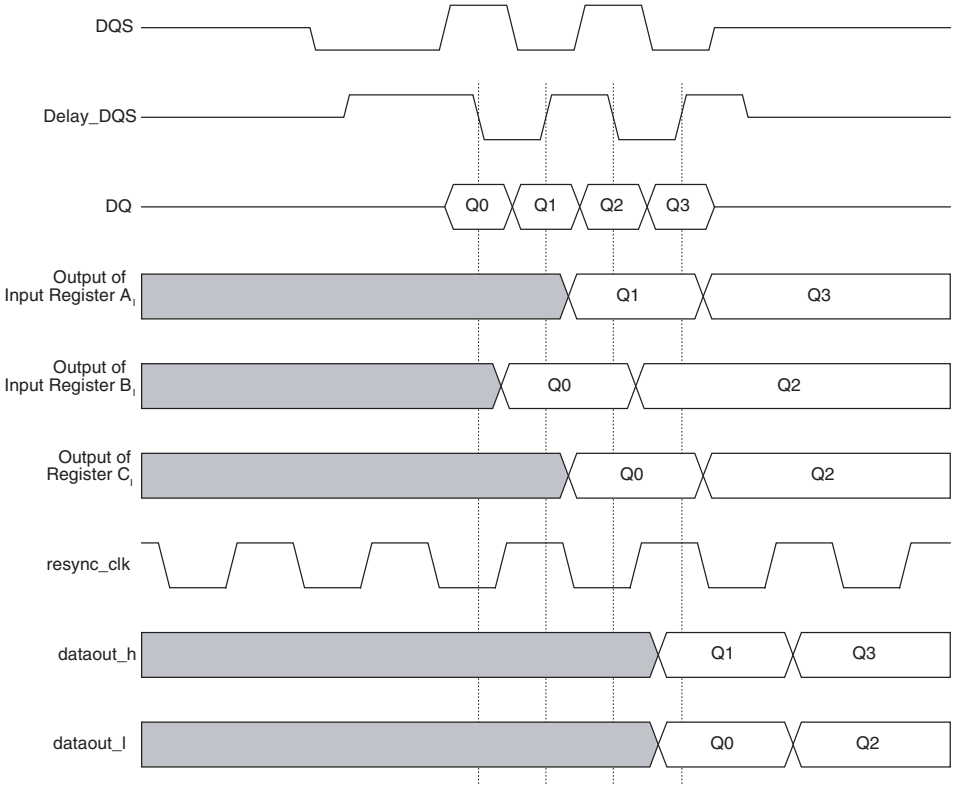
(2) For more information about the MultiTrack interconnect, refer to *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Read/Write Clock Mode

Cyclone II memory blocks can implement read/write clock mode for simple dual-port memory. The write clock controls the blocks' data inputs, write address, and write enable signals. The read clock controls the data output, read address, and read enable signals. The memory blocks support independent clock enables for each clock for the read- and write-side registers. This mode does not support asynchronous clear signals for the registers. Figure 8–17 shows a memory block in read/write clock mode.

Registers sync_reg_h and sync_reg_l synchronize the two data streams to the rising edge of the resynchronization clock. Figure 9–12 shows examples of functional waveforms from a double data rate input implementation.

Figure 9–12. DDR Input Functional Waveforms



The Cyclone II DDR input registers require you to invert the incoming DQS signal to ensure proper data transfer. The altdq megafunction automatically adds the inverter on the clock port of the DQ signals. As shown in Figure 9–11, the inverted DQS signal's rising edge clocks register A_I, its falling edge clocks register B_I, and register C_I aligns the data clocked by register B_I with register A_I on the inverted DQS signal's rising edge. In a DDR memory read operation, the last data coincides with the falling edge of DQS signal. If you do not invert the DQS pin, you do not get this last data because the register does not latch until the next rising edge of the DQS signal.

Pseudo-Differential SSTL-18 Class I and Differential SSTL-18 Class II

The 1.8-V differential SSTL-18 standard is formulated under JEDEC Standard, JESD8-15: Stub Series Terminated Logic for 1.8V (SSTL-18).

The differential SSTL-18 I/O standard is a 1.8-V standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard supports differential signals in systems using the SSTL-18 standard and supplements the SSTL-18 standard for differential clocks. Refer to Figures 10–9 and 10–10 for details on differential SSTL-18 termination.

Cyclone II devices do not support true differential SSTL-18 standards. Cyclone II devices support pseudo-differential SSTL-18 outputs for `PLL_OUT` pins and pseudo-differential SSTL-18 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

Figure 10–9. Differential SSTL-18 Class I Termination

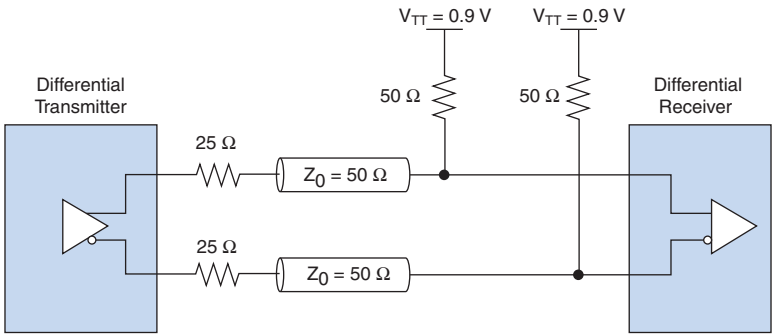
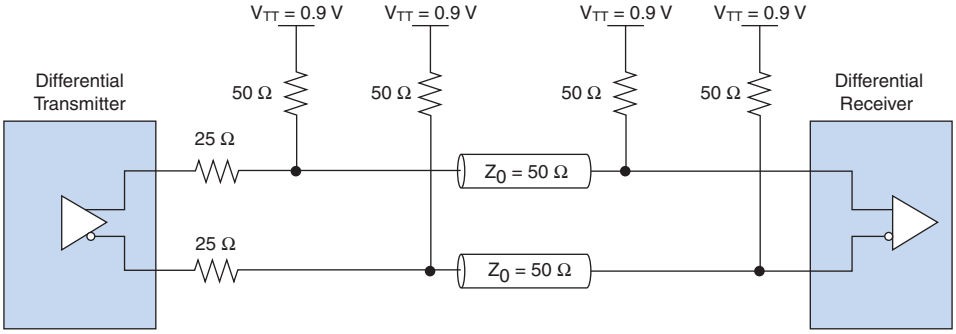


Figure 10–10. Differential SSTL-18 Class II Termination

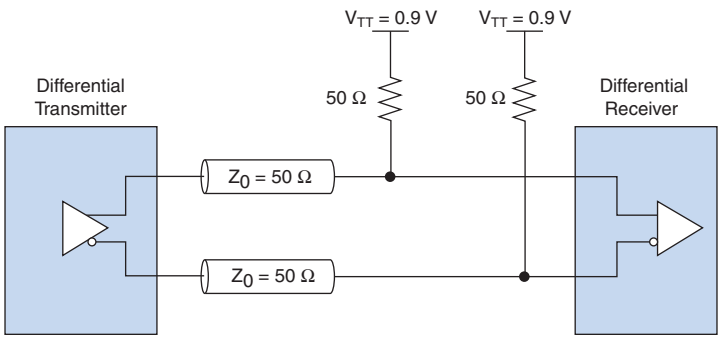


1.8-V Pseudo-Differential HSTL Class I and II

The 1.8-V differential HSTL specification is the same as the 1.8-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0 to 1.8-V HSTL logic switching range such as QDR memory clock interfaces. Cyclone II devices support both input and output levels. Refer to Figures 10–11 and 10–12 for details on 1.8-V differential HSTL termination.

Cyclone II devices do not support true 1.8-V differential HSTL standards. Cyclone II devices support pseudo-differential HSTL outputs for `PLL_OUT` pins and pseudo-differential HSTL inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential HSTL.

Figure 10–11. 1.8-V Differential HSTL Class I Termination



Additionally, each Cyclone II I/O bank has its own VCCIO pins. Any single I/O bank can only support one V_{CCIO} setting from among 1.5, 1.8, 2.5 or 3.3 V. Although there can only be one V_{CCIO} voltage per I/O bank, Cyclone II devices permit additional input signaling capabilities, as shown in Table 10–4.

Table 10–4. Acceptable Input Levels for LVTTL and LVCMOS

Bank V_{CCIO} (V)	Acceptable Input Levels (V)			
	3.3	2.5	1.8	1.5
3.3	✓	✓ (1)		
2.5	✓	✓		
1.8	✓ (2)	✓ (2)	✓	✓ (1)
1.5	✓ (2)	✓ (2)	✓	✓

Notes to Table 10–4:

(1) Because the input level does not drive to the rail, the input buffer does not completely shut off, and the I/O current is slightly higher than the default value.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on **Allow voltage overdrive for LVTTL/LVCMOS input pins** in Settings > Device > Device and Pin Options > Pin Placement tab. This setting allows input pins with LVTTL or LVCMOS I/O standards to be placed by the Quartus II software in an I/O bank with a lower V_{CCIO} voltage than the voltage specified by the pins.

Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank as long as they use compatible V_{CCIO} levels for input and output pins. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V LVTTL inputs and outputs, 2.5-V LVDS-compatible inputs and outputs, and 3.3-V LVCMOS inputs only.

Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value. For example, if you choose to implement both SSTL-2 and SSTL-18 in your Cyclone II device, I/O pins using these standards—because they require different V_{REF} values—must be in different banks from each other. However, the same I/O bank can support SSTL-2 and 2.5-V LVCMOS with the V_{CCIO} set to 2.5 V and the V_{REF} set to 1.25 V.

Refer to "Pad Placement and DC Guidelines" on page 10–27 for more information.

V_{REF} Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply and to prevent output switching noise from shifting the V_{REF} rail, there are restrictions on the placement of single-ended voltage referenced I/Os with respect to V_{REF} pads and VCCIO and ground pairs. Use the following guidelines for placing single-ended pads in Cyclone II devices.

The Quartus II software automatically does all the calculations in this section.

Input Pads

Each V_{REF} pad supports up to 15 input pads on each side of the V_{REF} pad for FineLine BGA devices. Each V_{REF} pad supports up to 10 input pads on each side of the V_{REF} pad for quad flat pack (QFP) devices. This is irrespective of VCCIO and ground pairs, and is guaranteed by the Cyclone II architecture.

Output Pads

When a voltage referenced input or bidirectional pad does not exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each VCCIO and ground pair supports 9 output pins for Fineline BGA packages (not more than 9 output pins per 12 consecutive row I/O pins) or 5 output pins for QFP packages (not more than 5 output pins per 12 consecutive row I/O pins or 8 consecutive column I/O pins). Any non-SSTL and non-HSTL output can be no closer than two pads away from a V_{REF} pad. Altera recommends that any SSTL or HSTL output, except for pintable defined DQ and DQS outputs, to be no closer than two pads away from a V_{REF} pad to maintain acceptable noise levels.

Quartus II software will not check for the SSTL and HSTL output pads placement rule.

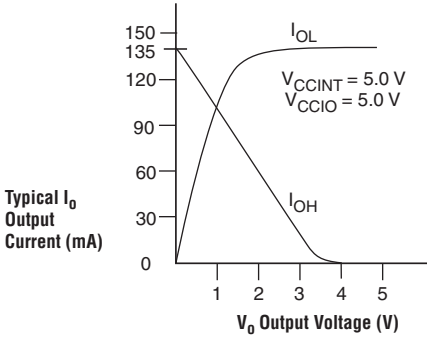
Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

Bidirectional Pads

Bidirectional pads must satisfy input and output guidelines simultaneously.

Refer to "DDR and QDR Pads" on page 10–32 for details about guidelines for DQ and DQS pads placement.

Figure 10–22. Output Drive Characteristics of a 5.0-V Device



As shown above, R_1 = 5.0-V/135 mA.

The values shown in data sheets usually reflect typical operating conditions. Subtract 20% from the data sheet value for guard band. This subtraction when applied in the example in Figure 10–22 gives R_1 a value of 30 Ω

R_2 should be selected so that it does not violate the driving device's I_{OH} specification. For example, if the device has a maximum I_{OH} of 8 mA, given that the PCI clamping diode, $V_{IN} = V_{CCIO} + 0.7\text{-V} = 3.7\text{-V}$, and the maximum supply load of a 5.0-V device (V_{CC}) is 5.25-V, the value of R_2 can be calculated as follows:

$$R_2 = \frac{(5.25\ V - 3.7\ V) - (8\ mA \times 30\ \Omega)}{8\ mA} = 164\ \Omega$$

This analysis assumes worst case conditions. If your system does not have a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because 5.0-V device tolerance in Cyclone II devices requires use of the PCI clamp, and this clamp is activated during configuration, 5.0-V signals may not be driven into the device until it is configured.

Conclusion

Cyclone II device I/O capabilities enable you to keep pace with increasing design complexity utilizing a low-cost FPGA device family. Support for I/O standards including SSTL and LVDS compatibility allow Cyclone II devices to fit into a wide variety of applications. The Quartus II

RSDS I/O Standard Support in Cyclone II Devices

The RSDS specification is used in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the National Semiconductor Corporation RSDS Interface Specification and support the RSDS output standard. Table 11–2 shows the RSDS electrical characteristics for Cyclone II devices.

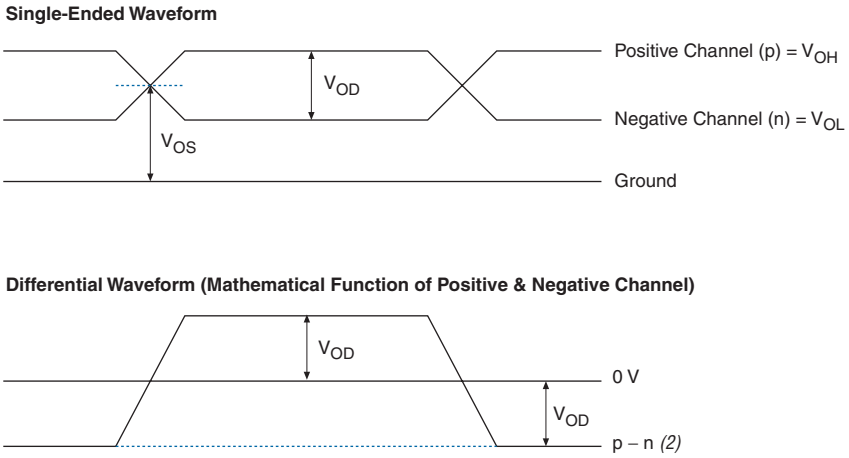
Table 11–2. RSDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	100		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
T_r/T_f	Transition time	20% to 80%		500		ps

Notes to Table 11–2:
(1) The specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

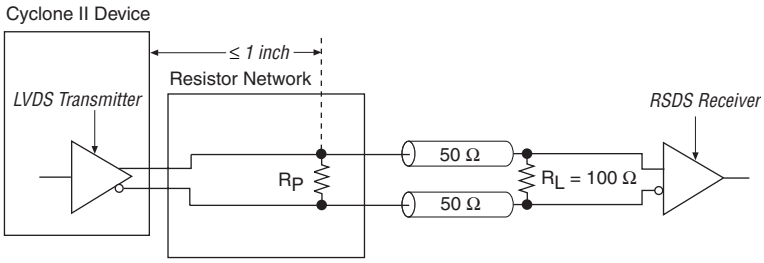
Figure 11–6 shows the RSDS transmitter output signal waveforms.

Figure 11–6. Transmitter Output Signal Level Waveforms for RSDS *Note (1)*



Notes to Figure 11–6:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 11–8. RSDS Single Resistor Network *Note (1)*



Note to Figure 11–8:
(1) R_p = 100 Ω

RSDS Software Support

When designing for the RSDS I/O standard, assign the RSDS I/O standard to the I/O pins intended for RSDS in the Quartus® II software. Contact Altera Applications for reference designs.

mini-LVDS Standard Support in Cyclone II Devices

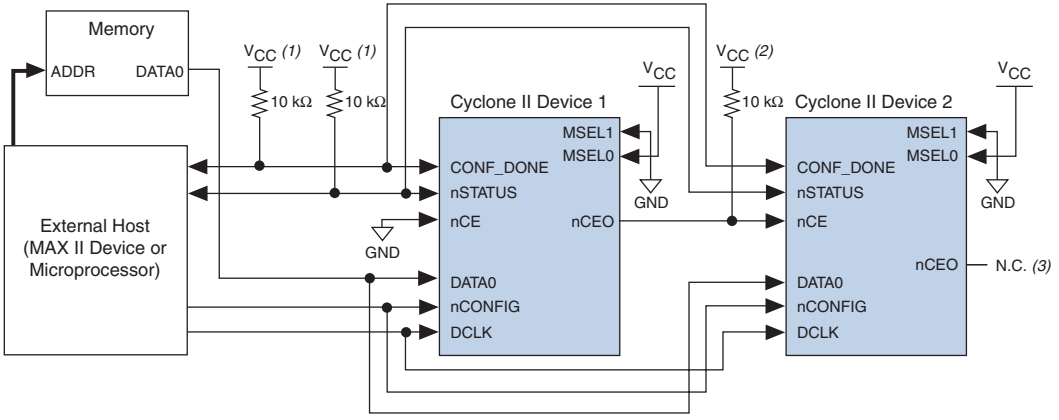
The mini-LVDS specification defines its use in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the Texas Instruments mini-LVDS Interface Specification and support the mini-LVDS output standard. Table 11–3 shows the mini-LVDS electrical characteristics for Cyclone II devices.

Table 11–3. mini-LVDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	300		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1125	1250	1375	mV
T_r / T_f	Transition time	20% to 80%			500	ps

Notes to Table 11–3:
(1) The V_{OD} specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

Figure 13–10. Multiple Device PS Configuration Using an External Host



Notes to Figure 13–10:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

In multiple device PS configuration, connect the first Cyclone II device's nCE pin to GND and connect the nCEO pin to the nCE pin of the next Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's nCEO pin high to its V_{CCIO} level to help the internal weak pull-up resistor when the nCEO pin feeds next Cyclone II device's nCE pin. The input to the nCE pin of the last Cyclone II device in the chain comes from the previous Cyclone II device. After the first device completes configuration in a multiple device configuration chain, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle. Therefore, the MAX II device begins to transfer data to the next Cyclone II device without interruption. The nCEO pin is a dual-purpose pin in Cyclone II devices. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in chain is a Cyclone II device.

The Quartus II software sets the Cyclone II device nCEO pin as a dedicated output by default. If the nCEO pin feeds the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

Table 13–13 describes the dedicated JTAG pins. JTAG pins must be kept stable before and during configuration to prevent accidental loading of JTAG instructions. The TCK pin has a weak internal pull-down resistor and the TDI and TMS JTAG input pins have weak internal pull-up resistors.

Table 13–13. Dedicated JTAG Pins

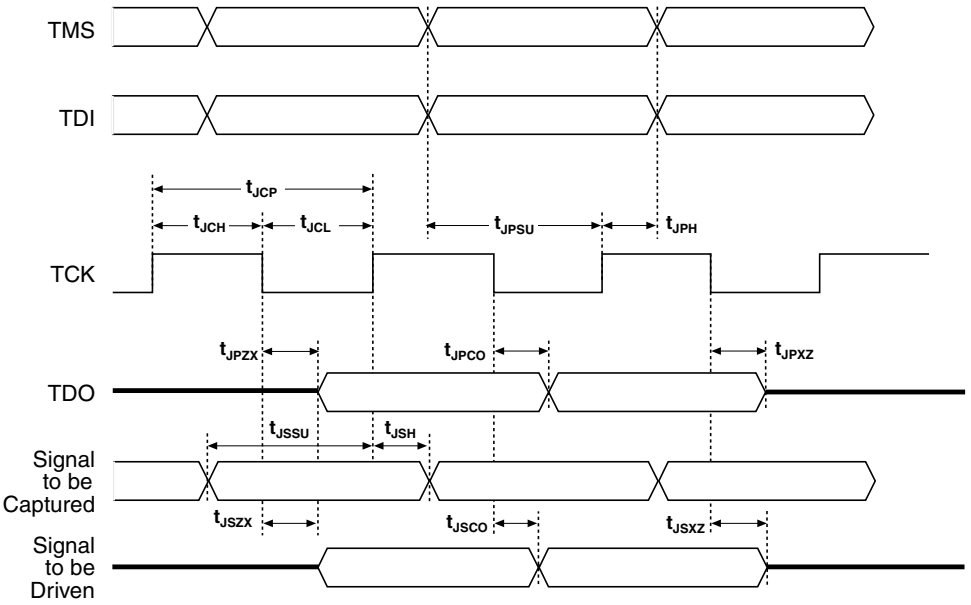
Pin Name	User Mode	Pin Type	Description
TDI	N/A	Input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.
TDO	N/A	Output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.
TMS	N/A	Input	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.
TCK	N/A	Input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to GND. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.

Conclusion

Cyclone II devices can be configured in AS, PS or JTAG configuration schemes to fit your system's need. The AS configuration scheme supported by Cyclone II devices can now operate at a higher DCLK

When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with IDCODE as the initial instruction. At device power-up, the TAP controller starts in this TEST_LOGIC/RESET state. In addition, forcing the TAP controller to the TEST_LOGIC/RESET state is done by holding TMS high for five TCK clock cycles. Once in the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS is held high (while TCK is clocked). Figure 14–6 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 14–6. IEEE Std. 1149.1 Timing Waveforms



To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin. The waveform diagram in Figure 14–7 represents the entry of the instruction code into the instruction register. It shows the values of TCK, TMS, TDI, TDO, and the states of the TAP controller. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP controller to SHIFT_IR.

Table 15–10. 240-Pin PQFP Package Outline Dimensions (Part 2 of 2)			
Symbol	Millimeter		
	Min.	Nom.	Max.
e	0.50 BSC		
θ	0°	3.5°	8°

Figure 15–3 shows a 240-pin PQFP package outline.

Figure 15–3. 240-pin PQFP Package Outline