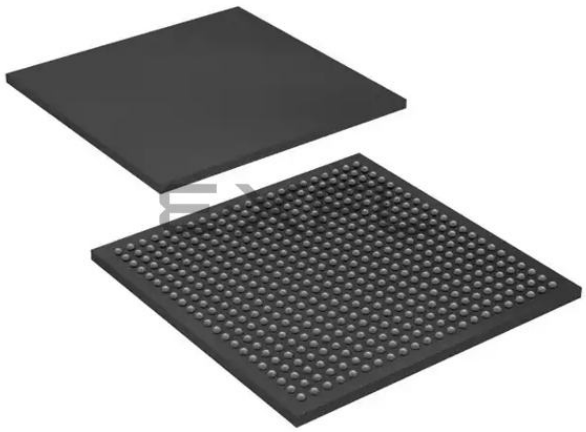


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	294
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f484i8

Chapter 14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

- 133-MHz PCI-X 1.0 specification compatibility
- High-speed external memory support, including DDR, DDR2, and SDR SDRAM, and QDRII SRAM supported by drop in Altera IP MegaCore functions for ease of use
- Three dedicated registers per I/O element (IOE): one input register, one output register, and one output-enable register
- Programmable bus-hold feature
- Programmable output drive strength feature
- Programmable delays from the pin to the IOE or logic array
- I/O bank grouping for unique VCCIO and/or VREF bank settings
- MultiVolt™ I/O standard support for 1.5-, 1.8-, 2.5-, and 3.3-interfaces
- Hot-socketing operation support
- Tri-state with weak pull-up on I/O pins before and during configuration
- Programmable open-drain outputs
- Series on-chip termination support

Flexible clock management circuitry

- Hierarchical clock network for up to 402.5-MHz performance
- Up to four PLLs per device provide clock multiplication and division, phase shifting, programmable duty cycle, and external clock outputs, allowing system-level clock management and skew control
- Up to 16 global clock lines in the global clock network that drive throughout the entire device

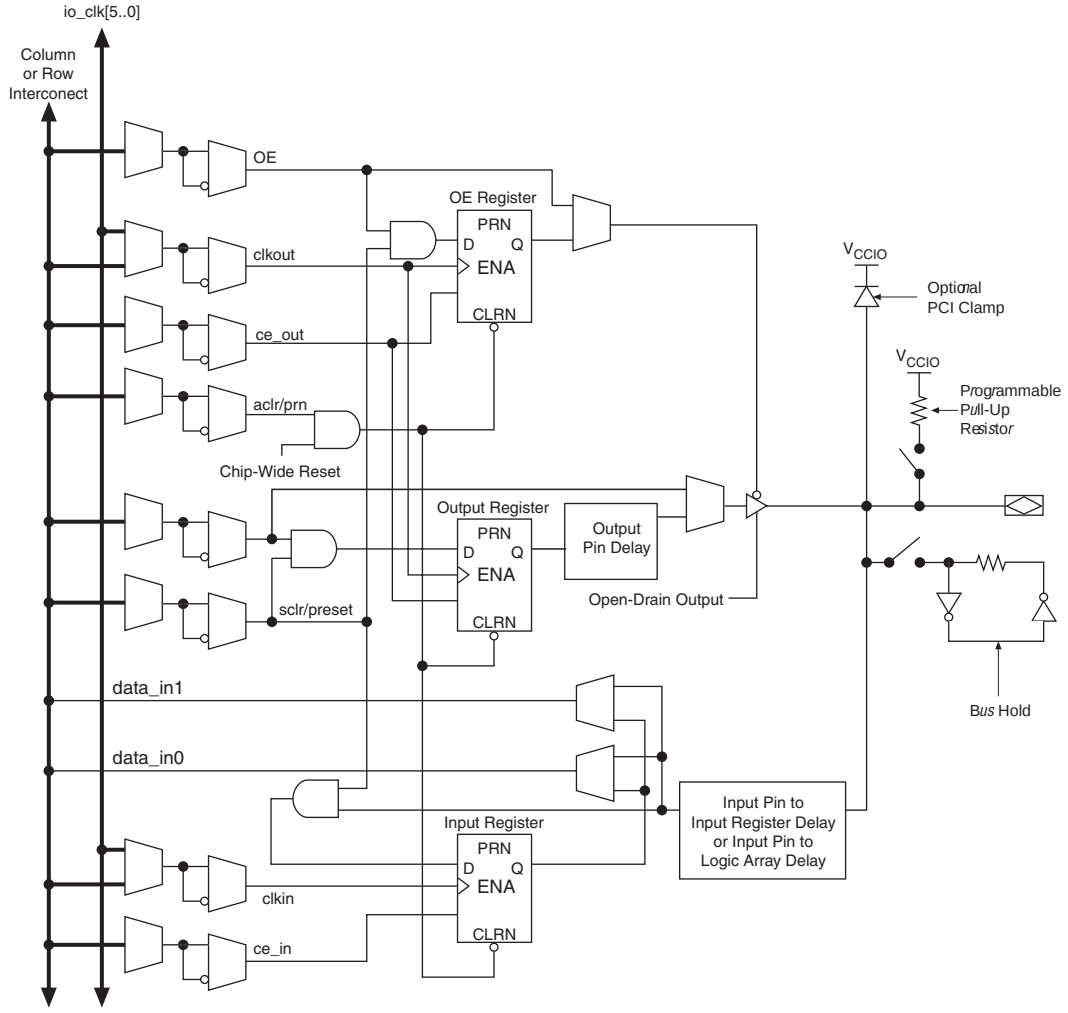
Device configuration

- Fast serial configuration allows configuration times less than 100 ms
- Decompression feature allows for smaller programming file storage and faster configuration times
- Supports multiple configuration modes: active serial, passive serial, and JTAG-based configuration
- Supports configuration through low-cost serial configuration devices
- Device configuration supports multiple voltages (either 3.3, 2.5, or 1.8 V)

Intellectual property

- Altera megafunction and Altera MegaCore function support, and Altera Megafunctions Partners Program (AMPP^{SM}) megafunction support, for a wide range of embedded processors, on-chip and off-chip interfaces, peripheral functions, DSP functions, and communications functions and

Figure 2–25. Cyclone II IOE in Bidirectional I/O Configuration



The Cyclone II device IOE includes programmable delays to ensure zero hold times, minimize setup times, or increase clock to output times.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays decrease input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time.

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI). Cyclone II devices support the RSDS and mini-LVDS I/O standards at data rates up to 311 Mbps at the transmitter.

A subset of pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. The dual-purpose LVDS pins require an external-resistor network at the transmitter channels in addition to 100- termination resistors on receiver channels. These pins do not contain dedicated serialization or deserialization circuitry. Therefore, internal logic performs serialization and deserialization functions.

Cyclone II pin tables list the pins that support the high-speed I/O interface. The number of LVDS channels supported in each device family member is listed in Table 2–18.

Table 2–18. Cyclone II Device LVDS Channels (Part 1 of 2)

Device	Pin Count	Number of LVDS Channels (1)
EP2C5	144	31 (35)
	208	56 (60)
	256	61 (65)
EP2C8	144	29 (33)
	208	53 (57)
	256	75 (79)
EP2C15	256	52 (60)
	484	128 (136)
EP2C20	240	45 (53)
	256	52 (60)
	484	128 (136)
EP2C35	484	131 (139)
	672	201 (209)
EP2C50	484	119 (127)
	672	189 (197)

Table 3–1. Cyclone II JTAG Instructions (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
CONFIG_IO	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the device is reconfigured.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Note to Table 3–1:
(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The Quartus II software has an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. In the **Settings** dialog box in the Assignments menu, click **Device & Pin Options**, then **General,** and then turn on the **Auto Usercode option**.

Devices Can Be Driven before Power-Up

You can drive signals into the I/O pins, dedicated input pins, and dedicated clock pins of Cyclone II devices before or during power-up or power-down without damaging the device. Cyclone II devices support any power-up or power-down sequence (V_{CCIO} and V_{CCINT}) to simplify system level design.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot-socketing situation, the Cyclone II device's output buffers are turned off during system power-up or power-down. The Cyclone II device also does not drive out until the device is configured and has attained proper operating conditions. The I/O pins are tri-stated until the device enters user mode with a weak pull-up resistor (R) to 3.3V. Refer to Figure 4–1 for more information.

1 You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. The V_{CCIO} and V_{CCINT} must have monotonic rise to their steady state levels. (Refer to Figure 4–3 for more information.) The power supply ramp rates can range from 100 µs to 100 ms for non "A" devices. Both V_{CC} supplies must power down within 100 ms of each other to prevent I/O pins from driving out. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF. Cyclone II devices meet the following hot-socketing specification.

The hot-socketing DC specification is $| I_{IOPIN} | < 300$ µA.
The hot-socketing AC specification is $| I_{IOPIN} | < 8$ mA for 10 ns or less.

This specification takes into account the pin capacitance but not board trace and external loading capacitance. You must consider additional capacitance for trace, connector, and loading separately.

I_{IOPIN} is the current at any user I/O pin on the device. The DC specification applies when all V_{CC} supplies to the device are stable in the powered-up or powered-down conditions. For the AC specification, the peak current duration due to power-up transients is 10 ns or less.

A possible concern for semiconductor devices in general regarding hot socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins may be connected and driven by the active system before

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 1 of 2)

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Unit
V_{IN}	Input voltage	(1), (2)		–0.5	—	4.0	V
I_i	Input pin leakage current	$V_{IN} = V_{CCIOmax}$ to 0 V (3)		–10	—	10	µA
V_{OUT}	Output voltage	—		0	—	V_{CCIO}	V
I_{OZ}	Tri-stated I/O pin leakage current	$V_{OUT} = V_{CCIOmax}$ to 0 V (3)		–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_{IN} = ground, no load, no toggling inputs T_J = 25° C Nominal V_{CCINT}	EP2C5/A	—	0.010	(4)	A
			EP2C8/A	—	0.017	(4)	A
			EP2C15A	—	0.037	(4)	A
			EP2C20/A	—	0.037	(4)	A
			EP2C35	—	0.066	(4)	A
			EP2C50	—	0.101	(4)	A
			EP2C70	—	0.141	(4)	A
I_{CCIO0}	V_{CCIO} supply current (standby)	V_{IN} = ground, no load, no toggling inputs T_J = 25° C V_{CCIO} = 2.5 V	EP2C5/A	—	0.7	(4)	mA
			EP2C8/A	—	0.8	(4)	mA
			EP2C15A	—	0.9	(4)	mA
			EP2C20/A	—	0.9	(4)	mA
			EP2C35	—	1.3	(4)	mA
			EP2C50	—	1.3	(4)	mA
			EP2C70	—	1.7	(4)	mA

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 2 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
2.5V	4 mA	t_{OP}	1208	1267	2478	2614	2743	2750	ps
		t_{DIP}	1340	1406	2648	2808	2969	2969	ps
	8 mA	t_{OP}	1190	1248	2307	2434	2554	2561	ps
		t_{DIP}	1322	1387	2477	2628	2780	2780	ps
	12 mA	t_{OP}	1154	1210	2192	2314	2430	2437	ps
		t_{DIP}	1286	1349	2362	2508	2656	2656	ps
	16 mA (1)	t_{OP}	1140	1195	2152	2263	2375	2382	ps
		t_{DIP}	1272	1334	2322	2457	2601	2601	ps
1.8V	2 mA	t_{OP}	1682	1765	3988	4279	4563	4570	ps
		t_{DIP}	1814	1904	4158	4473	4789	4789	ps
	4 mA	t_{OP}	1567	1644	3301	3538	3768	3775	ps
		t_{DIP}	1699	1783	3471	3732	3994	3994	ps
	6 mA	t_{OP}	1475	1547	2993	3195	3391	3398	ps
		t_{DIP}	1607	1686	3163	3389	3617	3617	ps
	8 mA	t_{OP}	1451	1522	2882	3074	3259	3266	ps
		t_{DIP}	1583	1661	3052	3268	3485	3485	ps
	10 mA	t_{OP}	1438	1508	2853	3041	3223	3230	ps
		t_{DIP}	1570	1647	3023	3235	3449	3449	ps
	12 mA (1)	t_{OP}	1438	1508	2853	3041	3223	3230	ps
		t_{DIP}	1570	1647	3023	3235	3449	3449	ps
1.5V	2 mA	t_{OP}	2083	2186	4477	4870	5256	5263	ps
		t_{DIP}	2215	2325	4647	5064	5482	5482	ps
	4 mA	t_{OP}	1793	1881	3649	3965	4274	4281	ps
		t_{DIP}	1925	2020	3819	4159	4500	4500	ps
	6 mA	t_{OP}	1770	1857	3527	3823	4112	4119	ps
		t_{DIP}	1902	1996	3697	4017	4338	4338	ps
	8 mA (1)	t_{OP}	1703	1787	3537	3827	4111	4118	ps
		t_{DIP}	1835	1926	3707	4021	4337	4337	ps

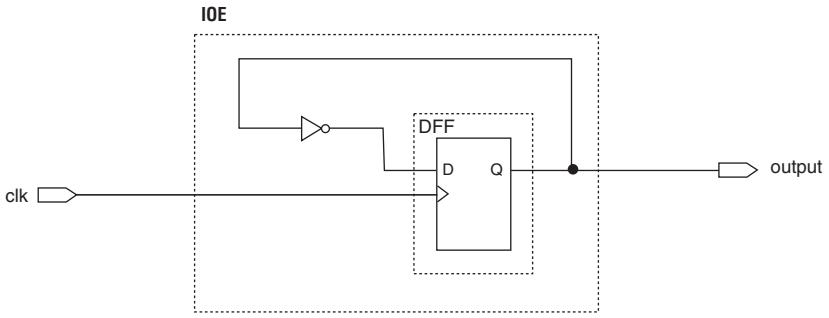
(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

DCD Measurement Techniques

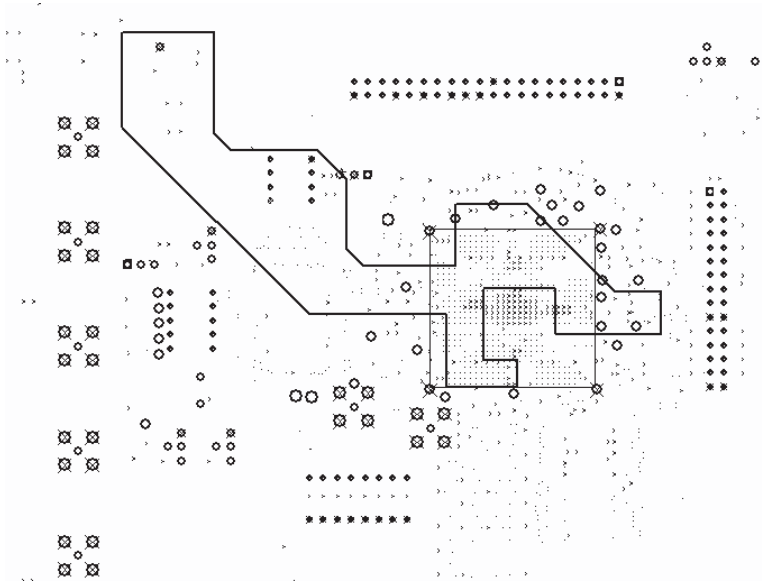
DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 5–9). Therefore, any DCD present on the input clock signal, or caused by the clock input buffer, or different input I/O standard, does not transfer to the output signal.

Figure 5–9. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs



However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 5–10). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

Figure 7–16. V_{CCINT} Plane Partitioned for VCCA Island



Thick VCCA Trace

Because of board constraints, you may not be able to partition a VCCA island. Instead, run a thick trace from the power supply to each VCCA pin. The traces should be at least 20 mils thick.

In each of these three cases, you should filter each VCCA pin with a decoupling circuit shown in Figure 7–17. Place a ferrite bead that exhibits high impedance at frequencies of 50 MHz or higher and a 10 µF tantalum parallel capacitor where the power enters the board. Decouple each VCCA pin with a 0.1 µF and 0.001 µF parallel combination of ceramic capacitors located as close as possible to the Cyclone II device. You can connect the GNDA pins directly to the same ground plane as the device's digital ground.

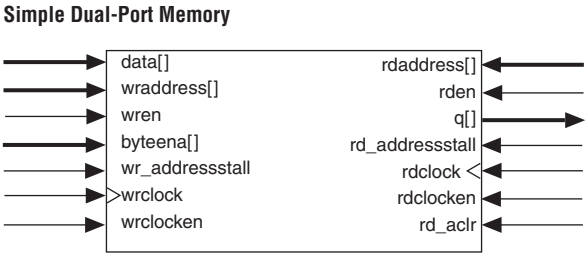
Document Revision History

Table 7–10 shows the revision history for this document.

Table 7–10. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	Added document revision history. Updated handpara note in "Introduction". Updated Note (3)in Table 7–2. Updated Figure 7–5. Updated "Control Signals" section. Updated "Thick VCCA Trace" section.	Updated chapter with extended temperature information. Updated `pllena` information in "Control Signals" section. Corrected capacitor unit from10-F to 10 µF.
December 2005 v2.2	Updated industrial temperature range	
November 2005 v2.1	Updated Figure 7–12. Updated Figure 7–17.	
July 2005 v2.0	Updated Table 7–6. Updated "Hardware Features" section. Updated "areset" section. Updated Table 7–8. Added "Board Layout" section.	
February 2005 v1.2	Updated information concerning signals. Added a note to Figures 7-9 through 7-13 regarding violating the setup or hold time on address registers.	
November, 2004 v1.1	Updated "Introduction" section.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Figure 8–8. Cyclone II Simple Dual-Port Mode Note (1)



Note to Figure 8–8:
(1) Simple dual-port RAM supports input and output clock mode in addition to the read and write clock mode shown.

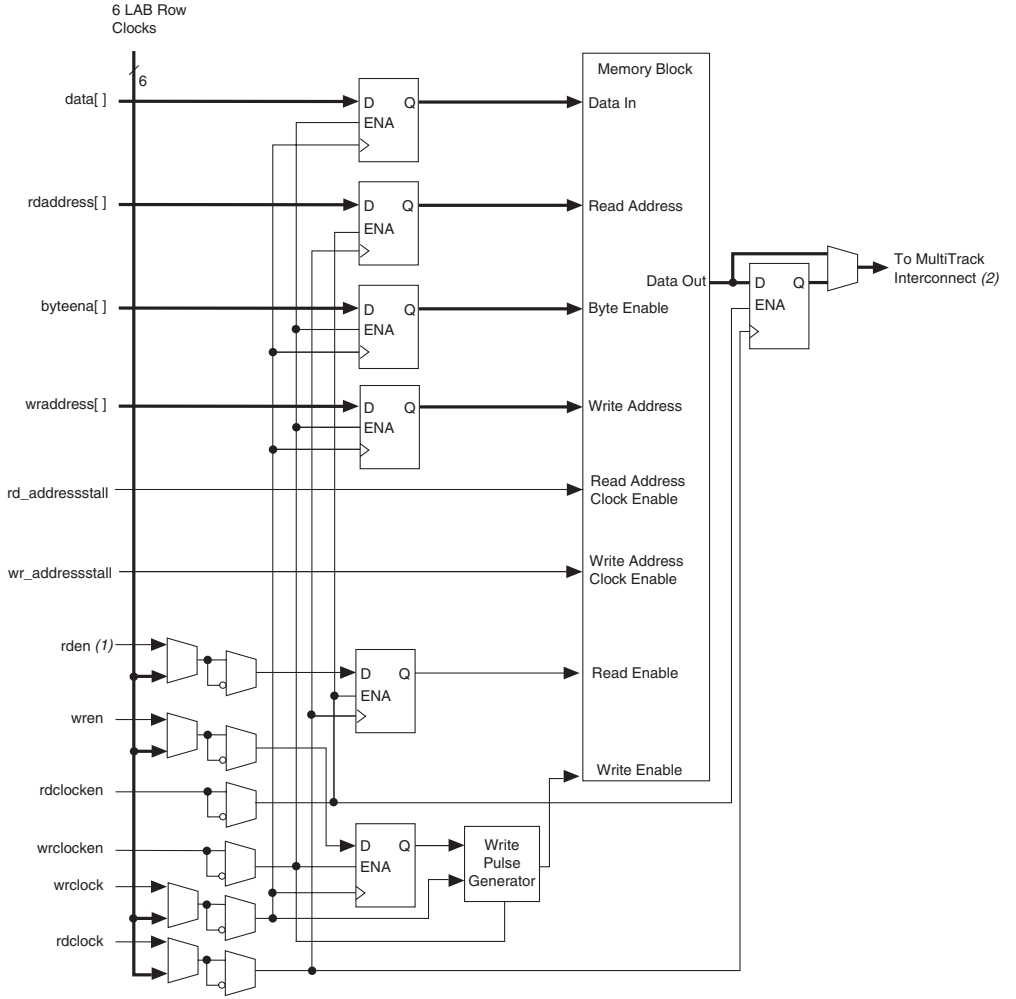
Cyclone II memory blocks support mixed-width configurations, allowing different read and write port widths. Tables 8–5 and 8–6 show the mixed-width configurations.

Table 8–5. Cyclone II Memory Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	v	v	v	v	v	v			
2K × 2	v	v	v	v	v	v			
1K × 4	v	v	v	v	v	v			
512 × 8	v	v	v	v	v	v			
256 × 16	v	v	v	v	v	v			
128 × 32	v	v	v	v	v	v			
512 × 9							v	v	v
256 × 18							v	v	v
128 × 36							v	v	v

In simple dual-port mode, the memory blocks have one write enable and one read enable signal. They do not support a clear port on the write enable and read enable registers. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is the old data stored at the memory

Figure 8–17. Cyclone II Read/Write Clock Mode Notes (1), (2)

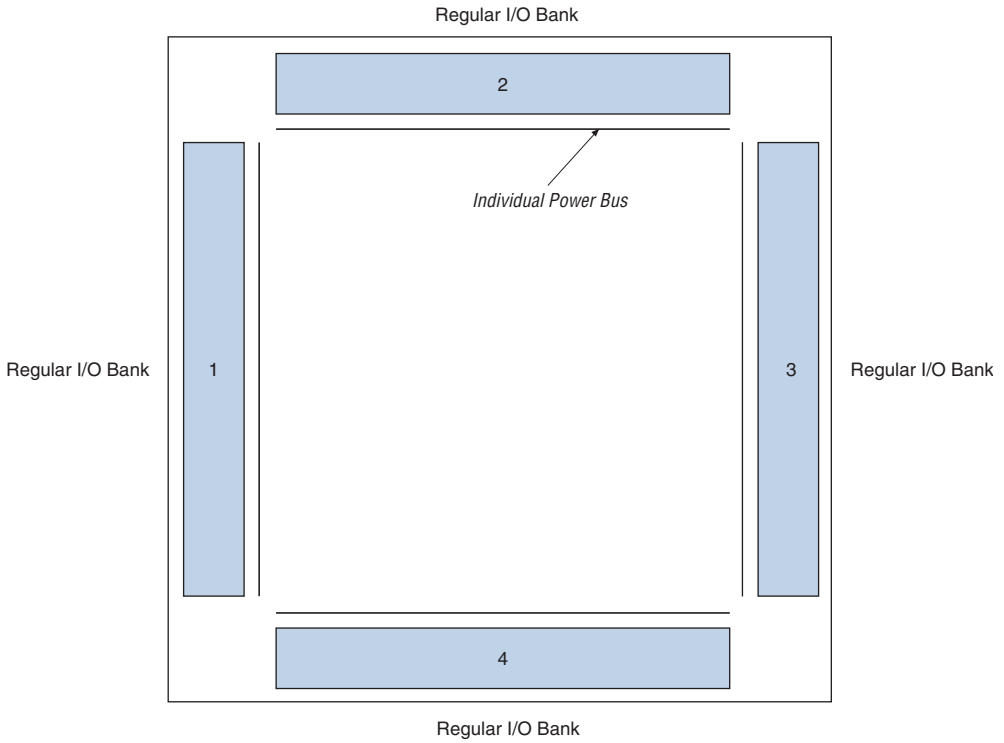


Notes to Figure 8–17:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) For more information about the MultiTract interconnect, refer to *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Figure 10–19. EP2C5 and EP2C8 Device I/O Banks Notes (1), (2)



Notes to Figure 10–19:

(1) This is a top view of the silicon die.

(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

I/O Driver Impedance Matching (R_S) and Series Termination (R_S)

Cyclone II devices support driver impedance matching to the impedance of the transmission line, typically 25 or 50 . When used with the output drivers, on-chip termination (OCT) sets the output driver impedance to 25 or 50 by choosing the driver strength. Once matching impedance is selected, driver current can not be changed. Table 10–7 provides a list of output standards that support impedance matching. All I/O banks and I/O pins support impedance matching and series termination. Dedicated configuration pins and JTAG pins do not support impedance matching or series termination.

Table 10–7. Selectable I/O Drivers with Impedance Matching and Series Termination

I/O Standard	Target R_S ( )
3.3-V LVTTL/CMOS	25 (1)
2.5-V LVTTL/CMOS	50 (1)
1.8-V LVTTL/CMOS	50 (1)
SSTL-2 class I	50 (1)
SSTL-18 class I	50 (1)

Note to Table 10–7:

(1) These RS values are nominal values. Actual impedance varies across process, voltage, and temperature conditions. Tolerance is specified in the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Handbook*.

Pad Placement and DC Guidelines

This section provides pad placement guidelines for the programmable I/O standards supported by Cyclone II devices and includes essential information for designing systems using the devices' selectable I/O capabilities. This section also discusses the DC limitations and guidelines.

Quartus II software provides user controlled restriction relaxation options for some placement constraints. When a default restriction is relaxed by a user, the Quartus II fitter generates warnings.

f For more information about how Quartus II software checks I/O restrictions, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

12. Embedded Multipliers in Cyclone II Devices

CII51012-1.2

Introduction

Use Cyclone® II FPGAs alone or as digital signal processing (DSP) co-processors to improve price-to-performance ratios for DSP applications. You can implement high-performance yet low-cost DSP systems with the following Cyclone II device features and design support:

- Up to 150 18 x 18 multipliers
- Up to 1.1 Mbit of on-chip embedded memory
- High-speed interface to external memory
- DSP Intellectual Property (IP) cores
- DSP Builder interface to the Mathworks Simulink and Matlab design environment
- DSP Development Kit, Cyclone II Edition

This chapter focuses on the Cyclone II embedded multiplier blocks.

Cyclone II devices have embedded multiplier blocks optimized for multiplier-intensive low-cost DSP applications. These embedded multipliers combined with the flexibility of programmable logic devices (PLDs), provide you with the ability to efficiently implement various cost sensitive DSP functions easily. Consumer-based application systems such as digital television (DTV) and home entertainment systems typically require a cost effective solution for implementing multipliers to perform signal processing functions like finite impulse response (FIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

Along with the embedded multipliers, the M4K memory blocks in Cyclone II devices also support various soft multiplier implementations. These, in combination with the embedded multipliers increase the available number of multipliers in Cyclone II devices and provide the user with a wide variety of implementation options and flexibility when designing their systems.

f See the Cyclone II Device Family Data Sheet section in Volume 1 of the ***Cyclone II Device Handbook*** for more information on Cyclone II devices.

If the configuration bitstream size exceeds the capacity of a serial configuration device, you must select a larger configuration device and/or enable the compression feature. When configuring multiple devices, the size of the bitstream is the sum of the individual devices' configuration bitstreams.

Configuring Multiple Cyclone II Devices with the Same Design

Certain designs require you to configure multiple Cyclone II devices with the same design through a configuration bitstream or SOF. You can do this through one of two methods, as described in this section. For both methods, the serial configuration devices cannot be cascaded or chained together.

Multiple SOFs

In the first method, two copies of the SOF file are stored in the serial configuration device. Use the first copy to configure the master Cyclone II device and the second copy to configure all remaining slave devices concurrently. In this setup, the master Cyclone II device is in AS mode, and the slave Cyclone II devices are in PS mode (MSEL=01). See Figure 13–5.

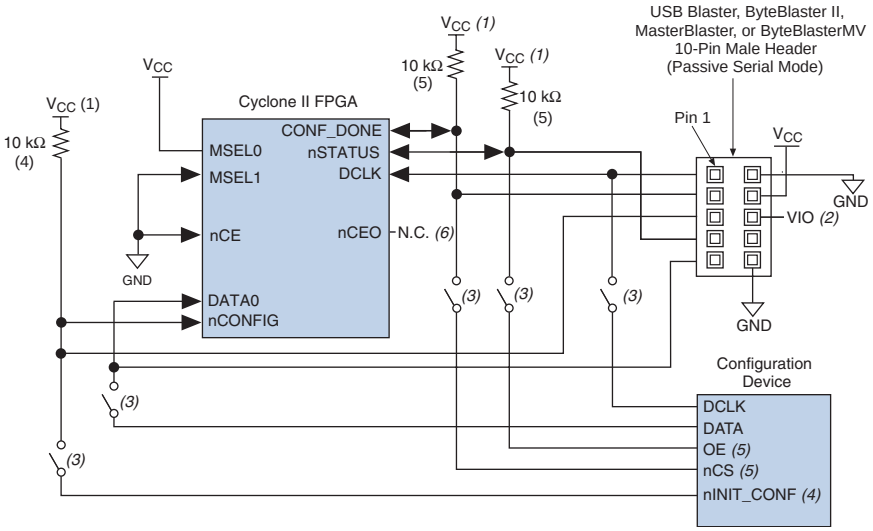
To configure four identical Cyclone II devices with the same SOF file, connect the three slave devices for concurrent configuration as shown in Figure 13–5. The nCEO pin from the master device drives the nCE input pins on all three slave devices. Connect the configuration device's DATA and DCLK pins to the Cyclone II device's DATA and DCLK pins in parallel. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding nCEO high. After completing its configuration cycle, the master drives nCE low and transmits the second copy of the configuration data to all three slave devices, configuring them simultaneously.

The advantage of using the setup in Figure 13–5 is that you can have a different SOF file for the Cyclone II master device. However, all the Cyclone II slave devices must be configured with the same SOF file. The SOF files in this configuration method can be either compressed or uncompressed.

1 You can still use this method if the master and slave Cyclone II devices use the same SOF.

the five common signals (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) between the cable and the configuration device. You can also remove the configuration device from the board when configuring the FPGA with the cable. Figure 13–21 shows a combination of a configuration device and a download cable to configure an FPGA.

Figure 13–21. PS Configuration with a Download Cable & Configuration Device Circuit



Notes to Figure 13–21:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(3) You should not attempt configuration with a download cable while a configuration device is connected to a Cyclone II device. Instead, you should either remove the configuration device from its socket when using the download cable or place a switch on the five common signals between the download cable and the configuration device.

(4) The nINIT_CONF pin (available on enhanced configuration devices and EPC2 devices only) has an internal pull-up resistor that is always active. This means an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used or not available (e.g., on EPC1 devices), nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(5) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(6) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

Document Revision History

Table 15–21 shows the revision history for this document.

Table 15–21. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.3	Added document revision history.	
November 2005 v2.1	Updated information throughout.	
July 2005 v2.0	Updated packaging information.	
November 2004 v1.0	Added document to the Cyclone II Device Handbook.	