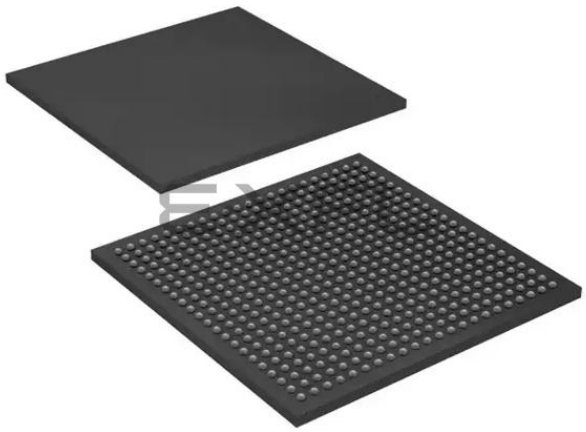

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	294
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f484i8n

- 133-MHz PCI-X 1.0 specification compatibility
- High-speed external memory support, including DDR, DDR2, and SDR SDRAM, and QDRII SRAM supported by drop in Altera IP MegaCore functions for ease of use
- Three dedicated registers per I/O element (IOE): one input register, one output register, and one output-enable register
- Programmable bus-hold feature
- Programmable output drive strength feature
- Programmable delays from the pin to the IOE or logic array
- I/O bank grouping for unique VCCIO and/or VREF bank settings
- MultiVolt™ I/O standard support for 1.5-, 1.8-, 2.5-, and 3.3-interfaces
- Hot-socketing operation support
- Tri-state with weak pull-up on I/O pins before and during configuration
- Programmable open-drain outputs
- Series on-chip termination support

- Flexible clock management circuitry
  - Hierarchical clock network for up to 402.5-MHz performance
  - Up to four PLLs per device provide clock multiplication and division, phase shifting, programmable duty cycle, and external clock outputs, allowing system-level clock management and skew control
  - Up to 16 global clock lines in the global clock network that drive throughout the entire device

- Device configuration
  - Fast serial configuration allows configuration times less than 100 ms
  - Decompression feature allows for smaller programming file storage and faster configuration times
  - Supports multiple configuration modes: active serial, passive serial, and JTAG-based configuration
  - Supports configuration through low-cost serial configuration devices
  - Device configuration supports multiple voltages (either 3.3, 2.5, or 1.8 V)

- Intellectual property
  - Altera megafunction and Altera MegaCore function support, and Altera Megafunctions Partners Program (AMPP^{SM}) megafunction support, for a wide range of embedded processors, on-chip and off-chip interfaces, peripheral functions, DSP functions, and communications functions and

Table 2–1. Cyclone II Device Routing Scheme (Part 2 of 2)

Source	Destination												
	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	LE	M4K RAM Block	Embedded Multiplier	PLL	Column IOE	Row IOE
LE	✓	✓	✓	✓		✓							
M4K memory Block		✓	✓	✓		✓							
Embedded Multipliers		✓	✓	✓		✓							
PLL			✓	✓		✓							
Column IOE						✓	✓						
Row IOE			✓	✓	✓	✓							

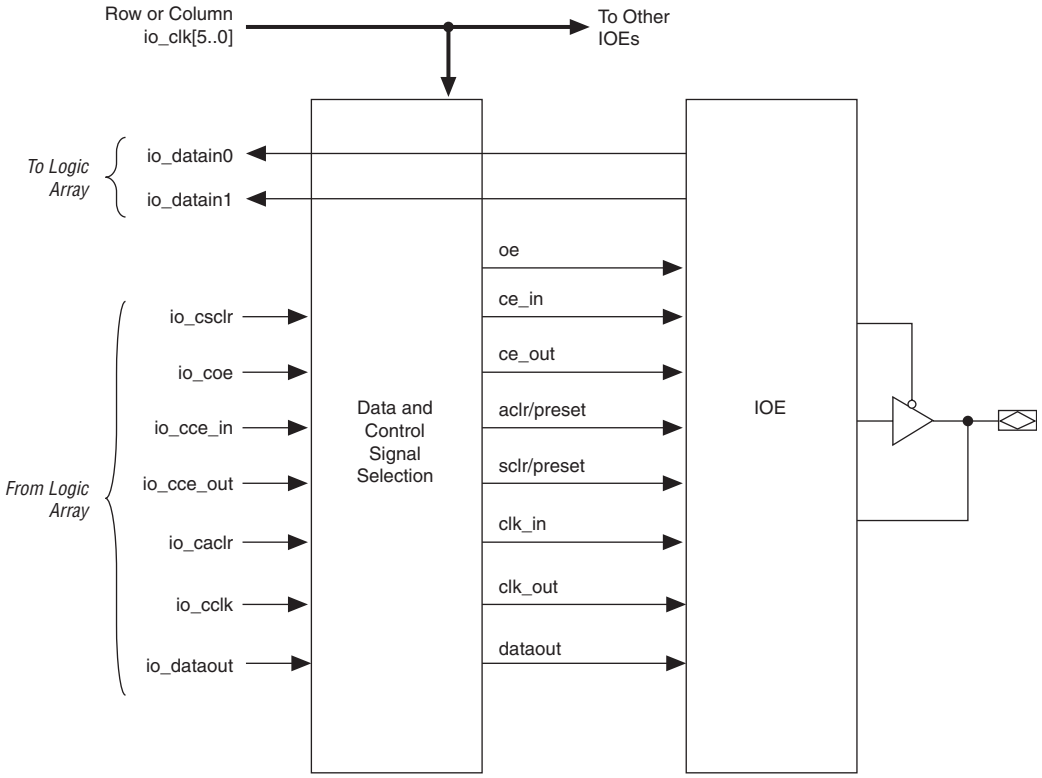
Global Clock Network & Phase-Locked Loops

Cyclone II devices provide global clock networks and up to four PLLs for a complete clock management solution. Cyclone II clock network features include:

- Up to 16 global clock networks
- Up to four PLLs
- Global clock network dynamic clock source selection
- Global clock network dynamic enable and disable

The pin's datain signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks, io_clk[5..0], provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions (see "Global Clock Network & Phase-Locked Loops" on page 2–16). Figure 2–23 illustrates the signal paths through the I/O block.

Figure 2–23. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: oe, ce_in, ce_out, aclr/preset, sclr/preset, clk_in, and clk_out. Figure 2–24 illustrates the control signal selection.

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL_18_CLASS_II	0	pF
1.5V_HSTL_CLASS_I	0	pF
1.5V_HSTL_CLASS_II	0	pF
1.8V_HSTL_CLASS_I	0	pF
1.8V_HSTL_CLASS_II	0	pF
DIFFERENTIAL_SSTL_2_CLASS_I	0	pF
DIFFERENTIAL_SSTL_2_CLASS_II	0	pF
DIFFERENTIAL_SSTL_18_CLASS_I	0	pF
DIFFERENTIAL_SSTL_18_CLASS_II	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
LVDS	0	pF
1.2V_HSTL	0	pF
1.2V_DIFFERENTIAL_HSTL	0	pF

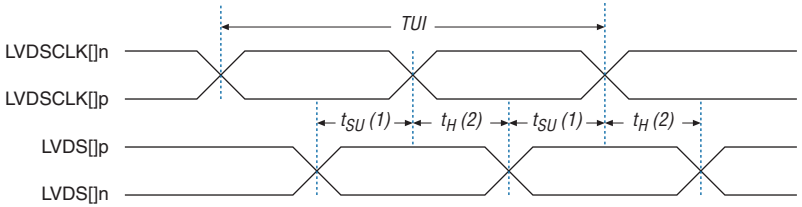
Table 5–49. Mini-LVDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Device operation in Mbps	×10	100	—	311	100	—	311	100	—	311	Mbps
	×8	80	—	311	80	—	311	80	—	311	Mbps
	×7	70	—	311	70	—	311	70	—	311	Mbps
	×4	40	—	311	40	—	311	40	—	311	Mbps
	×2	20	—	311	20	—	311	20	—	311	Mbps
	×1	10	—	311	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%	—	—	500	—	—	500	—	—	500	ps
t_{FALL}	80–20%	—	—	500	—	—	500	—	—	500	ps
t_{LOCK}		—	—	100	—	—	100	—	—	100	µs

In order to determine the transmitter timing requirements, mini-LVDS receiver timing requirements on the other end of the link must be taken into consideration. The mini-LVDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for mini-LVDS are shown in Figure 5–6.

Figure 5–6. mini-LVDS Transmitter AC Timing Specification



Notes to Figure 5–6:
(1) The data setup time, t_{SU}, is 0.225 × TUI.
(2) The data hold time, t_H, is 0.225 × TUI.

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins *Notes (1), (2)* *(Part 2 of 2)*

Row I/O Output Standard	C6	C7	C8	Unit
Differential SSTL-2 Class I	60	90	90	ps
Differential SSTL-2 Class II	65	75	75	ps
Differential SSTL-18 Class I	90	165	165	ps
Differential HSTL-18 Class I	85	155	155	ps
Differential HSTL-15 Class I	145	145	205	ps
LVDS	60	60	60	ps
Simple RSDS	60	60	60	ps
Mini LVDS	60	60	60	ps
PCI	195	255	255	ps
PCI-X	195	255	255	ps

Notes to Table 5–55:
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Here is an example for calculating the DCD as a percentage for an SDR output on a row I/O on a –6 device:

If the SDR output I/O standard is SSTL-2 Class II, the maximum DCD is 65 ps (refer to Table 5–55). If the clock frequency is 167 MHz, the clock period T is:

$$T = 1/f = 1 / 167\ \text{MHz} = 6\ \text{ns} = 6000\ \text{ps}$$

To calculate the DCD as a percentage:

$(T/2 - DCD) / T = (6000\ \text{ps}/2 - 65\ \text{ps}) / 6000\ \text{ps} = 48.91\%$ (for low boundary)

$(T/2 + DCD) / T = (6000\ \text{ps}/2 + 65\ \text{ps}) / 6000\text{ps} = 51.08\%$ (for high boundary

Table 5–56. Maximum DCD for SDR Output on Column I/O *Notes (1), (2)* *(Part 1 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
LVCMOS	195	285	285	ps
LVTTL	210	305	305	ps

Table 5–56. Maximum DCD for SDR Output on Column I/O Notes (1), (2) *(Part 2 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
2.5-V	140	140	155	ps
1.8-V	115	115	165	ps
1.5-V	745	745	770	ps
SSTL-2 Class I	60	60	75	ps
SSTL-2 Class II	60	60	80	ps
SSTL-18 Class I	60	130	130	ps
SSTL-18 Class II	60	135	135	ps
HSTL-18 Class I	60	115	115	ps
HSTL-18 Class II	75	75	100	ps
HSTL-15 Class I	150	150	150	ps
HSTL-15 Class II	135	135	155	ps
Differential SSTL-2 Class I	60	60	75	ps
Differential SSTL-2 Class II	60	60	80	ps
Differential SSTL-18 Class I	60	130	130	ps
Differential SSTL-18 Class II	60	135	135	ps
Differential HSTL-18 Class I	60	115	115	ps
Differential HSTL-18 Class II	75	75	100	ps
Differential HSTL-15 Class I	150	150	150	ps
Differential HSTL-15 Class II	135	135	155	ps
LVDS	60	60	60	ps
Simple RSDS	60	70	70	ps
Mini-LVDS	60	60	60	ps

Notes to Table 5–56:

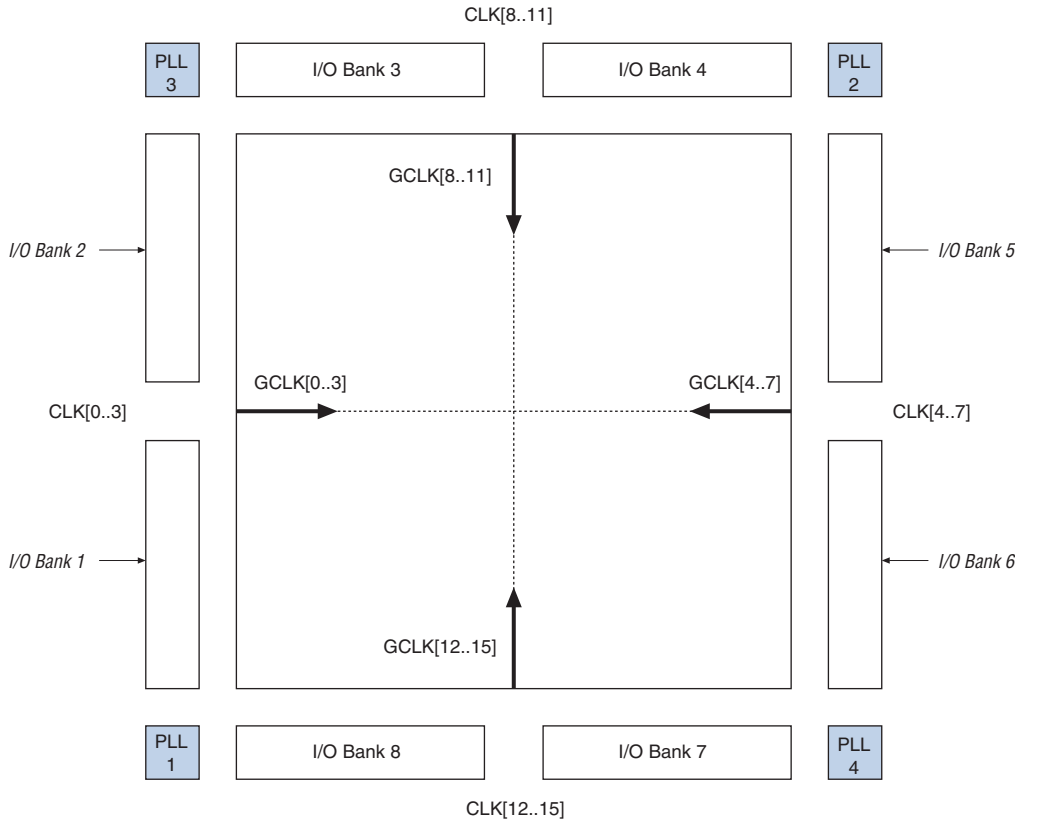
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

Table 5–57. Maximum for DDIO Output on Row Pins with PLL in the Clock Path Notes (1), (2) *(Part 1 of 2)*

Row Pins with PLL in the Clock Path	C6	C7	C8	Unit
LVCMOS	270	310	310	ps
LVTTL	285	305	335	ps
2.5-V	180	180	220	ps
1.8-V	165	175	205	ps

Figure 7–1. Cyclone II Device PLL Locations *Note (1)*



Note to Figure 7–1:

(1) This figure shows the PLL and clock inputs in the EP2C15 through EP2C70 devices. The EP2C5 and EP2C8 devices only have eight global clocks (`CLK[0..3]` and `CLK[4..7]`) and PLLs 1 and 2.

The main purpose of a PLL is to synchronize the phase and frequency of the VCO to an input reference clock. There are a number of components that comprise a PLL to achieve this phase alignment.

The PLL compares the rising edge of the reference input clock to a feedback clock using a phase-frequency detector (PFD). The PFD produces an up or down signal that determines whether the VCO needs to operate at a higher or lower frequency. The PFD output is applied to the charge pump and loop filter, which produces a control voltage for setting the frequency of the VCO. If the PFD transitions the up signal high, then the VCO frequency increases. If the PFD transitions the down signal high, then the VCO frequency decreases.

Independent Clock Mode

Cyclone II memory blocks can implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables for port A and B registers. However, ports do not support asynchronous clear signals for the registers.

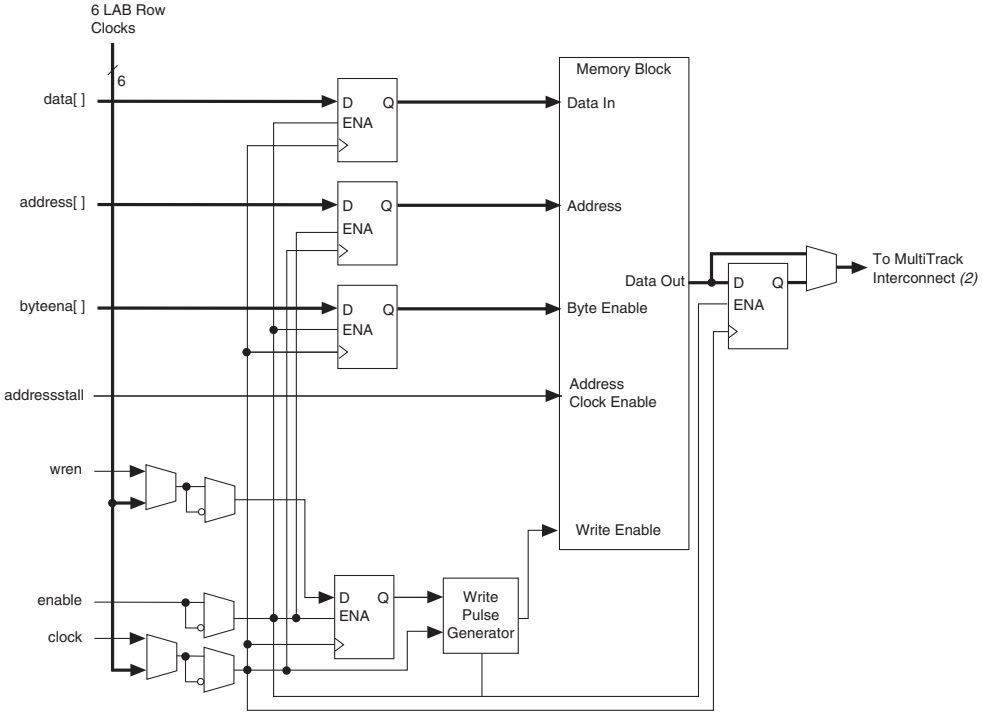
Figure 8–13 shows a memory block in independent clock mode.

Input/Output Clock Mode

Cyclone II memory blocks can implement the input/output clock mode for true and simple dual-port memory. On each of the two ports, A and B, one clock controls all registers for the data, write enable, and address inputs into the memory block. The other clock controls the blocks' data output registers. Each memory block port also supports independent clock enables for input and output registers. Asynchronous clear signals for the registers are not supported.

Figures 8–14 through 8–16 show the memory block in input/output clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

Figure 8–20. Cyclone II Single-Clock Mode in Single-Port Mode *Notes (1), (2)*



Notes to Figure 8–20:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in Volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

Power-Up Conditions & Memory Initialization

The Cyclone II memory block outputs always power-up to zero, regardless of whether the output registers are used or bypassed. Even if an MIF pre-loads the contents of the memory block, the outputs still power up cleared. For example, if address 0 is pre-initialized to `FF`, M4K blocks power up with the output at `00`. A subsequent read after power up from address 0 outputs the pre-initialized value of `FF`.

Document Revision History

Table 8–8 shows the revision history for this document.

Table 8–8. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v2.4	Corrected Figure 8–12.	—
February 2007 v2.3	• Added document revision history. • Updated "Packed Mode Support" section. • Updated "Mixed-Port Read-During-Write Mode" section and added new Figure 8–24.	• In packed mode support, the maximum data width for each of the two memory block is 18 bits wide. • Added don't care mode information to mixed-port read-during-write mode section.
November 2005 v2.1	Updated Figures 8–13 through 8–20.	—
July 2005 v2.0	Added Clear Signals section.	—
February 2005 v1.1	Added a note to Figures 8-13 through 8-20 regarding violating the setup and hold time on address registers.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Table 10–3. Cyclone II 33-MHz PCI Support (Part 2 of 2)

Device	Package	–6, –7 and –8 Speed Grades	
		64 Bits	32 Bits
EP2C20	240-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
	484-pin FineLine BGA	✓	✓
EP2C35	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C50	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C70	672-pin FineLine BGA	✓	✓
	896-pin FineLine BGA	✓	✓

3.3-V PCI-X

The 3.3-V PCI-X I/O standard is formulated under PCI-X Local Bus Specification Revision 1.0 developed by the PCI SIG.

The PCI-X 1.0 standard is used for applications that interface to the PCI local bus. The standard enables the design of systems and devices that operate at clock speeds up to 133 MHz, or 1 gigabit per second (Gbps) for a 64-bit bus. The PCI-X 1.0 protocol enhancements enable devices to operate much more efficiently, providing more usable bandwidth at any clock frequency. By using the PCI-X 1.0 standard, devices can be designed to meet PCI-X 1.0 requirements and operate as conventional 33- and 66-MHz PCI devices when installed in those systems. This standard requires 3.3-V V_{CCIO}. Cyclone II devices are fully compliant with the 3.3-V PCI-X Specification Revision 1.0a and meet the 133 MHz operating frequency and timing requirements. The 3.3-V PCI-X standard does not require input reference voltages or board terminations. Cyclone II devices support both input and output levels operation for left and right I/O banks.

Easy-to-Use, Low-Cost PCI Express Solution

PCI Express is rapidly establishing itself as the successor to PCI, providing higher performance, increased flexibility, and scalability for next-generation systems without increasing costs, all while maintaining software compatibility with existing PCI applications. Now you can easily design high volume, low-cost PCI Express ×1 solutions today featuring:

I/O Termination

The majority of the Cyclone II I/O standards are single-ended, non-voltage-referenced I/O standards and, as such, the following I/O standards do not specify a recommended termination scheme:

- 3.3-V LVTTL and LVCMOS
- 2.5-V LVTTL and LVCMOS
- 1.8-V LVTTL and LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI and PCI-X

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

For more information on termination for voltage-referenced I/O standards, refer to "Supported I/O Standards" on page 10–1.

Differential I/O Standard Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus.

Cyclone II devices support differential I/O standards LVDS, RSDS, and mini-LVDS, and differential LVPECL.

For more information on termination for differential I/O standards, refer to "Supported I/O Standards" on page 10–1.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pads in relation to differential pads in the same I/O bank. Use the following guidelines for placing single-ended pads with respect to differential pads and for differential output pads placement in Cyclone II devices.

For the LVDS I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVDS I/O pad.
- Single-ended outputs can be no closer than five pads away from an LVDS I/O pad.
- Maximum of four 155-MHz (or greater) LVDS output channels per VCCIO and ground pair.
- Maximum of three 311-MHz (or greater) LVDS output channels per VCCIO and ground pair.

For optimal signal integrity at the LVDS input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVDS input pad.

The Quartus II software only checks the first two cases.

For the RSDS and mini-LVDS I/O standards:

- Single-ended inputs can be no closer than four pads away from an RSDS and mini-LVDS output pad.
- Single-ended outputs can be no closer than five pads away from an RSDS and mini-LVDS output pad.
- Maximum of three 85-MHz (or greater) RSDS and mini-LVDS output channels per VCCIO and ground pair.

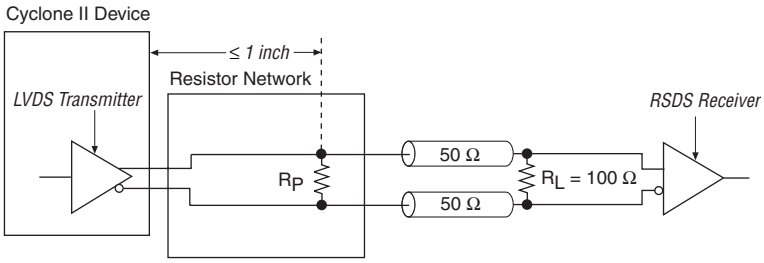
The Quartus II software only checks the first two cases.

For the LVPECL I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVPECL input pad.
- Single-ended outputs can be no closer than five pads away from an LVPECL input pad.

For optimal signal integrity at the LVPECL input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVPECL input pad.

Figure 11–8. RSDS Single Resistor Network *Note (1)*



Note to Figure 11–8:
(1) R_p = 100 Ω

RSDS Software Support

When designing for the RSDS I/O standard, assign the RSDS I/O standard to the I/O pins intended for RSDS in the Quartus® II software. Contact Altera Applications for reference designs.

mini-LVDS Standard Support in Cyclone II Devices

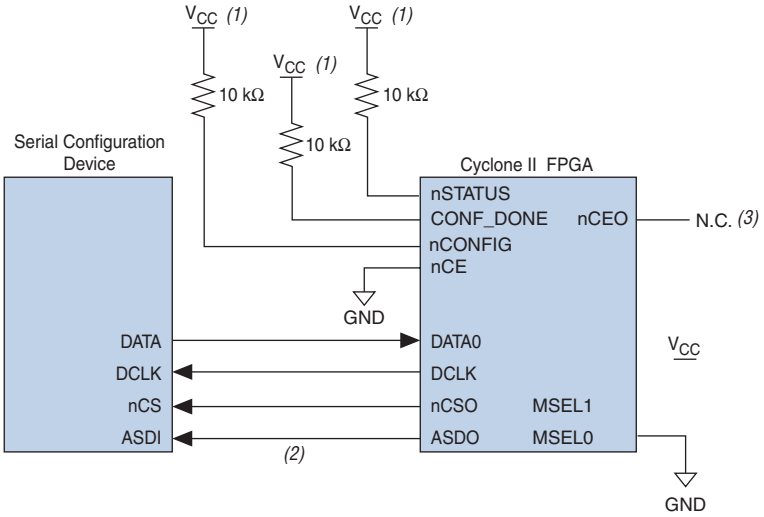
The mini-LVDS specification defines its use in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the Texas Instruments mini-LVDS Interface Specification and support the mini-LVDS output standard. Table 11–3 shows the mini-LVDS electrical characteristics for Cyclone II devices.

Table 11–3. mini-LVDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	300		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1125	1250	1375	mV
T_r / T_f	Transition time	20% to 80%			500	ps

Notes to Table 11–3:
(1) The V_{OD} specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

Figure 13–3. Single Device AS Configuration



Notes to Figure 13–3:

(1) Connect the pull-up resistors to a 3.3-V supply.

(2) Cyclone II devices use the ASDO to ASDI path to control the configuration device.

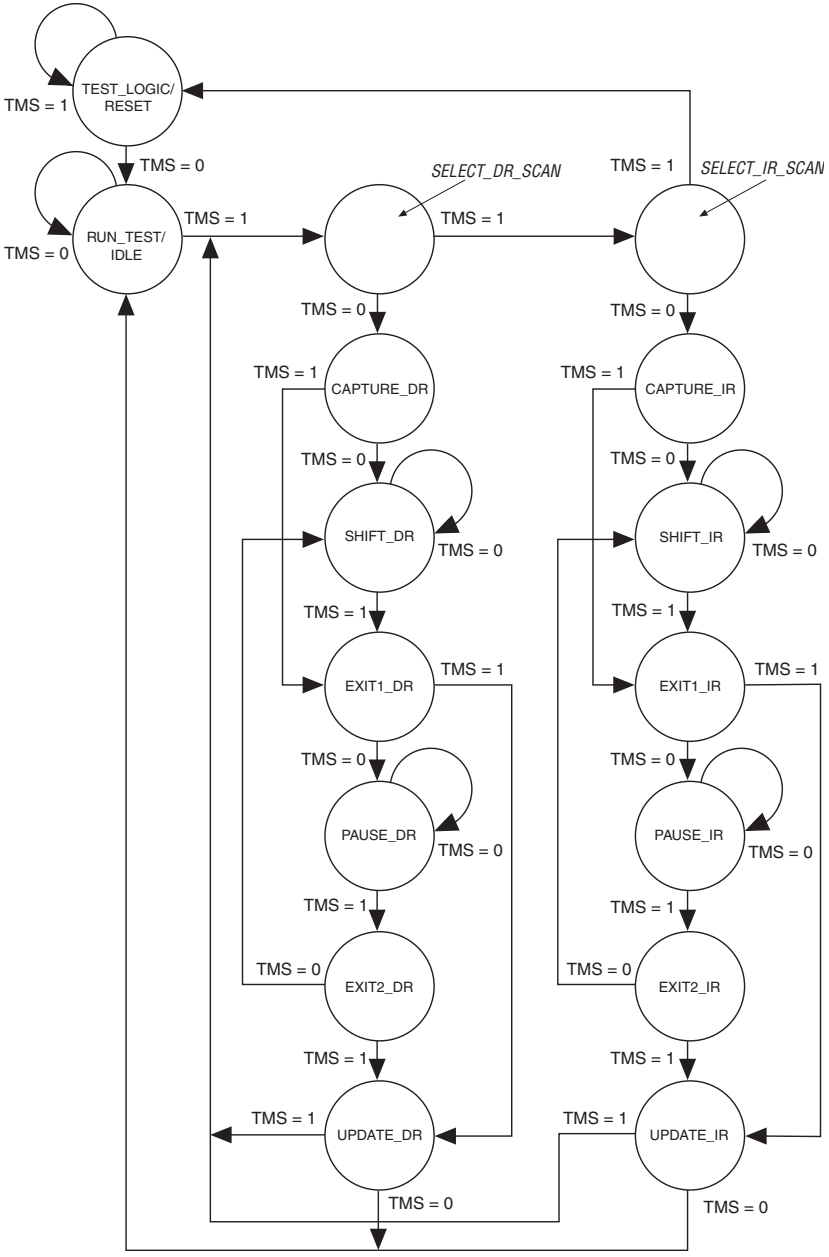
(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

Upon power-up, the Cyclone II device goes through a POR. During POR, the device resets, holds nSTATUS and CONF_DONE low, and tri-states all user I/O pins. After POR, which typically lasts 100 ms, the Cyclone II device releases nSTATUS and enters configuration mode when the external 10-kΩ resistor pulls the nSTATUS pin high. Once the FPGA successfully exits POR, all user I/O pins continue to be tri-stated. Cyclone II devices have weak pull-up resistors on the user I/O pins which are on before and during configuration.

The value of the weak pull-up resistors on the I/O pins that are on before and during configuration are available in the *DC Characteristics & Timing Specifications* chapter of the *Cyclone II Device Handbook*.

The configuration cycle consists of the reset, configuration, and initialization stages.

Figure 14–5. IEEE Std. 1149.1 TAP Controller State Machine



When designing a board for JTAG configuration of Cyclone II devices, the connections for the dedicated configuration pins need to be considered.

For more information on using the IEEE Std.1149.1 circuitry for device configuration, see the *Configuring Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

BST for Configured Devices

For a configured device, the input buffers are turned off by default for I/O pins that are set as output only in the design file. Nevertheless, executing the SAMPLE instruction will turn on the input buffers for the output pins. You can set the Quartus II software to always enable the input buffers on a configured device so it behaves the same as an unconfigured device for boundary-scan testing, allowing sample function on output pins in the design. This aspect can cause slight increase in standby current because the unused input buffer is always on. In the Quartus II software, do the following:

1. Choose **Settings** (Assignment menu).
2. Click **Assembler**.
3. Turn on **Always Enable Input Buffers**.
4. If you use the default setting with input disabled, you need to convert the default BSDL file to the design-specific BSDL file using the BSDLCustomizer script. For more information regarding BSDL file, refer to "Boundary-Scan Description Language (BSDL) Support".

Disabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Cyclone II devices is enabled upon device power-up. Because this circuitry may be used for BST or in-circuit reconfiguration, this circuitry must be enabled only at specific times as mentioned in "Using IEEE Std. 1149.1 BST Circuitry" on page 14–16.

If the IEEE Std. 1149.1 circuitry will not be utilized at any time, the circuitry should be permanently disabled. Table 14–3 shows the pin connections necessary for disabling the IEEE Std. 1149.1 circuitry in Cyclone II devices to ensure that the circuitry is not inadvertently enabled when it is not needed.

Table 14–3. Disabling IEEE Std. 1149.1 Circuitry

JTAG Pins *(1)*	Connection for Disabling
TMS	V_{CC}
TCK	GND
TDI	V_{CC}
TDO	Leave open

Note to Table 14–3:
(1) There is no software option to disable JTAG in Cyclone II devices. The JTAG pins are dedicated.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If the 10-bit checkerboard pattern "1010101010" does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the TAP controller has not reached the proper state. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and send the code 01100 to the TMS pin.
  - Check the connections to the V_{CC}, GND, JTAG, and dedicated configuration pins on the device.