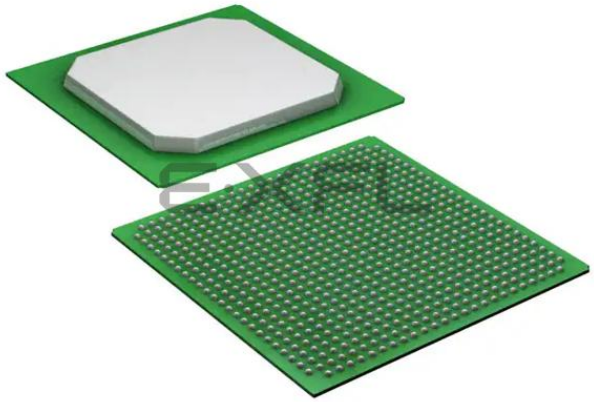

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f672c6

There are five dynamic control input signals that feed the embedded multiplier: `signa`, `signb`, `clk`, `clkena`, and `aclr`. `signa` and `signb` can be registered to match the data signal input path. The same `clk`, `clkena`, and `aclr` signals feed all registers within a single embedded multiplier.

For more information on Cyclone II embedded multipliers, see the *Embedded Multipliers in Cyclone II Devices* chapter.

I/O Structure & Features

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- V_{REF} pins

Cyclone II device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–20 shows the Cyclone II IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. You can use IOEs as input, output, or bidirectional pins.

Table 2–16. Programmable Drive Strength (Part 2 of 2) Note (1)		
I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top & Bottom I/O Pins	Side I/O Pins
LVCMOS (1.5 V)	2	2
	4	4
	6	6
	8	
SSTL-2 class I	8	8
	12	12
SSTL-2 class II	16	16
	20	
	24	
SSTL-18 class I	6	6
	8	8
	10	10
	12	
SSTL-18 class II	16	
	18	
HSTL-18 class I	8	8
	10	10
	12	12
HSTL-18 class II	16	
	18	
	20	
HSTL-15 class I	8	8
	10	
	12	
HSTL-15 class II	16	

Note to Table 2–16:
(1) The default current in the Quartus II software is the maximum setting for each I/O standard.

Open-Drain Output

Cyclone II devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (that is, interrupt and write-enable signals) that can be asserted by any of several devices.

SRAM configuration elements allow Cyclone II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with the nCONFIG pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files within the system or remotely.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

The configuration pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The voltage level of the configuration output pins is determined by the V_{CCIO} of the bank where the pins reside. The bank V_{CCIO} selects whether the configuration inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Configuration Schemes

You can load the configuration data for a Cyclone II device with one of three configuration schemes (see Table 3–4), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Cyclone II device. A low-cost configuration device can automatically configure a Cyclone II device at system power-up.

Multiple Cyclone II devices can be configured in any of the three configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 3–4. Data Sources for Configuration

Configuration Scheme	Data Source
Active serial (AS)	Low-cost serial configuration device
Passive serial (PS)	Enhanced or EPC2 configuration device, MasterBlaster, ByteBlasterMV, ByteBlaster II or USB Blaster download cable, or serial data source
JTAG	MasterBlaster, ByteBlasterMV, ByteBlaster II or USB Blaster download cable or a microprocessor with a Jam or JBC file

For more information on configuration, see the *Configuring Cyclone II Devices* chapter of the *Cyclone II Handbook, Volume 2*.

Table 5–30. EP2C35 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.410	1.476	2.514	2.724	2.986	ns
t_{COUT}	1.412	1.478	2.530	2.737	2.994	ns
t_{PLLCIN}	–0.117	–0.127	0.134	0.162	0.241	ns
$t_{PLLCOUT}$	–0.115	–0.125	0.15	0.175	0.249	ns

EP2C50 Clock Timing Parameters

Tables 5–31 and 5–32 show the clock timing parameters for EP2C50 devices.

Table 5–31. EP2C50 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.759	2.940	3.174	ns
t_{COUT}	1.589	1.666	2.793	2.972	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.113	0.075	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.147	0.107	0.118	ns

Table 5–32. EP2C50 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.624	2.791	3.010	ns
t_{COUT}	1.465	1.535	2.640	2.804	3.018	ns
t_{PLLCIN}	–0.261	–0.276	–0.022	–0.074	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	–0.006	–0.061	–0.067	ns

Table 5–37. Cyclone II IOE Programmable Delay on Row Pins Notes (1), (2) (Part 2 of 2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Input Register	Pad -> I/O input register	8	0	2669	0	4482	0	4834	0	4859	ps
			0	2802	—	—	0	4671	—	—	ps
Delay from Output Register to Output Pin	I/O output register -> Pad	2	0	308	0	572	0	648	0	682	ps
			0	324	—	—	0	626	—	—	ps

Notes to Table 5–37 :

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.

(3) The value in the first row represents the fast corner timing parameter for industrial and automotive devices. The second row represents the fast corner timing parameter for commercial devices.

(4) The value in the first row is for automotive devices. The second row is for commercial devices.

Default Capacitive Loading of Different I/O Standards

Refer to Table 5–38 for default capacitive loading of different I/O standards.

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 1 of 2)

I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5V	0	pF
1.8V	0	pF
1.5V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL_2_CLASS_I	0	pF
SSTL_2_CLASS_II	0	pF
SSTL_18_CLASS_I	0	pF

Table 5–48. RSDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max *(1)*	Min	Typ	Max *(1)*	Min	Typ	Max *(1)*	
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	80–20%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	—	—		100	—		100	—	—	100	µs

Note to Table 5–48:

(1) These specifications are for a three-resistor RSDS implementation. For single-resistor RSDS in ×10 through ×2 modes, the maximum data rate is 170 Mbps and the corresponding maximum input clock frequency is 85 MHz. For single-resistor RSDS in ×1 mode, the maximum data rate is 170 Mbps, and the maximum input clock frequency is 170 MHz. For more information about the different RSDS implementations, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the Cyclone II Device Handbook.

In order to determine the transmitter timing requirements, RSDS receiver timing requirements on the other end of the link must be taken into consideration. RSDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for RSDS are shown in Figure 5–5.

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins *Notes (1), (2)* *(Part 2 of 2)*

Row I/O Output Standard	C6	C7	C8	Unit
Differential SSTL-2 Class I	60	90	90	ps
Differential SSTL-2 Class II	65	75	75	ps
Differential SSTL-18 Class I	90	165	165	ps
Differential HSTL-18 Class I	85	155	155	ps
Differential HSTL-15 Class I	145	145	205	ps
LVDS	60	60	60	ps
Simple RSDS	60	60	60	ps
Mini LVDS	60	60	60	ps
PCI	195	255	255	ps
PCI-X	195	255	255	ps

Notes to Table 5–55:
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Here is an example for calculating the DCD as a percentage for an SDR output on a row I/O on a –6 device:

If the SDR output I/O standard is SSTL-2 Class II, the maximum DCD is 65 ps (refer to Table 5–55). If the clock frequency is 167 MHz, the clock period T is:

$$T = 1/f = 1 / 167\ \text{MHz} = 6\ \text{ns} = 6000\ \text{ps}$$

To calculate the DCD as a percentage:

$(T/2 - DCD) / T = (6000\ \text{ps}/2 - 65\ \text{ps}) / 6000\ \text{ps} = 48.91\%$ (for low boundary)

$(T/2 + DCD) / T = (6000\ \text{ps}/2 + 65\ \text{ps}) / 6000\text{ps} = 51.08\%$ (for high boundary

Table 5–56. Maximum DCD for SDR Output on Column I/O *Notes (1), (2)* *(Part 1 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
LVCMOS	195	285	285	ps
LVTTL	210	305	305	ps

Section II. Clock Management

This section provides information on the phase-locked loops (PLLs). Cyclone® II PLLs offer general-purpose clock management with multiplication and phase shifting and also have the ability to drive off chip to control system-level clock networks. This section contains detailed information on the features, the interconnections to the logic array and off chip, and the specifications for Cyclone II PLLs.

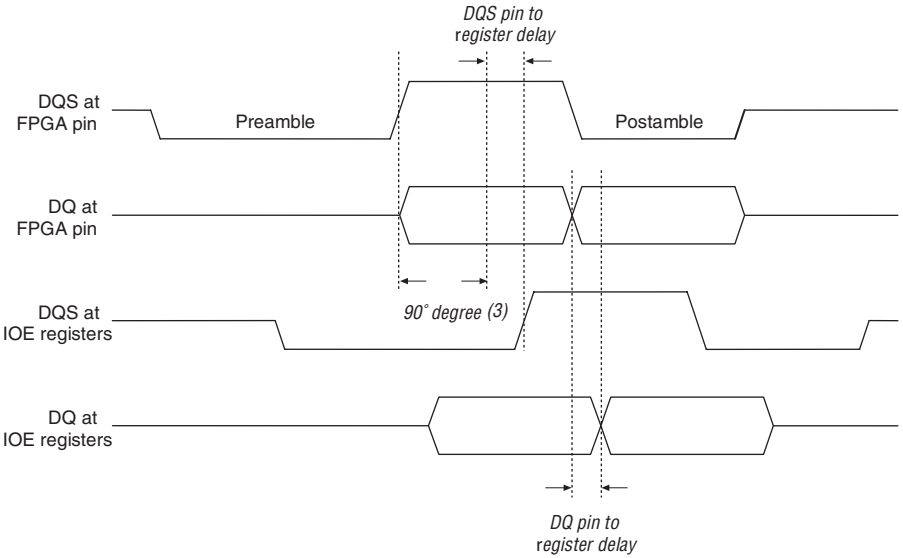
This section includes the following chapter:

- Chapter 7, PLLs in Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 9–1. Example of a 90° Shift on the DQS Signal *Notes (1), (2)*



Notes to Figure 9–1:
(1) RLDRAM II and QDRII SRAM memory interfaces do not have preamble and postamble specifications.
(2) DDR2 SDRAM does not support a burst length of two.
(3) The phase shift required for your system should be based on your timing analysis and may not be 90°.

During write operations to a DDR or DDR2 SDRAM device, the FPGA must send the data strobe to the memory device center-aligned relative to the data. Cyclone II devices use a PLL to center-align the data strobe by generating a 0° phase-shifted system clock for the write data strobes and a –90° phase-shifted write clock for the write data pins for the DDR and DDR2 SDRAM. Figure 9–2 shows an example of the relationship between the data and data strobe during a burst-of-two write.

Figure 9–2. DQ & DQS Relationship During a DDR & DDR2 SDRAM Write

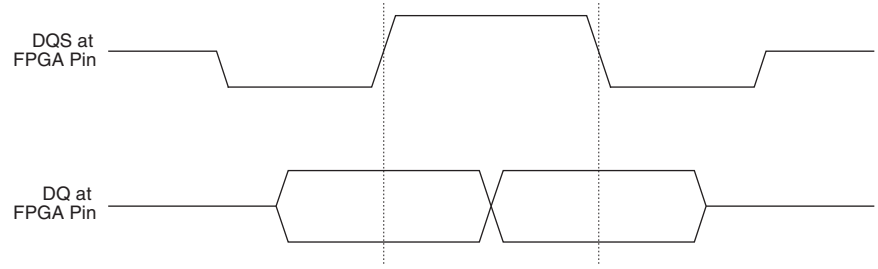


Table 10–3. Cyclone II 33-MHz PCI Support (Part 2 of 2)

Device	Package	–6, –7 and –8 Speed Grades	
		64 Bits	32 Bits
EP2C20	240-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
	484-pin FineLine BGA	✓	✓
EP2C35	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C50	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C70	672-pin FineLine BGA	✓	✓
	896-pin FineLine BGA	✓	✓

3.3-V PCI-X

The 3.3-V PCI-X I/O standard is formulated under PCI-X Local Bus Specification Revision 1.0 developed by the PCI SIG.

The PCI-X 1.0 standard is used for applications that interface to the PCI local bus. The standard enables the design of systems and devices that operate at clock speeds up to 133 MHz, or 1 gigabit per second (Gbps) for a 64-bit bus. The PCI-X 1.0 protocol enhancements enable devices to operate much more efficiently, providing more usable bandwidth at any clock frequency. By using the PCI-X 1.0 standard, devices can be designed to meet PCI-X 1.0 requirements and operate as conventional 33- and 66-MHz PCI devices when installed in those systems. This standard requires 3.3-V V_{CCIO}. Cyclone II devices are fully compliant with the 3.3-V PCI-X Specification Revision 1.0a and meet the 133 MHz operating frequency and timing requirements. The 3.3-V PCI-X standard does not require input reference voltages or board terminations. Cyclone II devices support both input and output levels operation for left and right I/O banks.

Easy-to-Use, Low-Cost PCI Express Solution

PCI Express is rapidly establishing itself as the successor to PCI, providing higher performance, increased flexibility, and scalability for next-generation systems without increasing costs, all while maintaining software compatibility with existing PCI applications. Now you can easily design high volume, low-cost PCI Express ×1 solutions today featuring:

1.8-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-7)

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts.

The 1.8-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.8-V LVCMOS.

SSTL-18 Class I and II

The 1.8-V SSTL-18 standard is formulated under JEDEC Standard, JESD815: Stub Series Terminated Logic for 1.8V (SSTL-18).

The SSTL-18 I/O standard is a 1.8-V memory bus standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V V_{REF} and a 0.9-V V_{TT}, with the termination resistors connected to both. There are no class definitions for the SSTL-18 standard in the JEDEC specification. The specification of this I/O standard is based on an environment that consists of both series and parallel terminating resistors. Altera provides solutions to two derived applications in JEDEC specification and names them class I and class II to be consistent with other SSTL standards. Figures 10–5 and 10–6 show SSTL-18 class I and II termination, respectively. Cyclone II devices support both input and output levels.

Figure 10–5. 1.8-V SSTL Class I Termination

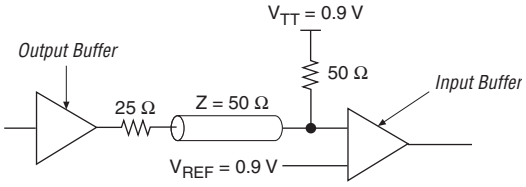
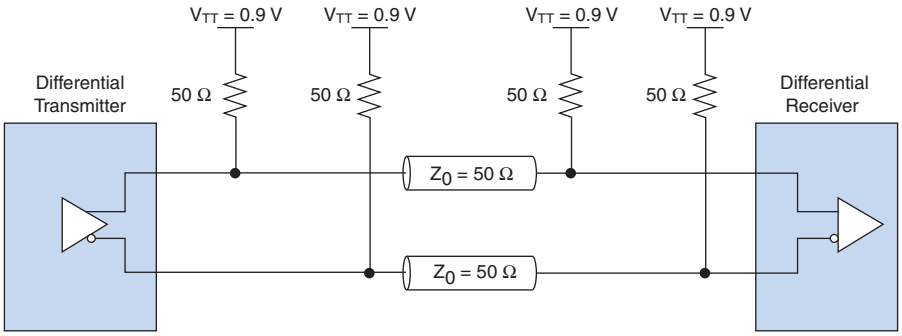


Figure 10–12. 1.8-V Differential HSTL Class II Termination



1.5-V LVCMOS (EIA/JEDEC Standard JESD8-11)

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices.

The 1.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.5-V LVCMOS.

1.5-V HSTL Class I and II

The 1.5-V HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic nominal switching range. This standard defines single-ended input and output specifications for all HSTL-compliant digital integrated circuits. The 1.5-V HSTL I/O standard in Cyclone II devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE, APEX 20KC, Stratix® II, Stratix GX, Stratix, and in Cyclone II devices themselves because the input and output voltage thresholds are compatible. Refer to Figures 10–13 and 10–14. Cyclone II devices support both input and output levels with V_{REF} and V_{TT}.

Table 10–5 shows I/O standards supported when a pin is used as a regular I/O pin in the I/O banks of Cyclone II devices.

- Maintain equal distance between traces in LVDS pairs, as much as possible. Routing the pair of traces close to each other maximizes the common-mode rejection ratio (CMRR).
- Longer traces have more inductance and capacitance. These traces should be as short as possible to limit signal integrity issues.
- Place termination resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° or 45° corners.
- Use high-performance connectors.
- Design backplane and card traces so that trace impedance matches the connector's and/or the termination's impedance.
- Keep equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths result in misplaced crossing points and decrease system margins as the channel-to-channel skew (TCCS) value increases.
- Limit vias because they cause discontinuities.
- Use the common bypass capacitor values such as 0.001, 0.01, and 0.1 µF to decouple the high-speed PLL power and ground planes.
- Keep switching transistor-to-transistor logic (TTL) signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Analyze system-level signals.

For PCB layout guidelines, see *AN 224: High-Speed Board Layout Guidelines*.

Conclusion

Cyclone II differential I/O capabilities enable you to keep pace with increasing design complexity. Support for I/O standards including LVDS, LVPECL, RSDS, mini-LVDS, differential SSTL and differential HSTL allows Cyclone II devices to fit into a wide variety of applications. Taking advantage of these I/O capabilities and Cyclone II pricing allows you to lower your design costs while remaining on the cutting edge of technology.

Software Support

Altera provides two methods for implementing multipliers in your design using embedded multiplier resources: instantiation and inference. Both methods use the following three Quartus II megafunctions:

- `lpm_mult`
- `altmult_add`
- `altmult_accum`

You can instantiate the megafunctions in the Quartus II software to use the embedded multipliers. You can use the `lpm_mult` and `altmult_add` megafunctions to implement multipliers. Additionally, you can use the `altmult_add` megafunctions to implement multiplier-adders where the embedded multiplier is used to implement the multiply function and the adder function is implemented in LEs. The `altmult_accum` megafunction implements multiply accumulate functions where the embedded multiplier implements the multiplier and the accumulator function is implemented in LEs.

See Quartus II On-Line Help for instructions on using the megafunctions and the MegaWizard Plug-In Manager.

For information on our complete DSP Design and Intellectual Property offerings, see **www.Altera.com**.

You can also infer the megafunctions by creating an HDL design and synthesize it using Quartus II integrated synthesis or a third-party synthesis tool that recognizes and infers the appropriate multiplier megafunction. Using either method, the Quartus II software maps the multiplier functionality to the embedded multipliers during compilation.

See the Synthesis section in Volume 1 of the ***Quartus II Handbook*** for more information.

Conclusion

The Cyclone II device embedded multipliers are optimized to support multiplier-intensive DSP applications such as FIR filters, FFT functions and encoders. These embedded multipliers can be configured to implement multipliers of various bit widths up to 18-bits to suit a particular application resulting in efficient resource utilization and improved performance and data throughput. The Quartus II software, together with the LeonardoSpectrum and Synplify software provide a complete and easy-to-use flow for implementing multiplier functions using embedded multipliers.

Table 13–1. Cyclone II Configuration Schemes		
Configuration Scheme	**MSEL1**	**MSEL0**
AS (20 MHz)	0	0
PS	0	1
Fast AS (40 MHz) *(1)*	1	0
JTAG-based Configuration *(2)*	*(3)*	*(3)*

Notes to Table 13–1:

(1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

(2) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

(3) Do not leave the MSEL pins floating; connect them to V_{CCIO} or ground. These pins support the non-JTAG configuration scheme used in production. If you are only using JTAG configuration, you should connect the MSEL pins to ground.

You can download configuration data to Cyclone II FPGAs with the AS, PS, or JTAG interfaces using the options in Table 13–2.

Table 13–2. Cyclone II Device Configuration Schemes	
Configuration Scheme	**Description**
AS configuration	Configuration using serial configuration devices (EPCS1, EPCS4, EPCS16 or EPCS64 devices)
PS configuration	Configuration using enhanced configuration devices (EPC4, EPC8, and EPC16 devices), EPC2 and EPC1 configuration devices, an intelligent host (microprocessor), or a download cable
JTAG-based configuration	Configuration via JTAG pins using a download cable, an intelligent host (microprocessor), or the Jam™ Standard Test and Programming Language (STAPL)

Configuration File Format

Table 13–3 shows the approximate uncompressed configuration file sizes for Cyclone II devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

Table 13–3. Cyclone II Raw Binary File (.rbf) Sizes *Note (1)*

Device	Data Size (Bits)	Data Size (Bytes)
EP2C5	1,265,792	152,998
EP2C8	1,983,536	247,974
EP2C15	3,892,496	486,562
EP2C20	3,892,496	486,562
EP2C35	6,858,656	857,332
EP2C50	9,963,392	1,245,424
EP2C70	14,319,216	1,789,902

Note to Table 13–3:
(1) These values are preliminary.

Use the data in Table 13–3 only to estimate the file size before design compilation. Different configuration file formats, such as a Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) format, have different file sizes. However, for any specific version of the Quartus® II software, any design targeted for the same device has the same uncompressed configuration file size. If compression is used, the file size can vary after each compilation since the compression ratio is dependent on the design.

Configuration Data Compression

Cyclone II devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Cyclone II devices. During configuration, the Cyclone II device decompresses the bitstream in real time and programs its SRAM cells.

Preliminary data indicates that compression reduces configuration bitstream size by 35 to 55%.

Cyclone II devices support decompression in the AS and PS configuration schemes. Decompression is not supported in JTAG-based configuration.

devices and to the slave configuration devices. Connect the first configuration device's nCS pin to all the Cyclone II device's CONF_DONE pins, and connect the nCASC pin to the nCS pin of the next configuration device in the chain. Leave the nCASC pin of the last configuration device floating. When the master configuration device sends all the data to the Cyclone II device, the configuration device transitions the nCASC pin low, which drives nCS on the next configuration device. Because a configuration device requires less than one clock cycle to activate a subsequent configuration device, the data stream is uninterrupted.

Enhanced configuration devices (EPC16, EPC8, and EPC4 devices) cannot be cascaded.

Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, the master configuration device stops configuration for the entire chain and the entire chain must be reconfigured. For example, if the master configuration device does not detect the Cyclone II device's CONF_DONE pin transitioning high at the end of configuration, it resets the entire chain by transitioning its OE pin low. This low signal drives the OE pin low on the slave configuration device(s) and drives nSTATUS low on all Cyclone II devices, causing them to enter a reset state. This behavior is similar to the FPGA detecting an error in the configuration data.

Figure 13–17 shows how to configure multiple devices using cascaded EPC2 or EPC1 devices.

Combining JTAG & Active Serial Configuration Schemes

You can combine the AS configuration scheme with JTAG-based configuration. Set the MSEL[1..0] pins to 00 (AS mode) or 10 (Fast AS mode)in this setup, which uses two 10-pin download cable headers on the board. The first header programs the serial configuration device in the system via the AS programming interface, and the second header configures the Cyclone II directly via the JTAG interface.

If you try configuring the device using both schemes simultaneously, JTAG configuration takes precedence and AS configuration is terminated.

When a blank serial configuration device is attached to Cyclone II device, turn on the **Halt on-chip configuration controller** option under the Tools menu by clicking **Options**. The Options dialog box appears. In the **Category** list, select **Programmer** before starting the JTAG configuration with the Quartus II programmer. This option stops the AS reconfiguration loop from a blank serial configuration device before starting the JTAG configuration. This includes using the Serial Flash Loader IP because JTAG is used for configuring the Cyclone II device. Users do not need to recompile their Quartus II designs after turning on this Option.

Programming Serial Configuration Devices In-System Using the JTAG Interface

Cyclone II devices in a single device chain or in a multiple device chain support in-system programming of a serial configuration device using the JTAG interface via the serial flash loader design. The board's intelligent host or download cable can use the four JTAG pins on the Cyclone II device to program the serial configuration device in system, even if the host or download cable cannot access the configuration device's configuration pins (DCLK, DATA, ASDI, and nCS pins).

The serial flash loader design is a JTAG-based in-system programming solution for Altera serial configuration devices. The serial flash loader is a bridge design for the FPGA that uses its JTAG interface to access the EPCS JIC (JTAG Indirect Configuration Device Programming) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the serial flash loader design.

In a multiple device chain, you only need to configure the master Cyclone II device which is controlling the serial configuration device. The slave devices in the multiple device chain which are configured by the serial configuration device do not need to be configured when using this