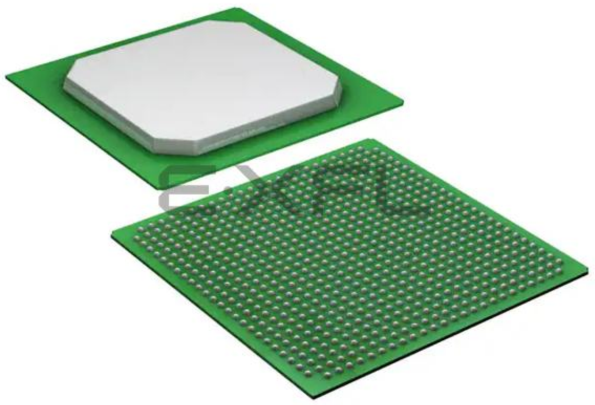
Intel - EP2C50F672C6N Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f672c6n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

A LAB-wide asynchronous load signal to control the logic for the register's preset signal is not available. The register preset is achieved by using a NOT gate push-back technique. Cyclone II devices can only support either a preset or asynchronous clear signal.

In addition to the clear port, Cyclone II devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Cyclone II architecture, connections between LEs, M4K memory blocks, embedded multipliers, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

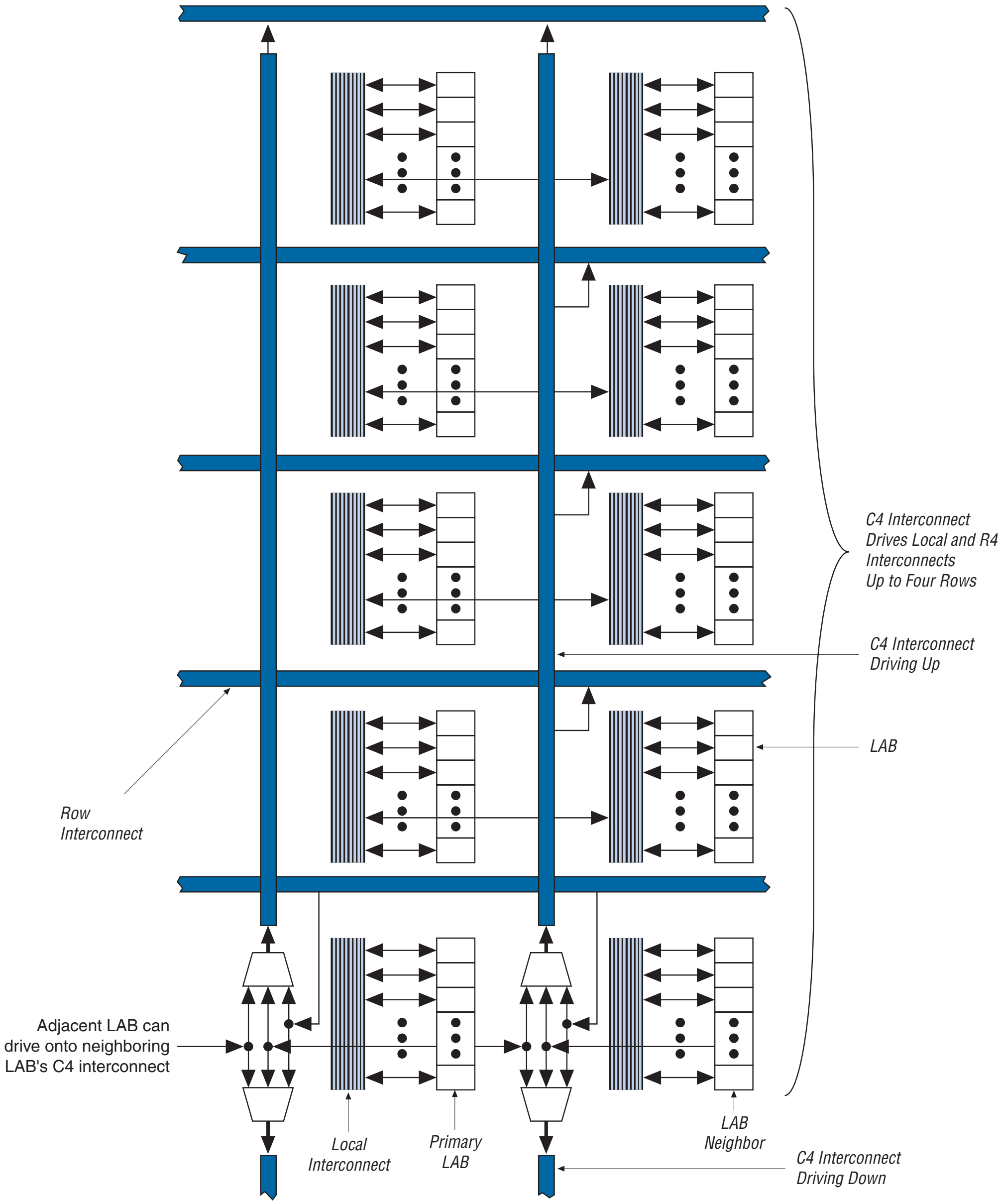
The MultiTrack interconnect consists of row (direct link, R4, and R24) and column (register chain, C4, and C16) interconnects that span fixed distances. A routing structure with fixed-length resources for all devices allows predictable and repeatable performance when migrating through different device densities.

Row Interconnects

Dedicated row interconnects route signals to and from LABs, PLLs, M4K memory blocks, and embedded multipliers within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 interconnects for high-speed access across the length of the device

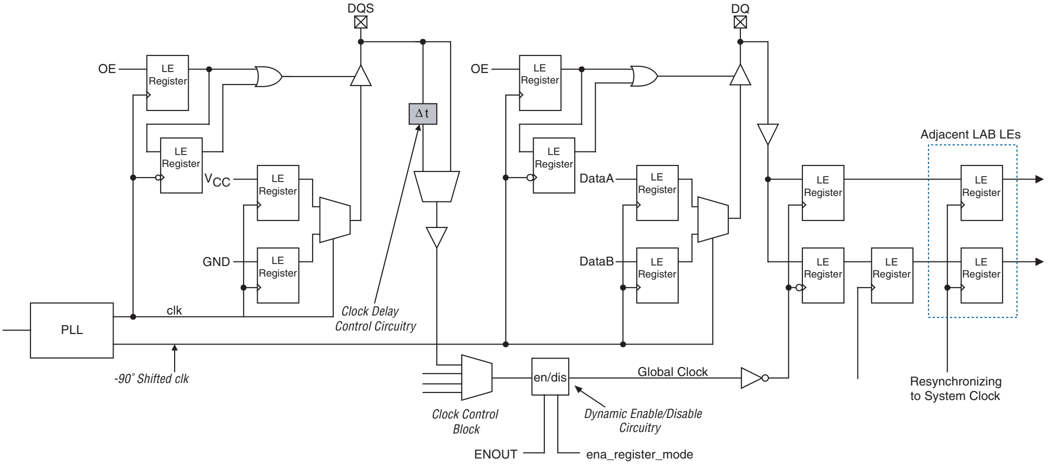
Figure 2–10. C4 Interconnect Connections Note (1)



Note to Figure 2–10:

(1) Each C4 interconnect can drive either up or down four rows.

Figure 2–27. DDR SDRAM Interfacing



For more information on Cyclone II external memory interfaces, see the *External Memory Interfaces* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Table 5–19. M4K Block Internal Timing Microparameters (Part 3 of 3)

Parameter	–6 Speed Grade *(1)*		–7 Speed Grade *(2)*		–8 Speed Grade *(3)*		Unit
	Min	Max	Min	Max	Min	Max	
TM4KCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Notes to Table 5–19:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Cyclone II Clock Timing Parameters

Refer to Tables 5–20 through 5–34 for Cyclone II clock timing parameters.

Table 5–20. Cyclone II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2C5/A Clock Timing Parameters

Tables 5–21 and 5–22 show the clock timing parameters for EP2C5/A devices.

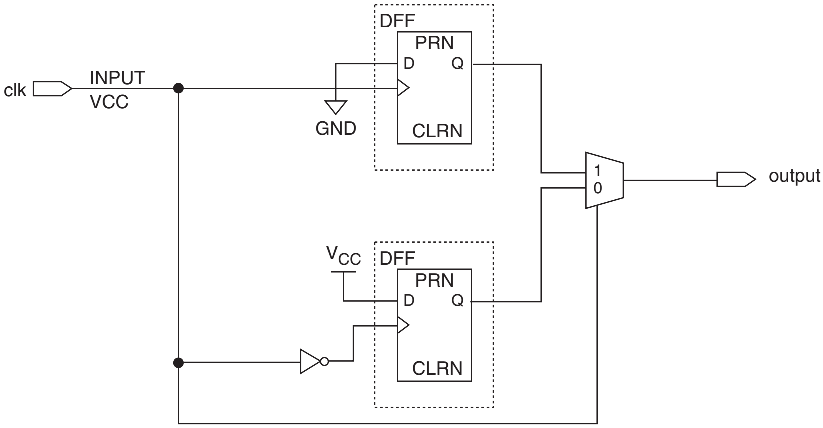
Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade *(1)*	–7 Speed Grade *(2)*	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.283	1.343	2.329	2.484	2.688	2.688	ns
t_{COUT}	1.297	1.358	2.363	2.516	2.717	2.717	ns
t_{PLLCIN}	–0.188	–0.201	0.076	0.038	0.042	0.052	ns

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_2_CLASS_II	16 mA	42	43	45	15	29	42	15	29	42
	20 mA	41	42	44	—	—	—	—	—	—
	24 mA	40	42	43	—	—	—	—	—	—
SSTL_18_ CLASS_I	6 mA	20	22	24	46	47	49	46	47	49
	8 mA	20	22	24	47	49	51	47	49	51
	10 mA	20	22	25	23	25	27	23	25	27
	12 mA	19	23	26	—	—	—	—	—	—
SSTL_18_ CLASS_II	16 mA	30	33	36	—	—	—	—	—	—
	18 mA	29	29	29	—	—	—	—	—	—
1.8V_HSTL_ CLASS_I	8 mA	26	28	29	59	61	63	59	61	63
	10 mA	46	47	48	65	66	68	65	66	68
	12 mA	67	67	67	71	71	72	71	71	72
1.8V_HSTL_ CLASS_II	16 mA	62	65	68	—	—	—	—	—	—
	18 mA	59	62	65	—	—	—	—	—	—
	20 mA	57	59	62	—	—	—	—	—	—
1.5V_HSTL_ CLASS_I	8 mA	40	40	41	28	32	36	28	32	36
	10 mA	41	42	42	—	—	—	—	—	—
	12 mA	43	43	43	—	—	—	—	—	—
1.5V_HSTL_ CLASS_II	16 mA	18	20	21	—	—	—	—	—	—
DIFFERENTIAL_SSTL_2 _CLASS_I	8 mA	46	47	49	25	40	56	25	40	56
	12 mA	67	69	70	23	42	60	23	42	60
DIFFERENTIAL_SSTL_2 _CLASS_II	16 mA	42	43	45	15	29	42	15	29	42
	20 mA	41	42	44	—	—	—	—	—	—
	24 mA	40	42	43	—	—	—	—	—	—
DIFFERENTIAL_SSTL_ 18_CLASS_I	6 mA	20	22	24	46	47	49	46	47	49
	8 mA	20	22	24	47	49	51	47	49	51
	10 mA	20	22	25	23	25	27	23	25	27
	12 mA	19	23	26	—	—	—	—	—	—

Figure 5–10. DCD Measurement Technique for DDIO (Double-Data Rate) Outputs



When an FPGA PLL generates the internal clock, the PLL output clocks the IOE block. As the PLL only monitors the positive edge of the reference clock input and internally re-creates the output clock signal, any DCD present on the reference clock is filtered out. Therefore, the DCD for a DDIO output with PLL in the clock path is better than the DCD for a DDIO output without PLL in the clock path.

Tables 5–55 through 5–58 give the maximum DCD in absolution derivation for different I/O standards on Cyclone II devices. Examples are also provided that show how to calculate DCD as a percentage.

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins Notes (1), (2) (Part 1 of 2)

Row I/O Output Standard	C6	C7	C8	Unit
LVCMOS	165	230	230	ps
LVTTL	195	255	255	ps
2.5-V	120	120	135	ps
1.8-V	115	115	175	ps
1.5-V	130	130	135	ps
SSTL-2 Class I	60	90	90	ps
SSTL-2 Class II	65	75	75	ps
SSTL-18 Class I	90	165	165	ps
HSTL-15 Class I	145	145	205	ps
HSTL-18 Class I	85	155	155	ps

Referenced Documents

This chapter references the following documents:

- *Cyclone II Architecture* chapter in *Cyclone II Device Handbook*
- *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in the *Cyclone II Handbook*
- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Early Power Estimator User Guide*
- *PowerPlay Power Analysis* chapters in volume 3 of the *Quartus II Handbook*

Document Revision History

Table 5–59 shows the revision history for this document.

Table 5–59. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
February 2008 v4.0	• Updated the following tables with I/O timing numbers for automotive-grade devices: Tables 5–2, 5–12, 5–13, 5–15, 5–16, 5–17, 5–18, 5–19, 5–21, 5–22, 5–23, 5–25, 5–26, 5–27, 5–28, 5–36, 5–37, 5–40, 5–41, 5–42, 5–43, 5–55, 5–56, 5–57, and 5–58. • Added "Referenced Documents".	Added I/O timing numbers for automotive-grade devices.
April 2007 v3.2	• Updated Table 5–3.	Updated R_{CONF} typical and maximum values in Table 5–3.

6. Reference & Ordering Information

CII51006-1.4

Software

Cyclone® II devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Quartus II Handbook* for more information on the Quartus II software features.

The free Quartus II Web Edition software, available at **www.Altera.com**, supports Microsoft Windows XP and Windows 2000. The full version of Quartus II software is available through the Altera subscription program. The full version of Quartus II software supports all Altera devices, is available for Windows XP, Windows 2000, Sun Solaris, and Red Hat Linux operating systems, and includes a free suite of popular IP MegaCore® functions for DSP applications and interfacing to external memory devices. Quartus II software and Quartus II Web Edition software support seamless integration with your favorite third party EDA tools.

Device Pin-Outs

Device pin-outs for Cyclone II devices are available on the Altera web site (**www.altera.com**). For more information contact Altera Applications.

Ordering Information

Figure 6–1 describes the ordering codes for Cyclone II devices. For more information on a specific package, contact Altera Applications.

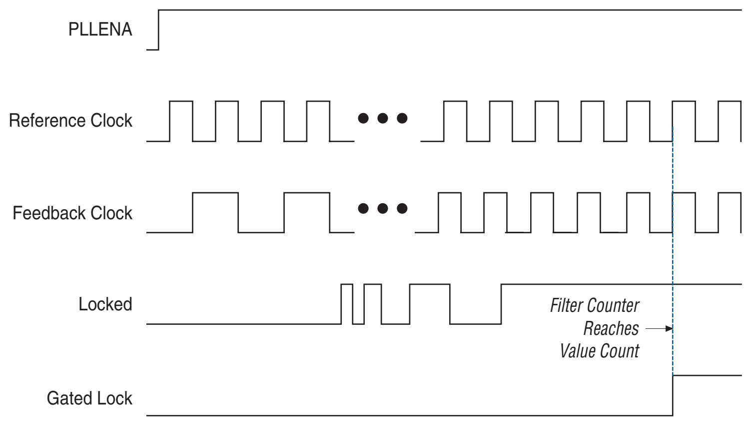
locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals



Single-Clock Mode

Cyclone II memory blocks support single-clock mode for true dual-port, simple dual-port, and single-port memory. In this mode, a single clock, together with a clock enable, controls all registers of the memory block. This mode does not support asynchronous clear signals for the registers. Figures 8–18 through 8–20 show the memory block in single-clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

10. Selectable I/O Standards in Cyclone II Devices

CII51010-2.4

Introduction

The proliferation of I/O standards and the need for improved I/O performance have made it critical that low-cost devices have flexible I/O capabilities. Selectable I/O capabilities such as SSTL-18, SSTL-2, and LVDS compatibility allow Cyclone® II devices to connect to other devices on the same printed circuit board (PCB) that may require different operating and I/O voltages. With these aspects of implementation easily manipulated using the Altera® Quartus® II software, the Cyclone II device family allows you to use low cost FPGAs while keeping pace with increasing design complexity.

This chapter is a guide to understanding the input and output capabilities of the Cyclone II devices, including:

- Supported I/O standards
- Cyclone II I/O banks
- Programmable current drive strength
- I/O termination
- Pad placement and DC guidelines

For information on hot socketing, refer to the *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information on ESD specifications, refer to the *Altera Reliability Report*.

Supported I/O Standards

Cyclone II devices support the I/O standards shown in Table 10–1.

For more details on the I/O standards discussed in this section, including target data rates and voltage values for each I/O standard, refer to the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*.

3.3-V LVCMOS (EIA/JEDEC Standard JESD8-B)

The 3.3-V LVCMOS I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVCMOS standard defines the DC interface parameters for digital circuits operating from a 3.0- or 3.3-V power supply and driving or being driven by LVCMOS-compatible devices.

The LVCMOS standard specifies the same input voltage requirements as LVTTL (-0.3 V $\leq V_I \leq 3.9$ V). The output buffer drives to the rail to meet the minimum high-level output voltage requirements. The 3.3-V I/O standard does not require input reference voltages or board terminations. Cyclone II devices support both input and output levels specified by the 3.3-V LVCMOS I/O standard.

3.3-V (PCI Special Interest Group [SIG] PCI Local Bus Specification Revision 3.0)

The PCI local bus specification is used for applications that interface to the PCI local bus, which provides a processor-independent data path between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems. The conventional PCI specification revision 3.0 defines the PCI hardware environment including the protocol, electrical, mechanical, and configuration specifications for the PCI devices and expansion boards. This standard requires a 3.3-V V_{CCIO}. The 3.3-V PCI standard does not require input reference voltages or board terminations.

The side (left and right) I/O banks on all Cyclone II devices are fully compliant with the 3.3V PCI Local Bus Specification Revision 3.0 and meet 32-bit/66 MHz operating frequency and timing requirements.

Table 10–2 lists the specific Cyclone II devices that support 64- and 32-bit PCI at 66 MHz.

Table 10–2. Cyclone II 66-MHz PCI Support (Part 1 of 2)

Device	Package	–6 and –7 Speed Grades	
		64 Bits	32 Bits
EP2C5	144-pin TQFP		
	208-pin PQFP		✓
	256-pin FineLineBGA®		✓

Figure 10–1. SSTL-2 Class I Termination

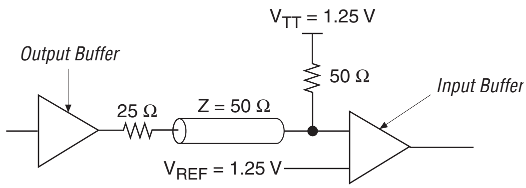
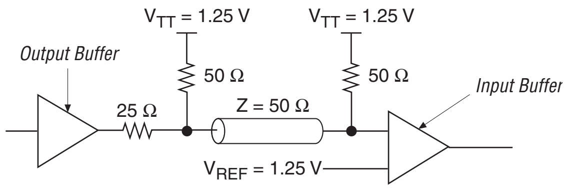


Figure 10–2. SSTL-2 Class II Termination



Cyclone II devices support both input and output SSTL-2 class I and II levels.

Pseudo-Differential SSTL-2

The differential SSTL-2 I/O standard (EIA/JEDEC standard JESD8-9A) is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard specifies an input voltage range of $-0.3\text{ V} \leq V_I \leq V_{CCIO} + 0.3\text{ V}$. The differential SSTL-2 standard does not require an input reference voltage. Refer to Figures 10–3 and 10–4 for details on differential SSTL-2 terminations.

Cyclone II devices do not support true differential SSTL-2 standards. Cyclone II devices support pseudo-differential SSTL-2 outputs for `PLL_OUT` pins and pseudo-differential SSTL-2 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

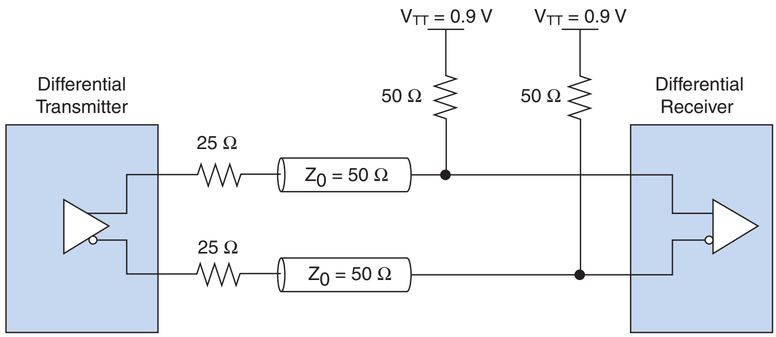
Pseudo-Differential SSTL-18 Class I and Differential SSTL-18 Class II

The 1.8-V differential SSTL-18 standard is formulated under JEDEC Standard, JESD8-15: Stub Series Terminated Logic for 1.8V (SSTL-18).

The differential SSTL-18 I/O standard is a 1.8-V standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard supports differential signals in systems using the SSTL-18 standard and supplements the SSTL-18 standard for differential clocks. Refer to Figures 10–9 and 10–10 for details on differential SSTL-18 termination.

Cyclone II devices do not support true differential SSTL-18 standards. Cyclone II devices support pseudo-differential SSTL-18 outputs for `PLL_OUT` pins and pseudo-differential SSTL-18 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

Figure 10–9. Differential SSTL-18 Class I Termination



Section V. DSP

This section provides information for design and optimization of digital signal processing (DSP) functions and arithmetic operations using the embedded multiplier blocks.

This section includes the following chapter:

- Chapter 12, Embedded Multipliers in Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Configuration File Format

Table 13–3 shows the approximate uncompressed configuration file sizes for Cyclone II devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

Table 13–3. Cyclone II Raw Binary File (.rbf) Sizes *Note (1)*

Device	Data Size (Bits)	Data Size (Bytes)
EP2C5	1,265,792	152,998
EP2C8	1,983,536	247,974
EP2C15	3,892,496	486,562
EP2C20	3,892,496	486,562
EP2C35	6,858,656	857,332
EP2C50	9,963,392	1,245,424
EP2C70	14,319,216	1,789,902

Note to Table 13–3:
(1) These values are preliminary.

Use the data in Table 13–3 only to estimate the file size before design compilation. Different configuration file formats, such as a Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) format, have different file sizes. However, for any specific version of the Quartus® II software, any design targeted for the same device has the same uncompressed configuration file size. If compression is used, the file size can vary after each compilation since the compression ratio is dependent on the design.

Configuration Data Compression

Cyclone II devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Cyclone II devices. During configuration, the Cyclone II device decompresses the bitstream in real time and programs its SRAM cells.

☞ Preliminary data indicates that compression reduces configuration bitstream size by 35 to 55%.

Cyclone II devices support decompression in the AS and PS configuration schemes. Decompression is not supported in JTAG-based configuration.

For more information on configuration issues, see the *Debugging Configuration Problems* chapter of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site (**www.altera.com**).

Multiple Device AS Configuration

You can configure multiple Cyclone II devices using a single serial configuration device. You can cascade multiple Cyclone II devices using the chip-enable (`nCE`) and chip-enable-out (`nCEO`) pins. Connect the `nCE` pin of the first device in the chain to ground and connect the `nCEO` pin to the `nCE` pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the `nCEO` signal high to its V_{CCIO} level to help the internal weak pull-up resistor. When the first device captures all of its configuration data from the bitstream, it transitions its `nCEO` pin low, initiating the configuration of the next device in the chain. You can leave the `nCEO` pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in chain is a Cyclone II device.

The Quartus II software sets the Cyclone II device `nCEO` pin as an output pin driving to ground by default. If the device is in a chain, and the `nCEO` pin is connected to the next device's `nCE` pin, you must make sure that the `nCEO` pin is not used as a user I/O pin after configuration. The software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

The first Cyclone II device in the chain is the configuration master and controls the configuration of the entire chain. Select the AS configuration scheme for the first Cyclone II device and the PS configuration scheme for the remaining Cyclone II devices (configuration slaves). Any other Altera® device that supports PS configuration can also be part of the chain as a configuration slave. In a multiple device chain, the `nCONFIG`, `nSTATUS`, `CONF_DONE`, `DCLK`, and `DATA0` pins of each device in the chain are connected (see Figure 13–4). Figure 13–4 shows the pin connections for this setup.

Combining JTAG & Active Serial Configuration Schemes

You can combine the AS configuration scheme with JTAG-based configuration. Set the `MSEL[1..0]` pins to 00 (AS mode) or 10 (Fast AS mode)in this setup, which uses two 10-pin download cable headers on the board. The first header programs the serial configuration device in the system via the AS programming interface, and the second header configures the Cyclone II directly via the JTAG interface.

If you try configuring the device using both schemes simultaneously, JTAG configuration takes precedence and AS configuration is terminated.

When a blank serial configuration device is attached to Cyclone II device, turn on the **Halt on-chip configuration controller** option under the Tools menu by clicking **Options**. The Options dialog box appears. In the **Category** list, select **Programmer** before starting the JTAG configuration with the Quartus II programmer. This option stops the AS reconfiguration loop from a blank serial configuration device before starting the JTAG configuration. This includes using the Serial Flash Loader IP because JTAG is used for configuring the Cyclone II device. Users do not need to recompile their Quartus II designs after turning on this Option.

Programming Serial Configuration Devices In-System Using the JTAG Interface

Cyclone II devices in a single device chain or in a multiple device chain support in-system programming of a serial configuration device using the JTAG interface via the serial flash loader design. The board's intelligent host or download cable can use the four JTAG pins on the Cyclone II device to program the serial configuration device in system, even if the host or download cable cannot access the configuration device's configuration pins (`DCLK`, `DATA`, `ASDI`, and `nCS` pins).

The serial flash loader design is a JTAG-based in-system programming solution for Altera serial configuration devices. The serial flash loader is a bridge design for the FPGA that uses its JTAG interface to access the EPCS JIC (JTAG Indirect Configuration Device Programming) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the serial flash loader design.

In a multiple device chain, you only need to configure the master Cyclone II device which is controlling the serial configuration device. The slave devices in the multiple device chain which are configured by the serial configuration device do not need to be configured when using this

672-Pin FineLine BGA Package, Option 3 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

Tables 15–17 and 15–18 show the package information and package outline figure references, respectively, for the 672-pin FineLine BGA package.

Table 15–17. 672-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAL-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	7.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–18. 672-Pin FineLine BGA Package Outline Dimensions

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	27.00 BSC		
E	27.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		