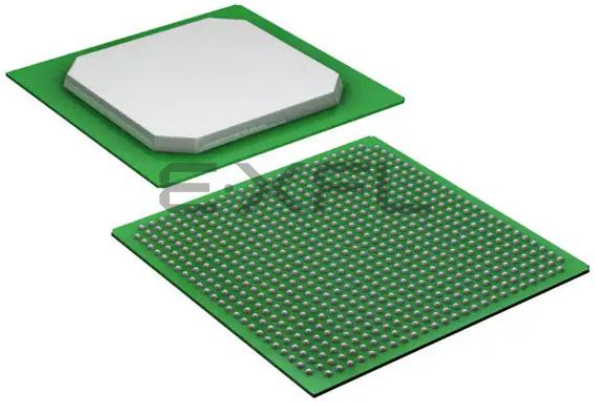

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f672c7

Chapter Revision Dates

The chapters in this book, *Cyclone II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
Revised: *February 2008*
Part number: *CII51001-3.2*

Chapter 2. Cyclone II Architecture
Revised: *February 2007*
Part number: *CII51002-3.1*

Chapter 3. Configuration & Testing
Revised: *February 2007*
Part number: *CII51003-2.2*

Chapter 4. Hot Socketing & Power-On Reset
Revised: *February 2007*
Part number: *CII51004-3.1*

Chapter 5. DC Characteristics and Timing Specifications
Revised: *February 2008*
Part number: *CII51005-4.0*

Chapter 6. Reference & Ordering Information
Revised: *February 2007*
Part number: *CII51006-1.4*

Chapter 7. PLLs in Cyclone II Devices
Revised: *February 2007*
Part number: *CII51007-3.1*

Chapter 8. Cyclone II Memory Blocks
Revised: *February 2008*
Part number: *CII51008-2.4*

Chapter 9. External Memory Interfaces
Revised: *February 2007*
Part number: *CII51009-3.1*

Table 1–1. Cyclone II FPGA Family Features (Part 2 of 2)

Feature	EP2C5 (2)	EP2C8 (2)	EP2C15 (1)	EP2C20 (2)	EP2C35	EP2C50	EP2C70
Maximum user I/O pins	158	182	315	315	475	450	622

Notes to Table 1–1:

(1) The EP2C15A is only available with the Fast On feature, which offers a faster POR time. This device is available in both commercial and industrial grade.

(2) The EP2C5, EP2C8, and EP2C20 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. The EP2C8A and EP2C20A devices are only available in industrial grade.

(3) This is the total number of 18 × 18 multipliers. For the total number of 9 × 9 multipliers per device, multiply the total number of 18 × 18 multipliers by 2.

PLLs

Cyclone II PLLs provide general-purpose clocking as well as support for the following features:

- Clock multiplication and division
- Phase shifting
- Programmable duty cycle
- Up to three internal clock outputs
- One dedicated external clock output
- Clock outputs for differential I/O support
- Manual clock switchover
- Gated lock signal
- Three different clock feedback modes
- Control signals

Cyclone II devices contain either two or four PLLs. Table 2–3 shows the PLLs available for each Cyclone II device.

Table 2–3. Cyclone II Device PLL Availability

Device	PLL1	PLL2	PLL3	PLL4
EP2C5	✓	✓		
EP2C8	✓	✓		
EP2C15	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes

Clock Mode	Description
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`.
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

Table 2–9. Cyclone II M4K Memory Clock Modes

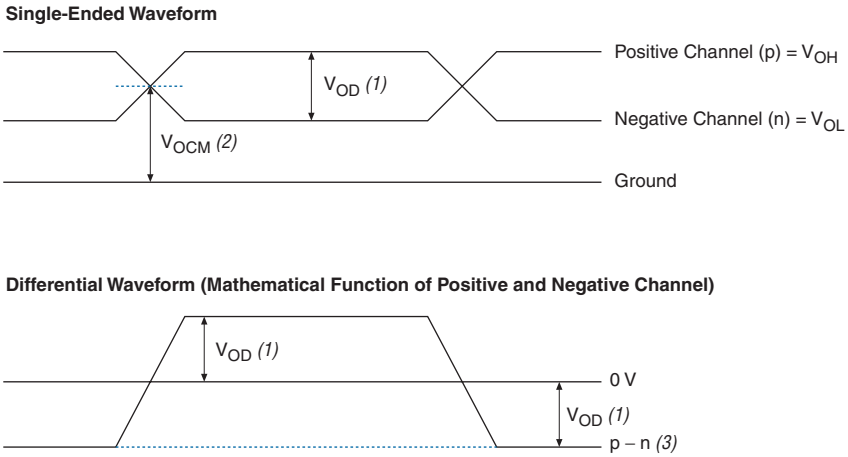
Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Figure 5–2 shows the transmitter output waveforms for all supported differential output standards (LVDS, mini-LVDS, RSDS, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards



Notes to Figure 5–2:
(1) V_{OD} is the output differential voltage. $V_{OD} = |p - n|$.
(2) V_{OCM} is the output common mode voltage. $V_{OCM} = (p + n)/2$.
(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–9 shows the DC characteristics for user I/O pins with differential I/O standards.

Table 5–9. DC Characteristics for User I/O Pins Using Differential I/O Standards Note (1) (Part 1 of 2)

I/O Standard	V_{OD} (mV)			ΔV_{OD} (mV)		V_{OCM} (V)			V_{OH} (V)		V_{OL} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	250	—	600	—	50	1.125	1.25	1.375	—	—	—	—
mini-LVDS (2)	300	—	600	—	50	1.125	1.25	1.375	—	—	—	—
RSDS (2)	100	—	600	—	—	1.125	1.25	1.375	—	—	—	—
Differential 1.5-V HSTL class I and II (3)	—	—	—	—	—	—	—	—	V_{CCIO} – 0.4	—	—	0.4

Table 5–27. EP2C20/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.337	–0.357	0.079	0.04	0.075	0.045	ns

Notes to Table 5–27:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–28. EP2C20/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.542	1.615	2.490	2.651	2.886	2.866	ns
t_{COUT}	1.544	1.617	2.506	2.664	2.894	2.874	ns
t_{PLLCIN}	–0.424	–0.448	–0.057	–0.107	–0.077	–0.107	ns
$t_{PLLCOUT}$	–0.422	–0.446	–0.041	–0.094	–0.069	–0.099	ns

Notes to Table 5–28:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C35 Clock Timing Parameters

Tables 5–29 and 5–30 show the clock timing parameters for EP2C35 devices.

Table 5–29. EP2C35 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.499	1.569	2.652	2.878	3.155	ns
t_{COUT}	1.513	1.584	2.686	2.910	3.184	ns
t_{PLLCIN}	–0.026	–0.032	0.272	0.316	0.41	ns
$t_{PLLCOUT}$	–0.012	–0.017	0.306	0.348	0.439	ns

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 3 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
1.8V_HSTL_ CLASS_I	8 mA	t_{OP}	1364	1430	2853	3017	3178	3184	ps
		t_{DIP}	1488	1562	3061	3254	3451	3451	ps
	10 mA	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
	12 mA (1)	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
1.5V_HSTL_ CLASS_I	8 mA (1)	t_{OP}	1657	1738	3642	3917	4185	4191	ps
		t_{DIP}	1781	1870	3850	4154	4458	4458	ps
DIFFERENTIAL_ SSTL_2_ CLASS_I	8 mA	t_{OP}	1090	1142	2152	2268	2376	2382	ps
		t_{DIP}	1214	1274	2360	2505	2649	2649	ps
	12 mA (1)	t_{OP}	1097	1150	2131	2246	2354	2360	ps
		t_{DIP}	1221	1282	2339	2483	2627	2627	ps
DIFFERENTIAL_ SSTL_2_ CLASS_II	16 mA (1)	t_{OP}	1068	1119	2067	2177	2281	2287	ps
		t_{DIP}	1192	1251	2275	2414	2554	2554	ps
DIFFERENTIAL_ SSTL_18_ CLASS_I	6 mA	t_{OP}	1371	1437	2828	3018	3200	3206	ps
		t_{DIP}	1495	1569	3036	3255	3473	3473	ps
	8 mA	t_{OP}	1365	1431	2832	3024	3209	3215	ps
		t_{DIP}	1489	1563	3040	3261	3482	3482	ps
	10 mA (1)	t_{OP}	1374	1440	2806	2990	3167	3173	ps
		t_{DIP}	1498	1572	3014	3227	3440	3440	ps
1.8V_ DIFFERENTIAL_ HSTL_ CLASS_I	8 mA	t_{OP}	1364	1430	2853	3017	3178	3184	ps
		t_{DIP}	1488	1562	3061	3254	3451	3451	ps
	10 mA	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
	12 mA (1)	t_{OP}	1332	1396	2842	3011	3173	3179	ps
		t_{DIP}	1456	1528	3050	3248	3446	3446	ps
1.5V_ DIFFERENTIAL_ HSTL_ CLASS_I	8 mA (1)	t_{OP}	1657	1738	3642	3917	4185	4191	ps
		t_{DIP}	1781	1870	3850	4154	4458	4458	ps

Table 5–53 shows the JTAG timing parameters and values for Cyclone II devices.

Table 5–53. Cyclone II JTAG Timing Parameters and Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU}	JTAG port setup time *(2)*	5	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(2)*	—	13	ns
t_{JPZX}	JTAG port high impedance to valid output *(2)*	—	13	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2)*	—	13	ns
t_{JSSU}	Capture register setup time *(2)*	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5–53:

(1) This information is preliminary.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the JTAG port and capture register clock setup time is 3 ns and port clock to output time is 15 ns.

Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Cyclone II devices are in the 18th position or after they will fail configuration. This does not affect the SignalTap® II logic analyzer.

For more information on JTAG, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in the *Cyclone II Handbook*.

The VCO frequency is a critical parameter that must be between 300 and 1,000 MHz to ensure proper operation of the PLL. The Quartus II software automatically sets the VCO frequency within the recommended range based on the clock output and phase-shift requirements in your design.

PLL Reference Clock Generation

In Cyclone II devices, up to four clock pins can drive the PLL, as shown in Figure 7–11 on page 7–26. The multiplexer output feeds the PLL reference clock input. The PLL has internal delay elements that compensate for the clock delay from the input pin to the clock input port of the PLL.

Table 7–3 shows the clock input pin connections to the PLLs in the Cyclone II device.

Table 7–3. PLL Clock Input Pin Connections

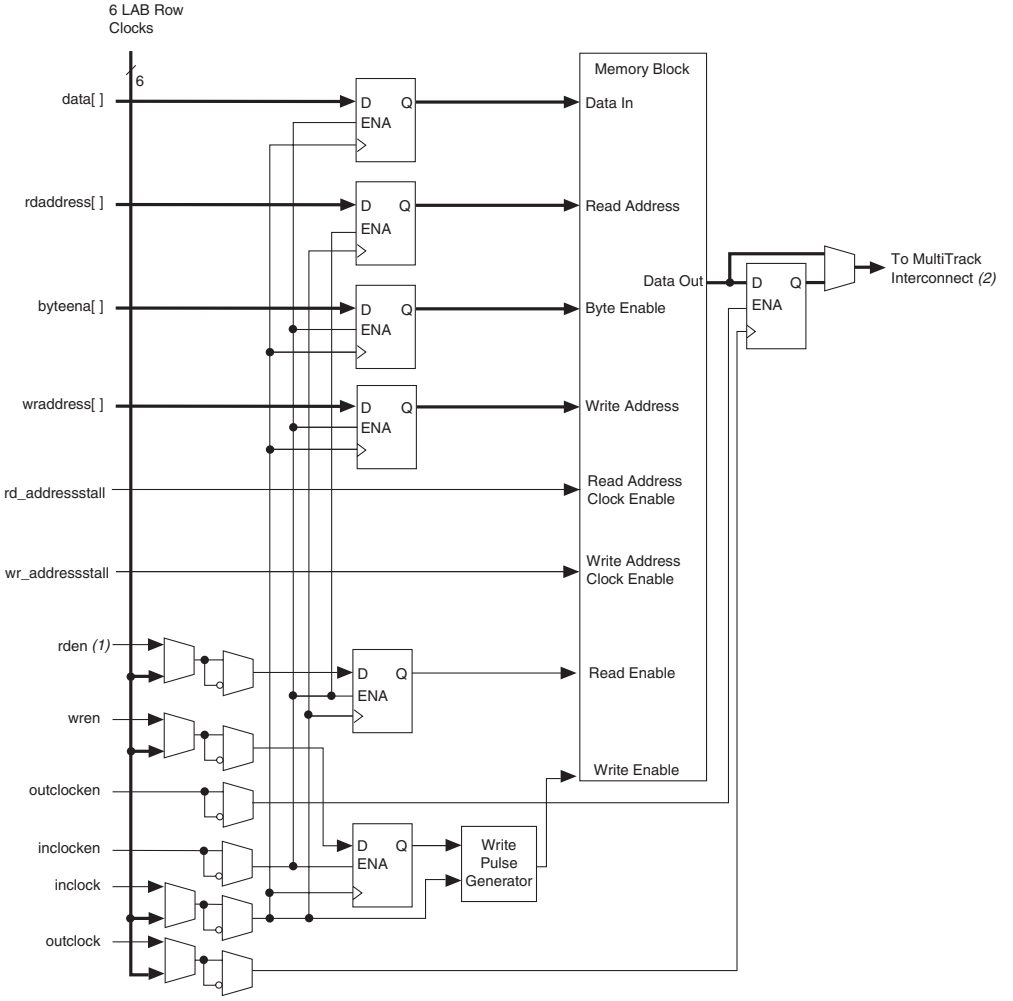
Device	PLL 1		PLL 2		PLL 3		PLL 4	
	CLK0 CLK1	CLK2 CLK3	CLK4 CLK5	CLK6 CLK7	CLK8 CLK9	CLK10 CLK11	CLK12 CLK13	CLK14 CLK15
EP2C5	✓	✓	✓	✓				
EP2C8	✓	✓	✓	✓				
EP2C15	✓	✓	✓	✓	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓	✓	✓	✓	✓

Each PLL can be fed by one of four single-ended or two differential clock input pins. For example, PLL 1 can be fed by `CLK[3..0]` when using a single-ended I/O standard. When your design uses a differential I/O standard, these same clock pins have a secondary function as `LVDSCLK[2..1]p` and `LVDSCLK[2..1]n` pins. When using differential clocks, the `CLK0` pin's secondary function is `LVDSCLK1p`, the `CLK1` pin's secondary function is `LVDSCLK1n`, etc.

Table 7–8. Global Clock Network Connections (Part 2 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PLL4_c0													✓	✓		✓
PLL4_c1													✓		✓	✓
PLL4_c2														✓	✓	
DPCLK0 *(1)*	✓															
DPCLK1 *(1)*		✓														
DPCLK10 *(1)*, *(2)* CDPCLK0 or CDPCLK7 *(3)*			✓													
DPCLK2 *(1)*, *(2)* CDPCLK1 or CDPCLK2 *(3)*				✓												
DPCLK7 *(1)*					✓											
DPCLK6 *(1)*						✓										
DPCLK8 *(1)*, *(2)* CDPCLK5 or CDPCLK6 *(3)*							✓									
DPCLK4 *(1)*, *(2)* CDPCLK4 or CDPCLK3 *(3)*								✓								
DPCLK8 *(1)*									✓							
DPCLK11 *(1)*										✓						
DPCLK9 *(1)*											✓					
DPCLK10 *(1)*												✓				
DPCLK5 *(1)*													✓			
DPCLK2 *(1)*														✓		
DPCLK4 *(1)*															✓	

Figure 8–15. Cyclone II Input/Output Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*



Notes to Figure 8–15:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack™ interconnect.

Figure 9–13 shows waveforms of the circuit shown in Figure 9–11. The first set of waveforms in Figure 9–13 shows the edge-aligned relationship between the DQ and DQS signals at the Cyclone II device pins. The second set of waveforms in Figure 9–13 shows what happens if the shifted DQS signal is not inverted. In this case, the last data, Q_n, does not get latched into the logic array as DQS goes to tri-state after the read postamble time. The third set of waveforms in Figure 9–13 shows a proper read operation with the DQS signal inverted after the 90° shift. The last data, Q_n, does get latched. In this case the outputs of register A_I and register C_I, which correspond to `dataout_h` and `dataout_l` ports, are now switched because of the DQS inversion. Register A_I, register B_I, and register C_I refer to the nomenclature in Figure 9–11.

Figure 9–13. DQ Captures With Noninverted & Inverted Shifted DQS

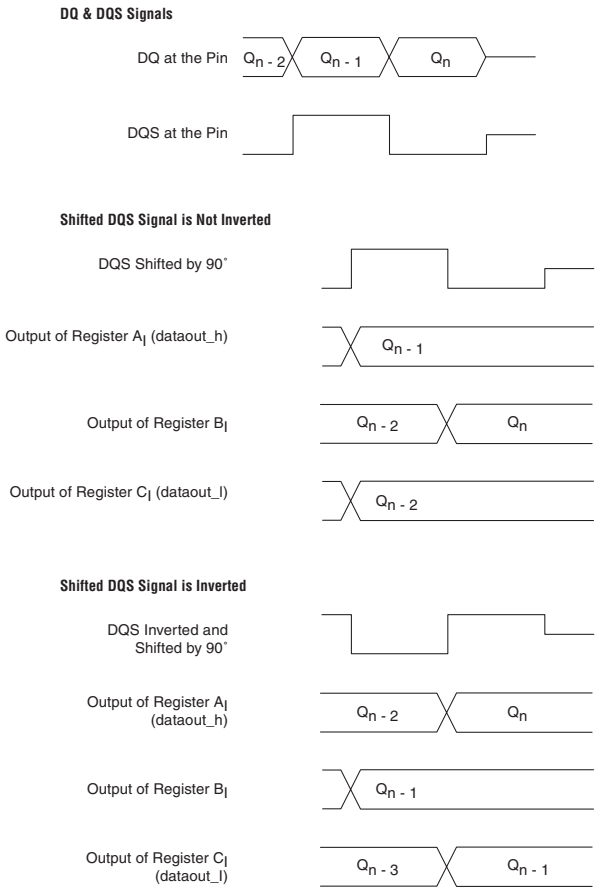
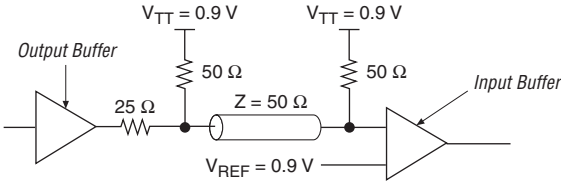


Figure 10–6. 1.8-V SSTL Class II Termination



1.8-V HSTL Class I and II

The HSTL standard is a technology independent I/O standard developed by JEDEC to provide voltage scalability. It is used for applications designed to operate in the 0.0- to 1.8-V HSTL logic switching range such as quad data rate (QDR) memory clock interfaces.

Although JEDEC specifies a maximum V_{CCIO} value of 1.6 V, there are various memory chip vendors with HSTL standards that require a V_{CCIO} of 1.8 V. Cyclone II devices support interfaces with V_{CCIO} of 1.8 V for HSTL. Figures 10–7 and 10–8 show the nominal V_{REF} and V_{TT} required to track the higher value of V_{CCIO}. The value of V_{REF} is selected to provide optimum noise margin in the system. Cyclone II devices support both input and output levels of operation.

Figure 10–7. 1.8-V HSTL Class I Termination

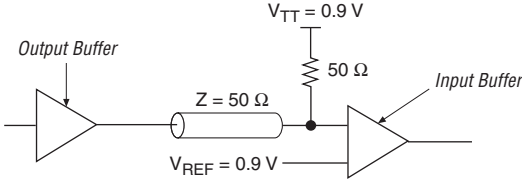
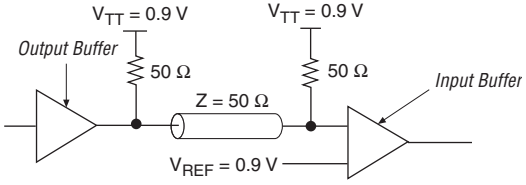


Figure 10–8. 1.8-V HSTL Class II Termination



See the *Cyclone II Memory Blocks* chapter in Volume 1 of the ***Cyclone II Device Handbook*** for more information on Cyclone II M4K memory blocks.

Refer to *AN 306: Techniques for Implementing Multipliers in FPGA Devices* for more information on soft multipliers.

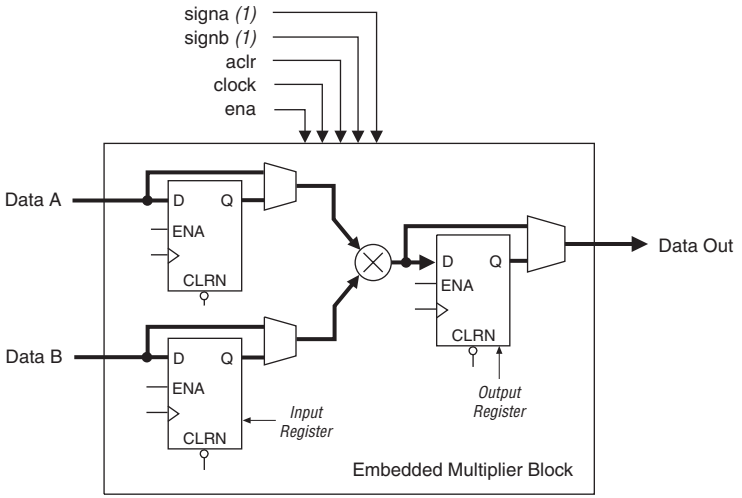
Architecture

Each embedded multiplier consists of the following elements:

- Multiplier stage
- Input and output registers
- Input and output interfaces

Figure 12–2 shows the multiplier block architecture.

Figure 12–2. Multiplier Block Architecture



Note to Figure 12–2:

(1) If necessary, you can send these signals through one register to match the data signal path.

Input Registers

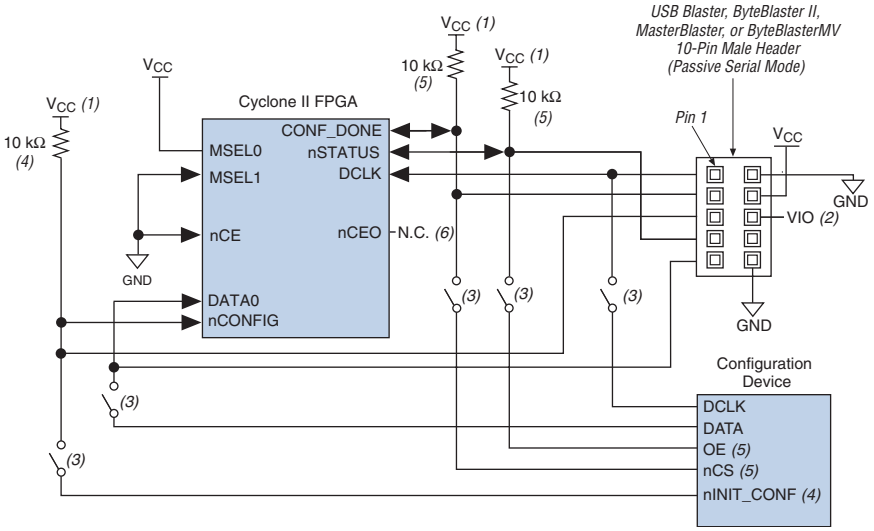
You can send each multiplier input signal into an input register or directly into the multiplier in 9- or 18-bit sections depending on the operational mode of the multiplier. You can send each multiplier input signal through a register independently of each other (e.g., you can send the multiplier's

nCONFIG low for at least 2 µs to restart configuration. The microprocessor or controller can only transition the nCONFIG pin low if the pin is under system control and not tied to V_{CC}.

The enhanced configuration devices support parallel configuration of up to eight devices. The *n*-bit (*n* = 1, 2, 4, or 8) PS configuration mode allows enhanced configuration devices to concurrently configure a chain of FPGAs. These devices do not have to be the same device family or density; they can be any combination of Altera FPGAs with different designs. An individual enhanced configuration device DATA pin is available for each targeted FPGA. Each DATA line can also feed a chain of FPGAs. Figure 13–15 shows how to concurrently configure multiple devices using an enhanced configuration device.

the five common signals (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) between the cable and the configuration device. You can also remove the configuration device from the board when configuring the FPGA with the cable. Figure 13–21 shows a combination of a configuration device and a download cable to configure an FPGA.

Figure 13–21. PS Configuration with a Download Cable & Configuration Device Circuit



Notes to Figure 13–21:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(3) You should not attempt configuration with a download cable while a configuration device is connected to a Cyclone II device. Instead, you should either remove the configuration device from its socket when using the download cable or place a switch on the five common signals between the download cable and the configuration device.

(4) The nINIT_CONF pin (available on enhanced configuration devices and EPC2 devices only) has an internal pull-up resistor that is always active. This means an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used or not available (e.g., on EPC1 devices), nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(5) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

(6) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

feature. To use this feature successfully, set the MSEL[1..0] pins of the master Cyclone II device to select the AS configuration scheme or fast AS configuration scheme (see Table 13–1).

The Quartus II software version 4.1 and higher supports serial configuration device ISP through an FPGA JTAG interface using a JIC file.

The serial configuration device in-system programming through the Cyclone II JTAG interface has three stages, which are described in the following sections.

Loading the Serial Flash Loader Design

The serial flash loader design is a design inside the Cyclone II device that bridges the JTAG interface and AS interface inside the Cyclone II device using glue logic.

The intelligent host uses the JTAG interface to configure the master Cyclone II device with a serial flash loader design. The serial flash loader design allows the master Cyclone II device to control the access of four serial configuration device pins, also known as the Active Serial Memory Interface (ASMI) pins, through the JTAG interface. The ASMI pins are the serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS) pins.

If you configure a master Cyclone II device with a serial flash loader design, the master Cyclone II device can enter user mode even though the slave devices in the multiple device chain are not being configured. The master Cyclone II device can enter user mode with a serial flash loader design even though the CONF_DONE signal is externally held low by the other slave devices in chain. Figure 13–25 shows the JTAG configuration of a single Cyclone II device with a serial flash loader design.

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCEO	N/A if option is on. I/O if option is off.	All	Output	This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration. If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. Use the Quartus II software to make this pin a user I/O pin.
ASDO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data. In AS mode, ASDO has an internal pull-up that is always active.
nCSO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

Thermal Resistance

Thermal resistance values for Cyclone II devices are provided for a board meeting JEDEC specifications and for a typical board. The values provided are as follows:

- θ_{JA} (°C/W) Still Air—Junction-to-ambient thermal resistance with no airflow when a heat sink is not being used.
- θ_{JA} (°C/W) 100 ft./minute—Junction-to-ambient thermal resistance with 100 ft./minute airflow when a heat sink is not being used.
- θ_{JA} (°C/W) 200 ft./minute—Junction-to-ambient thermal resistance with 200 ft./minute airflow when a heat sink is not being used.
- θ_{JA} (°C/W) 400 ft./minute—Junction-to-ambient thermal resistance with 400 ft./minute airflow when a heat sink is not being used.
- θ_{JC} (°C/W)—Junction-to-case thermal resistance for device.
- θ_{JB} (°C/W)—Junction-to-board thermal resistance for specific board being used.

Table 15–2 provides θ_{JA} (junction-to-ambient thermal resistance) values and θ_{JC} (junction-to-case thermal resistance) values for Cyclone II devices on a board meeting JEDEC specifications for thermal resistance calculation. The JEDEC board specifications require two signal and two power/ground planes and are available at **www.jedec.org**.

Table 15–2. Thermal Resistance of Cyclone II Devices for Board Meeting JEDEC Specifications (Part 1 of 2)

Device	Pin Count	Package	θ_{JA} (°C/W) Still Air	θ_{JA} (°C/W) 100 ft./min.	θ_{JA} (°C/W) 200 ft./min.	θ_{JA} (°C/W) 400 ft./min.	θ_{JC} (°C/W)
EP2C5	144	TQFP	31	29.3	27.9	25.5	10
	208	PQFP	30.4	29.2	27.3	22.3	5.5
	256	FineLine BGA	30.2	26.1	23.6	21.7	8.7
EP2C8	144	TQFP	29.8	28.3	26.9	24.9	9.9
	208	PQFP	30.2	28.8	26.9	21.7	5.4
	256	FineLine BGA	27	23	20.5	18.5	7.1
EP2C15	256	FineLine BGA	24.2	20	17.8	16	5.5
	484	FineLine BGA	21	17	14.8	13.1	4.2
EP2C20	240	PQFP	26.6	24	21.4	17.4	4.2
	256	FineLine BGA	24.2	20	17.8	16	5.5
	484	FineLine BGA	21	17	14.8	13.1	4.2
EP2C35	484	FineLine BGA	19.4	15.4	13.3	11.7	3.3
	484	Ultra FineLine BGA	20.6	16.6	14.5	12.8	5
	672	FineLine BGA	18.6	14.6	12.6	11.1	3.1

672-Pin FineLine BGA Package, Option 3 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

Tables 15–17 and 15–18 show the package information and package outline figure references, respectively, for the 672-pin FineLine BGA package.

Table 15–17. 672-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAL-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	7.7 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–18. 672-Pin FineLine BGA Package Outline Dimensions

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	27.00 BSC		
E	27.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		