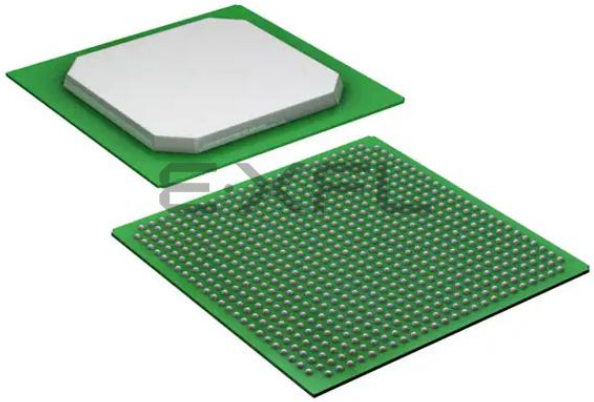

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f672c7n

Global Clock Network

The 16 or 8 global clock networks drive throughout the entire device. Dedicated clock pins (CLK[]), PLL outputs, the logic array, and dual-purpose clock (DPCLK[]) pins can also drive the global clock network.

The global clock network can provide clocks for all resources within the device, such as IOEs, LEs, memory blocks, and embedded multipliers. The global clock lines can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin, or DQS signals for DDR SDRAM or QDRII SRAM interfaces. Internal logic can also drive the global clock network for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fan-out.

Clock Control Block

There is a clock control block for each global clock network available in Cyclone II devices. The clock control blocks are arranged on the device periphery and there are a maximum of 16 clock control blocks available per Cyclone II device. The larger Cyclone II devices (EP2C15 devices and larger) have 16 clock control blocks, four on each side of the device. The smaller Cyclone II devices (EP2C5 and EP2C8 devices) have eight clock control blocks, four on the left and right sides of the device.

The control block has these functions:

- Dynamic global clock network clock source selection
- Dynamic enable/disable of the global clock network

In Cyclone II devices, the dedicated CLK[] pins, PLL counter outputs, DPCLK[] pins, and internal logic can all feed the clock control block. The output from the clock control block in turn feeds the corresponding global clock network.

The following sources can be inputs to a given clock control block:

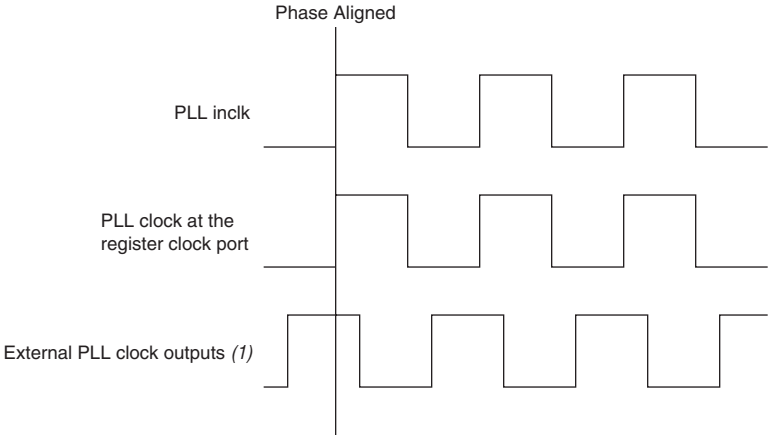
- Four clock pins on the same side as the clock control block
- Three PLL clock outputs from a PLL
- Four DPCLK pins (including CDPCLK pins) on the same side as the clock control block
- Four internally-generated signals

Tables 5–50 and 5–51 show the LVDS timing budget for Cyclone II devices. Cyclone II devices support LVDS receivers at data rates up to 805 Mbps, and LVDS transmitters at data rates up to 640 Mbps.

Table 5–50. LVDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
		Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	
f_{HSCLK} (input clock frequency)	×10	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×8	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×7	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×4	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×2	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (8)	402.5 (8)	MHz
HSIODR	×10	100	—	640	640	100	—	550	640	100	—	311 (5)	550 (7)	Mbps
	×8	80	—	640	640	80	—	550	640	80	—	311 (5)	550 (7)	Mbps
	×7	70	—	640	640	70	—	550	640	70	—	311 (5)	550 (7)	Mbps
	×4	40	—	640	640	40	—	550	640	40	—	311 (5)	550 (7)	Mbps
	×2	20	—	640	640	20	—	550	640	20	—	311 (5)	550 (7)	Mbps
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (9)	402.5 (9)	Mbps
t_{DUTY}	—	45	—	55	—	45	—	55	—	45	—	55	—	%
	—	—	—	—	160	—	—	—	312.5	—	—	—	363.6	ps
TCCS (3)	—	—	—	200		—	—	200		—	—	200		ps
Output jitter (peak to peak)	—	—	—	500		—	—	500		—	—	550 (10)		ps
t_{RISE}	20–80%	150	200	250		150	200	250		150	200	250 (11)		ps

Figure 7–4. Phase Relationship between Cyclone II PLL Clocks in Normal Mode

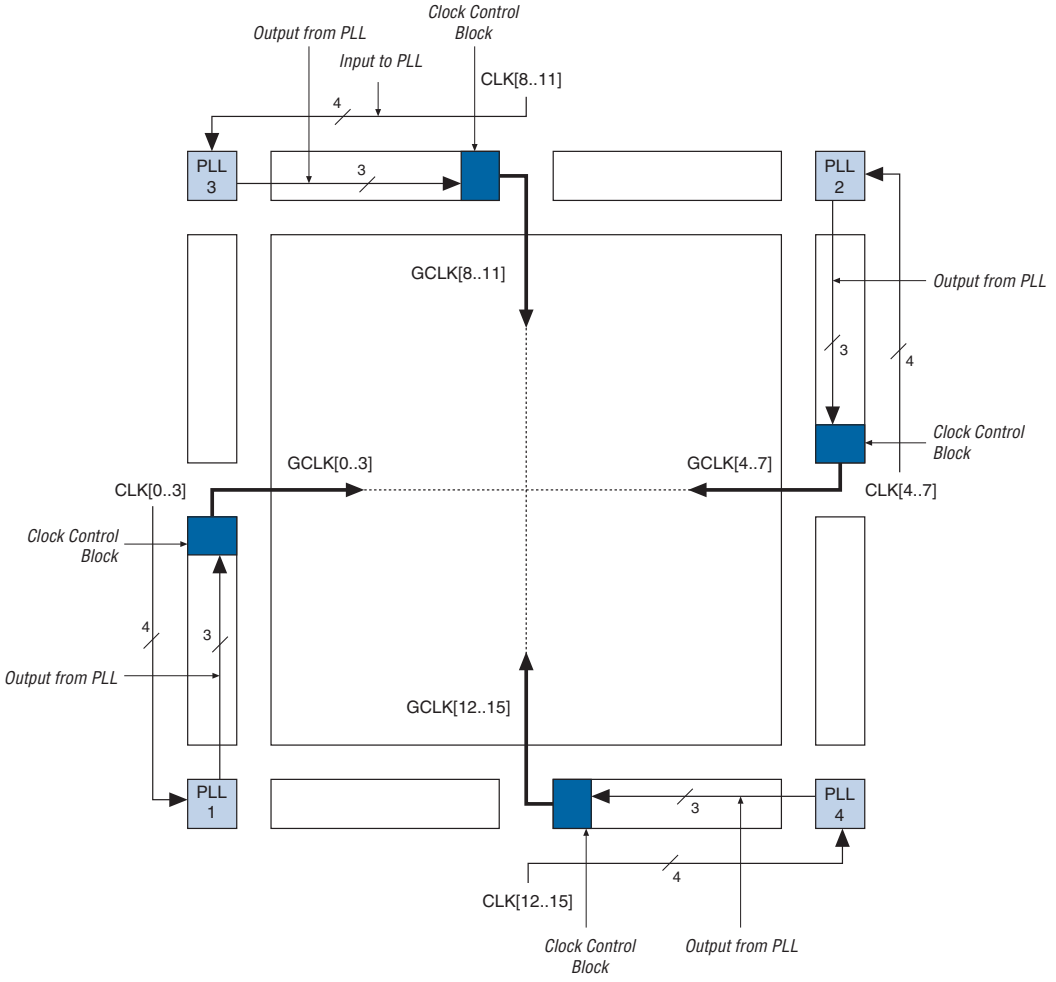


Note to Figure 7–4:
(1) The external clock output can lead or lag the PLL clock signals.

Zero Delay Buffer Mode

In zero delay buffer mode, the clock signal on the PLL external clock output pin (PLL<#>_OUT), fed by the c2 counter, is phase-aligned with the PLL input clock pin for zero delay. If the c[1..0] ports drive internal clock ports, there is a phase shift with respect to the input clock pin. Figure 7–5 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 7–12. Cyclone II Clock Control Blocks Placement



The inputs to the four clock control blocks on each side are chosen from among the following clock sources:

- Four clock input pins
- Three PLL counter outputs
- Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins and two CDPCLK pins from both the top and bottom
- Four signals from internal logic

VCCA & GNDA

Each Cyclone II PLL uses separate VCC and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called VCCA_PLL<*PLL number*> and GNDA_ PLL<*PLL number*>. Connect the VCCA power pin to a 1.2-V power supply, even if you do not use the PLL. Isolate the power connected to VCCA from the power to the rest of the Cyclone II device or any other digital device on the board. You can use one of three different methods of isolating the VCCA pin:

- Use separate VCCA power planes
- Use a partitioned VCCA island within the VCCINT plane
- Use thick VCCA traces

Separate VCCA Power Plane

A mixed signal system is already partitioned into analog and digital sections, each with its own power planes on the board. To isolate the VCCA pin using a separate VCCA power plane, connect the VCCA pin to the analog 1.2-V power plane.

Partitioned VCCA Island Within the VCCINT Plane

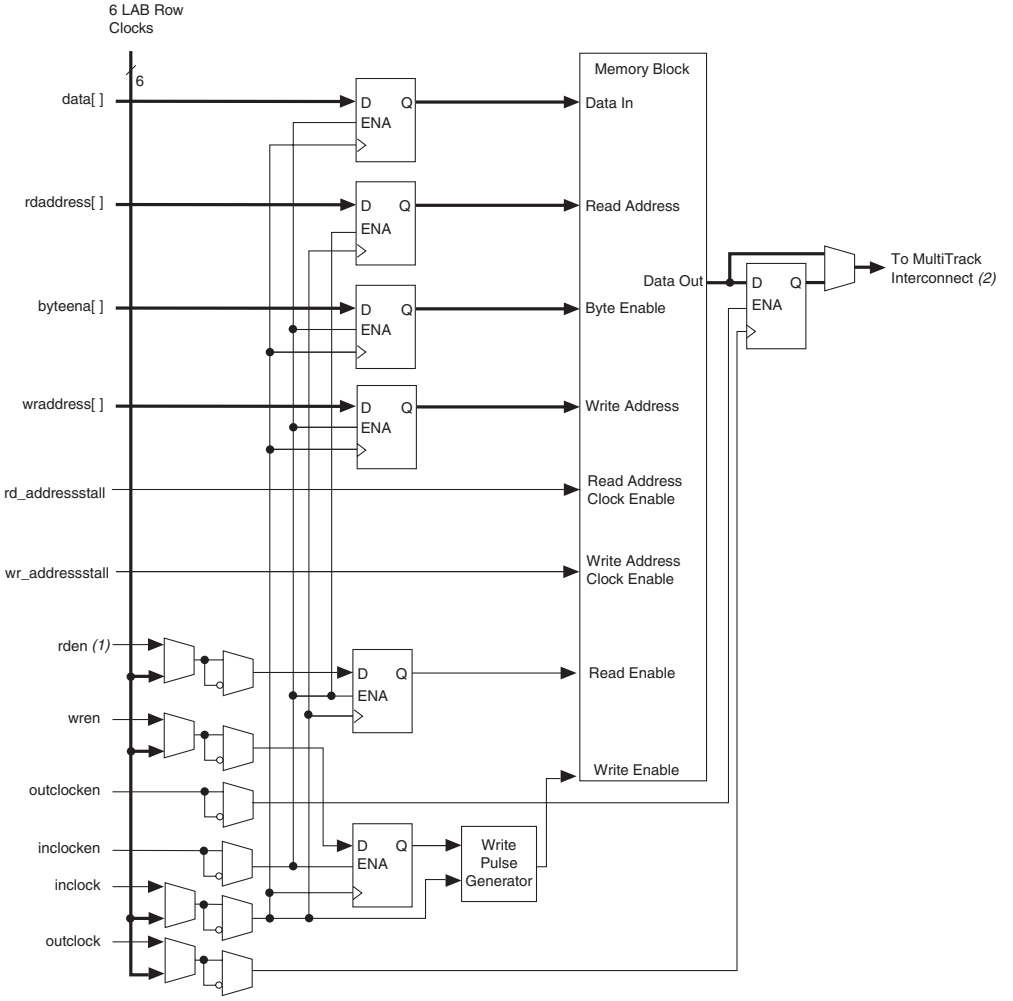
Fully digital systems do not have a separate analog power plane on the board. Since it is expensive to add new planes to the board, you can create islands for VCCA_PLL. Figure 7–16 shows an example board layout with an analog power island. The dielectric boundary that creates the island should be 25 mils thick. Figure 7–16 shows a partitioned plane within V_{CCINT} for VCCA.

Input/Output Clock Mode

Cyclone II memory blocks can implement the input/output clock mode for true and simple dual-port memory. On each of the two ports, A and B, one clock controls all registers for the data, write enable, and address inputs into the memory block. The other clock controls the blocks' data output registers. Each memory block port also supports independent clock enables for input and output registers. Asynchronous clear signals for the registers are not supported.

Figures 8–14 through 8–16 show the memory block in input/output clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

Figure 8–15. Cyclone II Input/Output Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*

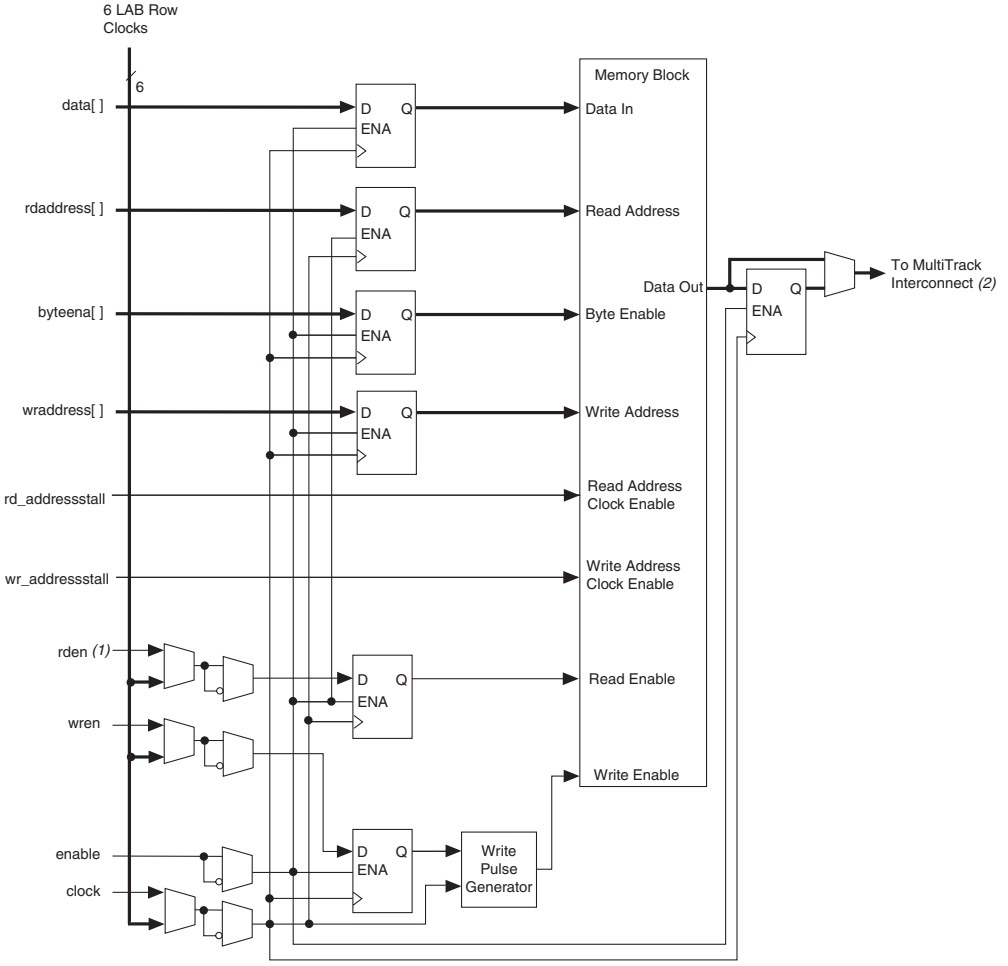


Notes to Figure 8–15:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack™ interconnect.

Figure 8–19. Cyclone II Single-Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*

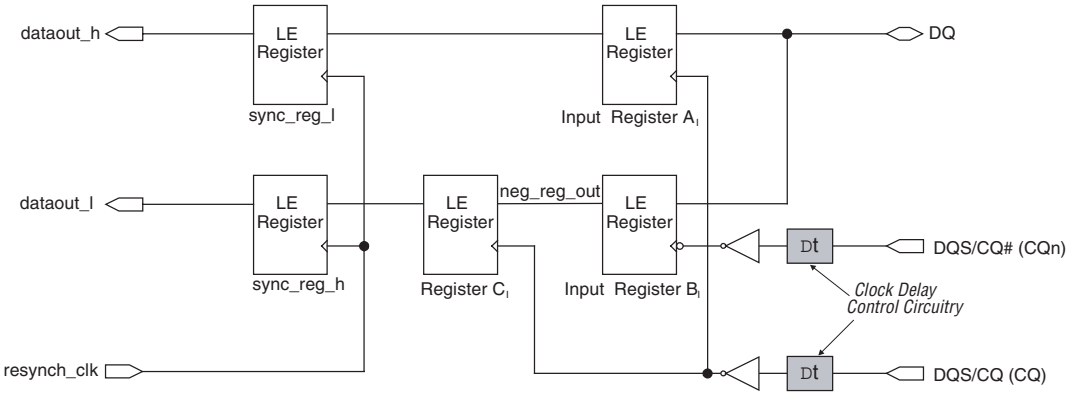


Notes to Figure 8–19:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

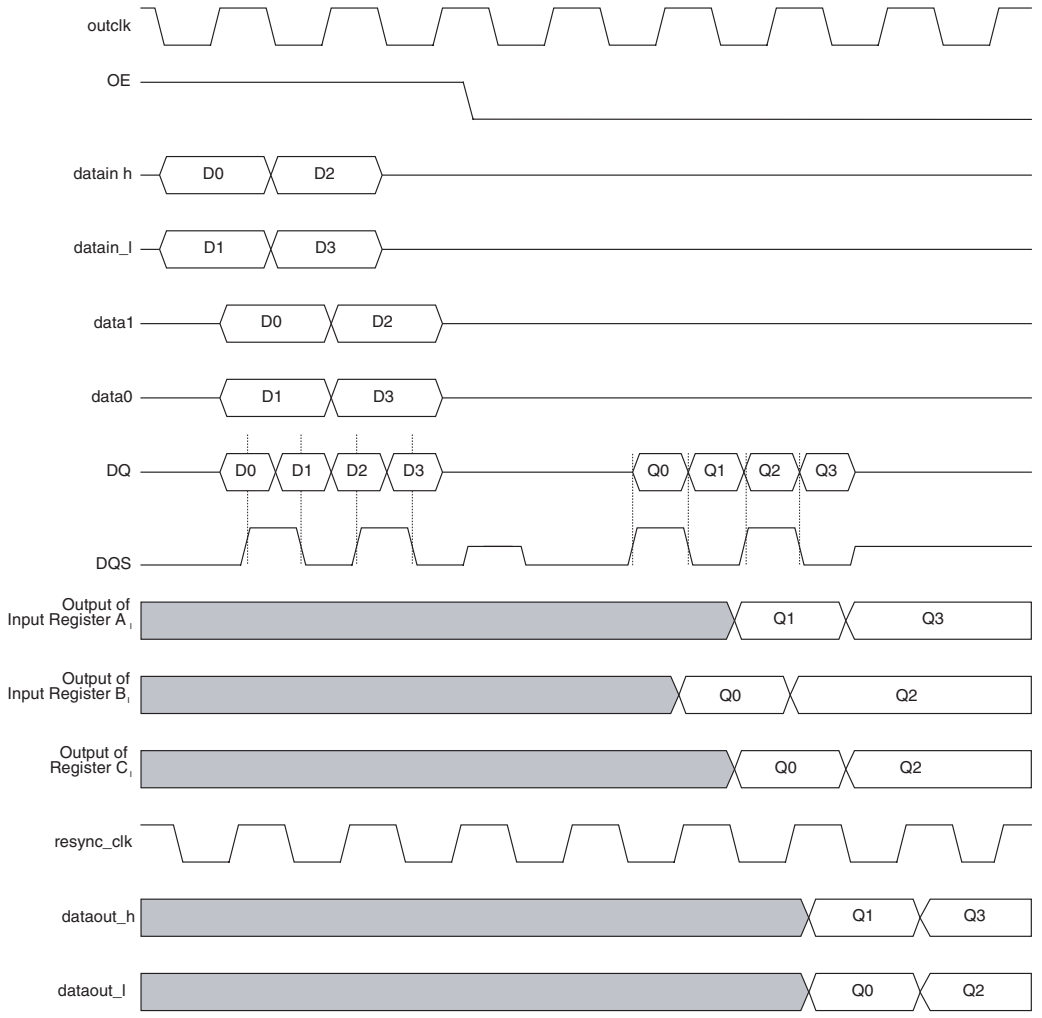
Figure 9–4. CQ & CQn Connection for QDRII SRAM Read



Read & Write Operation

Figure 9–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDRII SRAM devices send data within t_{CO} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. Data is valid until t_{DOH} time after each rising edge of the read clock C or C# in multi-clock mode or the input clock K or K# in single clock mode. The CQ and CQn clocks are edge-aligned with the read data signal. These clocks accompany the read data for data capture in Cyclone II devices.

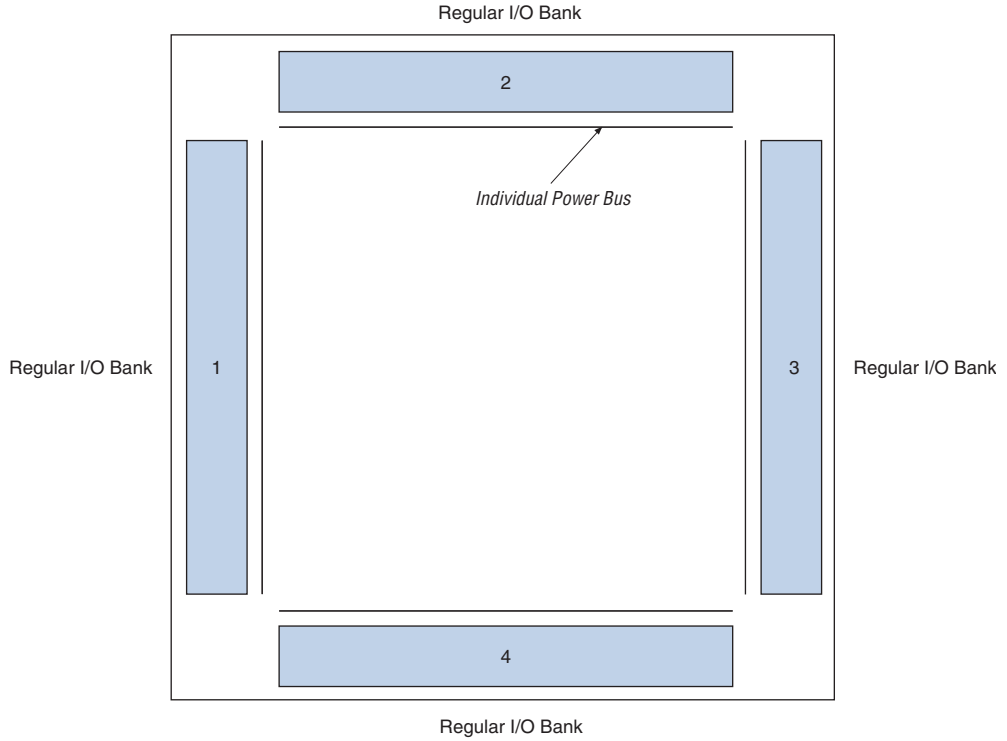
Figure 9–17. DDR Bidirectional Waveforms



Conclusion

Cyclone II devices support SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The clock delay control circuitry allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Figure 10–19. EP2C5 and EP2C8 Device I/O Banks *Notes (1), (2)*



Notes to Figure 10–19:

(1) This is a top view of the silicon die.

(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

November 2005 v2.1	• Updated Tables 10–2 and 10–3. • Added PCI Express information. • Updated Table 10–6.	—
July 2005 v2.0	Updated Table 10–1.	—
November 2004 v1.1	Updated Table 10–7.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Figure 11–12. Differential SSTL Class I Interface

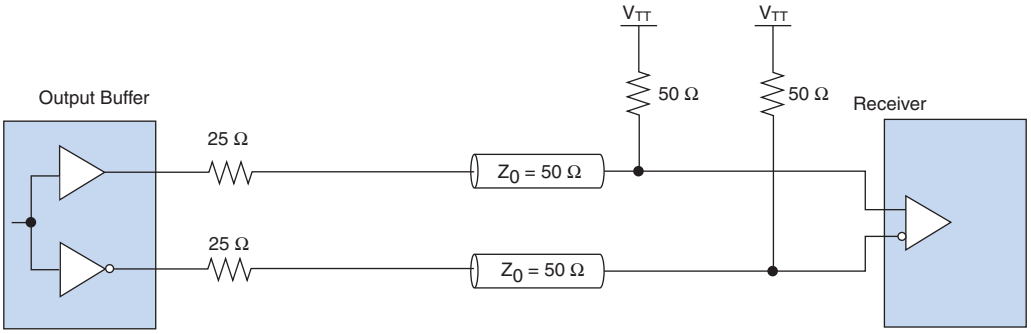
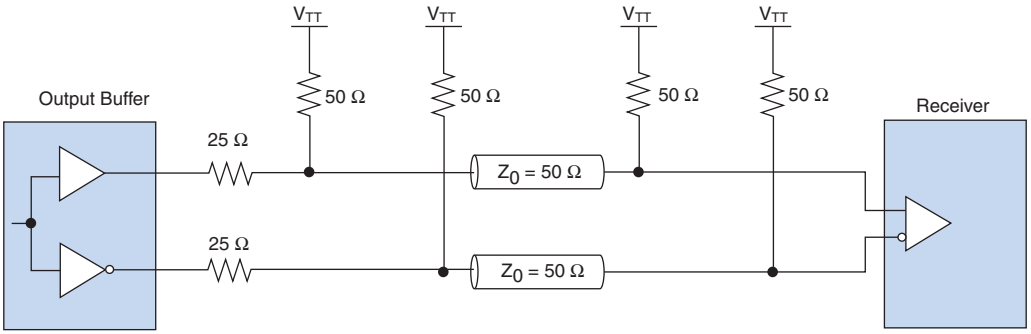


Figure 11–13. Differential SSTL Class II Interface



Differential HSTL Support in Cyclone II Devices

The differential HSTL AC and DC specifications are the same as the HSTL single-ended specifications. The differential HSTL I/O standard is available on the GCLK pins only, treating differential inputs as two single-ended HSTL, and only decoding one of them. The differential HSTL output I/O standard is only supported at the PLLCLKOUT pins using two single-ended HSTL output buffers with the second output programmed as inverted. The standard requires two differential inputs with an external termination voltage (V_{TT}) of 0.5 × V_{CCIO} to which termination resistors are connected.

For the HSTL signaling characteristics, see the *DC Characteristics & Timing Specifications* chapter and the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook.*

Table 11–5 defines the parameters of the timing diagram shown in Figure 11–16. Figure 11–17 shows the Cyclone II high-speed I/O timing budget.

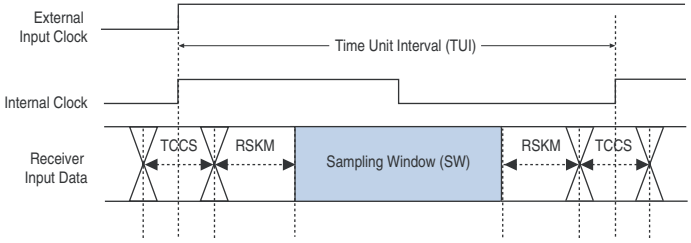
Table 11–5. High-Speed I/O Timing Definitions

Parameter	Symbol	Description
Transmitter channel-to-channel skew *(1)*	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window. $T_{SW} = T_{SU} + T_{hd}$ + PLL jitter.
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: RSKM = (TUI – SW – TCCS) / 2.
Input jitter tolerance (peak-to-peak)		Allowed input jitter on the input clock to the PLL that is tolerable while maintaining PLL lock.
Output jitter (peak-to-peak)		Peak-to-peak output jitter from the PLL.

Note to Table 11–5:

(1) The TCCS specification applies to the entire bank of LVDS as long as the SERDES logic are placed within the LAB adjacent to the output pins.

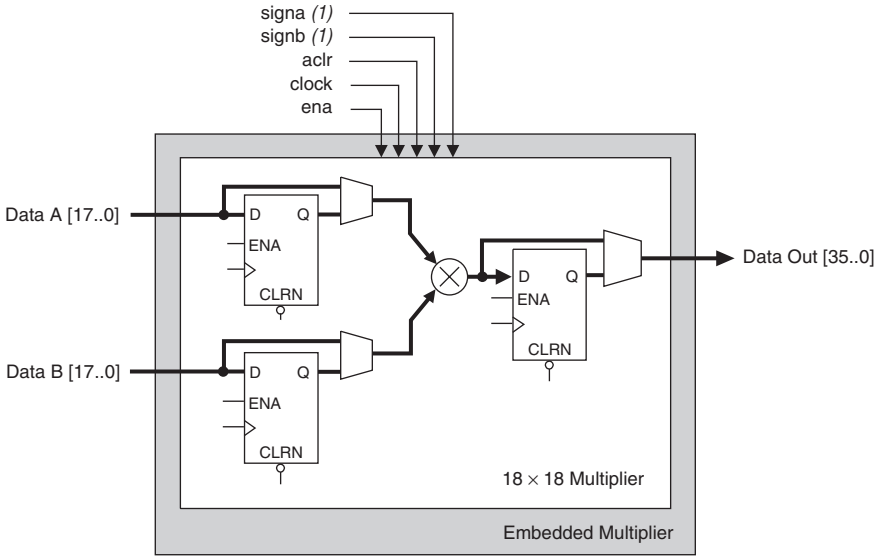
Figure 11–16. High-Speed I/O Timing Diagram



18-Bit Multipliers

Each embedded multiplier can be configured to support a single 18 × 18 multiplier for input widths from 10- to 18-bits. Figure 12–3 shows the embedded multiplier configured to support an 18-bit multiplier.

Figure 12–3. 18-Bit Multiplier Mode



Note to Figure 12–3:
(1) If necessary, you can send these signals through one register to match the data signal path.

All 18-bit multiplier inputs and results can be independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers or a combination of both. Additionally, you can change the `signa` and `signb` signals dynamically and can send these signals through dedicated input registers.

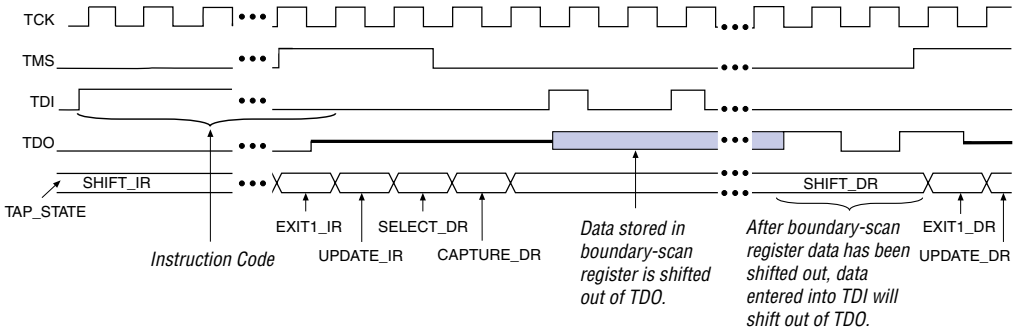
9-Bit Multipliers

Each embedded multiplier can also be configured to support two 9 × 9 independent multipliers for input widths up to 9-bits. Figure 12–4 shows the embedded multiplier configured to support two 9-bit multipliers.

EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the output and output enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data. Thus, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers, then shifted out of TDO during the shift phase. New test data can then be stored in the update registers during the update phase.

The EXTEST waveform diagram in Figure 14–11 resembles the SAMPLE/PRELOAD waveform diagram, except for the instruction code. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

Figure 14–11. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS mode is activated when an instruction code of all 1's is loaded in the instruction register. The waveforms in Figure 14–12 show how scan data passes through a device once the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 15–5 shows a 484-pin FineLine BGA package outline.

Figure 15–5. 484-Pin FineLine BGA Package Outline

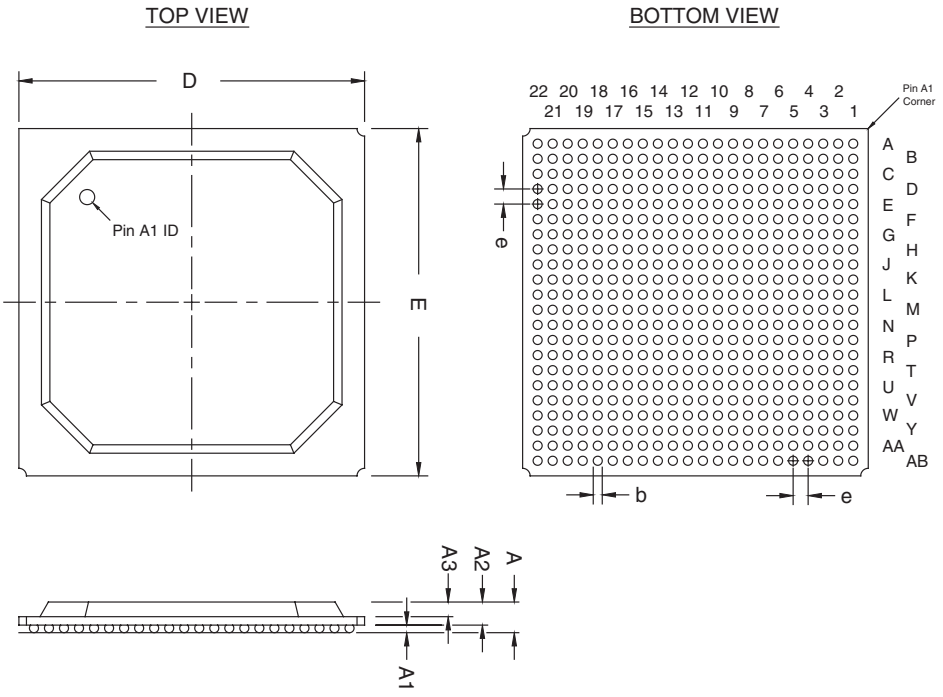


Figure 15–8 shows a 896-pin FineLine BGA package outline.

Figure 15–8. 896-Pin FineLine BGA Package Outline