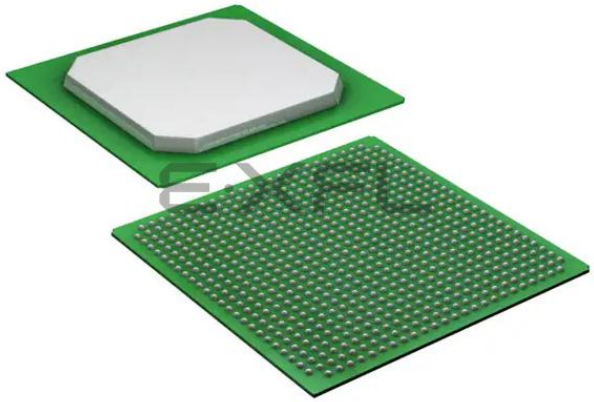

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f672c8

Contents

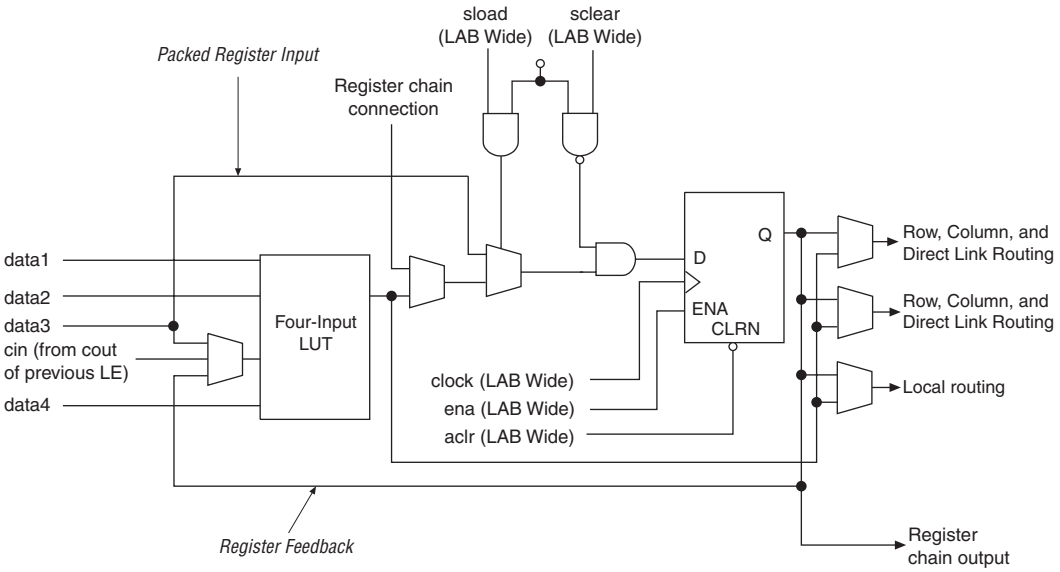
- 133-MHz PCI-X 1.0 specification compatibility
- High-speed external memory support, including DDR, DDR2, and SDR SDRAM, and QDRII SRAM supported by drop in Altera IP MegaCore functions for ease of use
- Three dedicated registers per I/O element (IOE): one input register, one output register, and one output-enable register
- Programmable bus-hold feature
- Programmable output drive strength feature
- Programmable delays from the pin to the IOE or logic array
- I/O bank grouping for unique VCCIO and/or VREF bank settings
- MultiVolt™ I/O standard support for 1.5-, 1.8-, 2.5-, and 3.3-interfaces
- Hot-socketing operation support
- Tri-state with weak pull-up on I/O pins before and during configuration
- Programmable open-drain outputs
- Series on-chip termination support

- Flexible clock management circuitry
  - Hierarchical clock network for up to 402.5-MHz performance
  - Up to four PLLs per device provide clock multiplication and division, phase shifting, programmable duty cycle, and external clock outputs, allowing system-level clock management and skew control
  - Up to 16 global clock lines in the global clock network that drive throughout the entire device

- Device configuration
  - Fast serial configuration allows configuration times less than 100 ms
  - Decompression feature allows for smaller programming file storage and faster configuration times
  - Supports multiple configuration modes: active serial, passive serial, and JTAG-based configuration
  - Supports configuration through low-cost serial configuration devices
  - Device configuration supports multiple voltages (either 3.3, 2.5, or 1.8 V)

- Intellectual property
  - Altera megafunction and Altera MegaCore function support, and Altera Megafunctions Partners Program (AMPP^{SM}) megafunction support, for a wide range of embedded processors, on-chip and off-chip interfaces, peripheral functions, DSP functions, and communications functions and

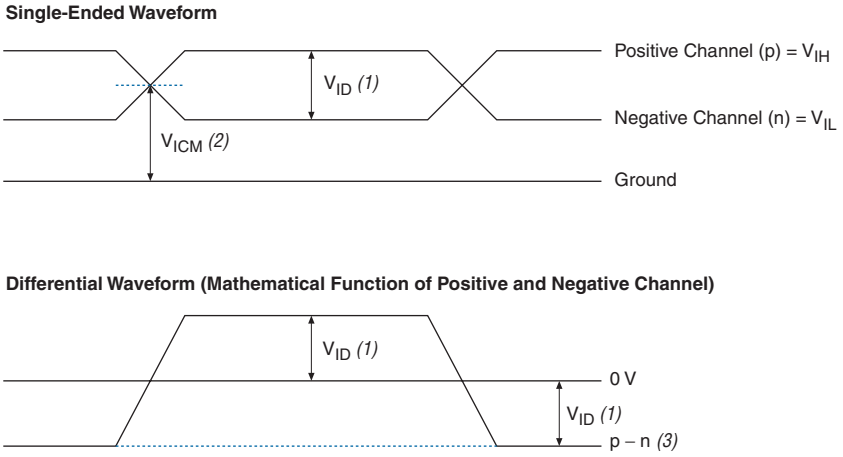
Figure 2–3. LE in Normal Mode



Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, and comparators. An LE in arithmetic mode implements a 2-bit full adder and basic carry chain (see Figure 2–4). LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output. Register feedback and register packing are supported when LEs are used in arithmetic mode.

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards



Notes to Figure 5–1:

(1) V_{ID} is the differential input voltage. $V_{ID} = |p - n|$.

(2) V_{ICM} is the input common mode voltage. $V_{ICM} = (p + n)/2$.

(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–11 specifies the bus hold parameters for general I/O pins.

Table 5–11. Bus Hold Parameters *Note (1)*

Parameter	Conditions	V_{CCIO} Level						Unit
		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$(maximum)	30	—	50	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IL}$(minimum)	–30	—	–50	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	200	—	300	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–200	—	–300	—	–500	µA
Bus-hold trip point *(2)*	—	0.68	1.07	0.7	1.7	0.8	2.0	V

Notes to Table 5–11:
(1) There is no specification for bus-hold at V_{CCIO} = 1.5 V for the HSTL I/O standard.
(2) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination Specifications

Table 5–12 defines the specifications for internal termination resistance tolerance when using series or differential on-chip termination.

Table 5–12. Series On-Chip Termination Specifications

Symbol	Description	Conditions	Resistance Tolerance			
			Commercial Max	Industrial Max	Extended/ Automotive Temp Max	Unit
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3V	±30	±30	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 2.5V	±30	±30	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8V	±30 *(1)*	±40	±50	%

Note to Table 5–12:
(1) For commercial –8 devices, the tolerance is ±40%.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 5–14. Cyclone II Device Timing Model Status

Device	Speed Grade	Preliminary	Final
EP2C5/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C8/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C15A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C20/A	Commercial/Industrial	—	✓
	Automotive	✓	—
EP2C35	Commercial/Industrial	—	✓
EP2C50	Commercial/Industrial	—	✓
EP2C70	Commercial/Industrial	—	✓

Performance

Table 5–15 shows Cyclone II performance for some common designs. All performance values were obtained with Quartus II software compilation of LPM, or MegaCore functions for the FIR and FFT designs.

Table 5–15. Cyclone II Performance (Part 1 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
LE	16-to-1 multiplexer *(1)*	21	0	0	385.35	313.97	270.85	286.04
	32-to-1 multiplexer *(1)*	38	0	0	294.2	260.75	228.78	191.02
	16-bit counter	16	0	0	401.6	349.4	310.65	310.65
	64-bit counter	64	0	0	157.15	137.98	126.08	126.27

Table 5–47. High-Speed I/O Timing Definitions (Part 2 of 2)

Parameter	Symbol	Description
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. Sampling window is the sum of the setup time, hold time, and jitter. The window of t_{SU} + t_H is expected to be centered in the sampling window. SW = TUI – TCCS – (2 × RSKM)
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2
Input jitter (peak to peak)	—	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak to peak)	—	Peak-to-peak output jitter on high-speed PLLs.
Signal rise time	t_{RISE}	Low-to-high transmission time.
Signal fall time	t_{FALL}	High-to-low transmission time.
Lock time	t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Figure 5–3. High-Speed I/O Timing Diagram

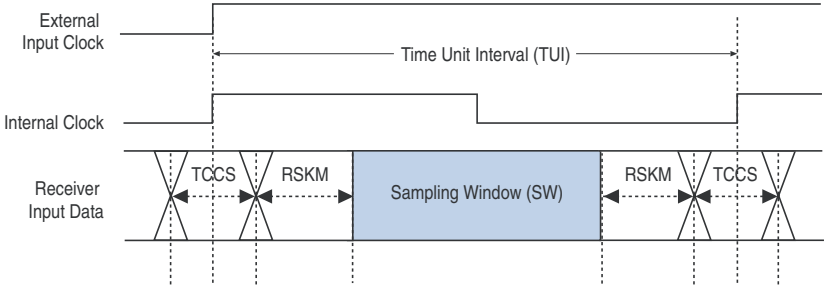


Figure 5–4 shows the high-speed I/O timing budget.

PLL Specifications

See the *DC & Switching Characteristics* chapter in Volume 1 of the *Cyclone II Device Handbook* for information on PLL timing specifications.

Clocking

Cyclone II devices provide up to 16 dedicated clock pins (`CLK[15..0]`) that can drive the global clock networks. The smaller Cyclone II devices (EP2C5 and EP2C8 devices) support four dedicated clock pins on each side (left and right) capable of driving a total of eight global clock networks, while the larger devices (EP2C15 devices and larger) support four clock pins on all four sides of the device. These clock pins can drive a total of 16 global clock networks.

Table 7–7 shows the number of global clocks available across the Cyclone II family members.

Table 7–7. Number of Global Clocks Available in Cyclone II Devices

Device	Number of Global Clocks
EP2C5	8
EP2C8	8
EP2C15	16
EP2C20	16
EP2C35	16
EP2C50	16
EP2C70	16

Global Clock Network

Global clocks drive throughout the entire device, feeding all device quadrants. All resources within the device (IOEs, logic array blocks (LABs), dedicated multiplier blocks, and M4K memory blocks) can use the global clock networks as clock sources. These clock network resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed by an external pin. Internal logic can also drive the global clock networks for internally generated global clocks and asynchronous clears, clock enables, or other control signals with high fan-out.

8. Cyclone II Memory Blocks

CII51008-2.4

Introduction

Cyclone® II devices feature embedded memory structures to address the on-chip memory needs of FPGA designs. The embedded memory structure consists of columns of M4K memory blocks that can be configured to provide various memory functions such as RAM, first-in first-out (FIFO) buffers, and ROM. M4K memory blocks provide over 1 Mbit of RAM at up to 250-MHz operation (see Table 8–2 on page 8–2 for total RAM bits per density).

Overview

The M4K blocks support the following features:

- Over 1 Mbit of RAM available without reducing available logic
- 4,096 memory bits per block (4,608 bits per block including parity)
- Variable port configurations
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Initialization file to pre-load content of memory in RAM and ROM modes
- Up to 250-MHz operation

Table 8–1 summarizes the features supported by the M4K memory.

Table 8–1. Summary of M4K Memory Features (Part 1 of 2)

Feature	M4K Blocks
Maximum performance *(1)*	250 MHz
Total RAM bits (including parity bits)	4,608
Configurations	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36
Parity bits	✓
Byte enable	✓

Phase Lock Loop (PLL)

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two outputs is needed to generate the system clock and the write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock shifts by –90° from the system clock and generates the DQ signals during writes.

Clock Delay Control

Clock delay control circuit on each DQS pin allows a phase shift that center-aligns the incoming DQS signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal then clocks the DQ signals on internal LE registers. The clock delay control circuitry is used during the read operations where the DQS signals are acting as input clocks or strobes.

Figure 9–8 illustrates DDR SDRAM interfacing from the I/O pins through the dedicated circuitry to the logic array.

Figure 9–8. DDR SDRAM Interfacing

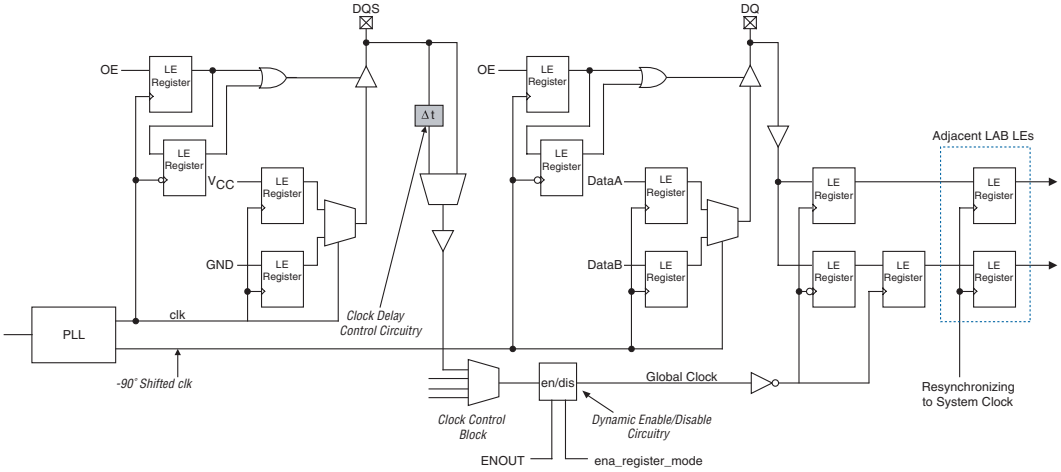
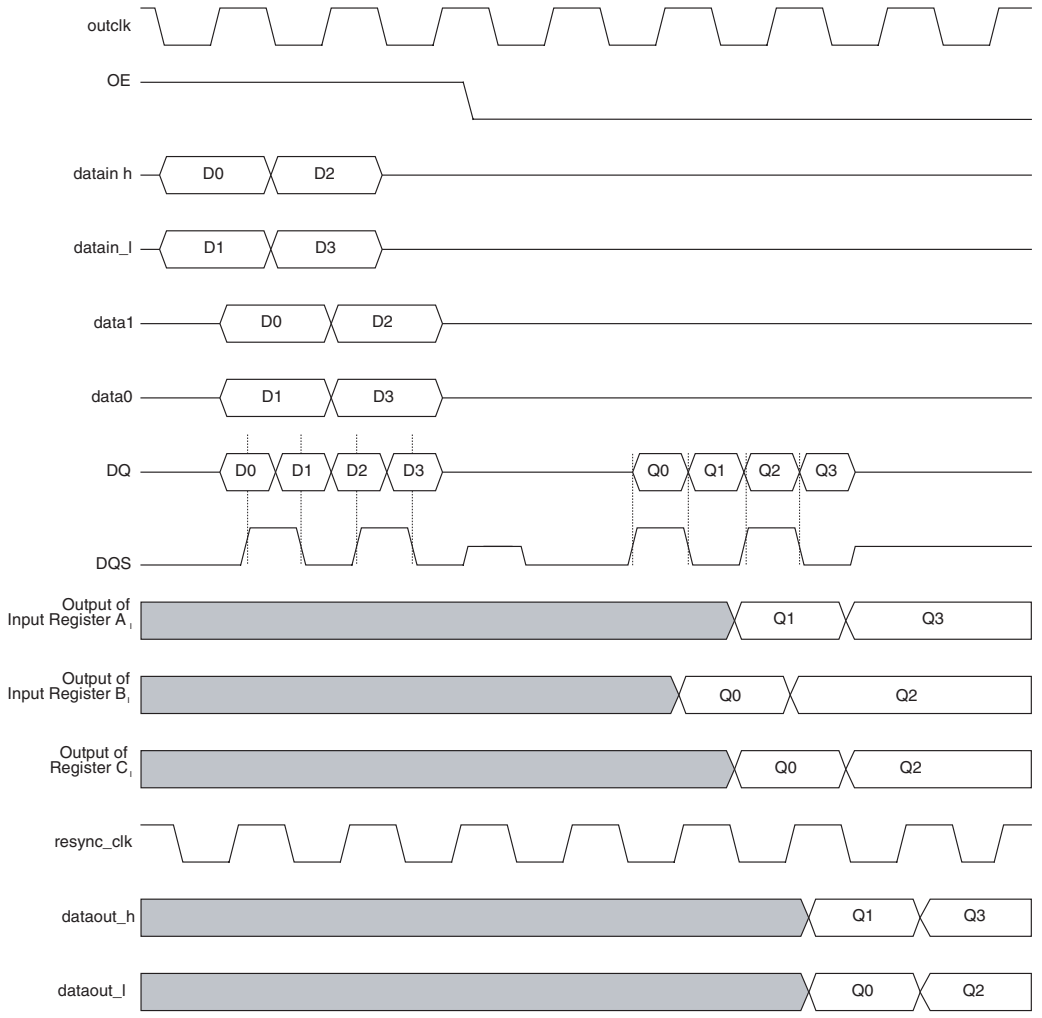


Figure 9–1 on page 9–4 shows an example where the DQS signal is shifted by 90°. The DQS signal goes through the 90° shift delay set by the clock delay control circuitry and global clock routing delay from the clock delay control circuitry to the DQ LE registers. The DQ signals only goes through routing delays from the DQ pin to the DQ LE registers. The delay from

Figure 9–17. DDR Bidirectional Waveforms



Conclusion

Cyclone II devices support SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The clock delay control circuitry allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Additionally, each Cyclone II I/O bank has its own VCCIO pins. Any single I/O bank can only support one V_{CCIO} setting from among 1.5, 1.8, 2.5 or 3.3 V. Although there can only be one V_{CCIO} voltage per I/O bank, Cyclone II devices permit additional input signaling capabilities, as shown in Table 10–4.

Table 10–4. Acceptable Input Levels for LVTTL and LVCMOS

Bank V_{CCIO} (V)	Acceptable Input Levels (V)			
	3.3	2.5	1.8	1.5
3.3	✓	✓ (1)		
2.5	✓	✓		
1.8	✓ (2)	✓ (2)	✓	✓ (1)
1.5	✓ (2)	✓ (2)	✓	✓

Notes to Table 10–4:

(1) Because the input level does not drive to the rail, the input buffer does not completely shut off, and the I/O current is slightly higher than the default value.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on **Allow voltage overdrive for LVTTL/LVCMOS input pins** in Settings > Device > Device and Pin Options > Pin Placement tab. This setting allows input pins with LVTTL or LVCMOS I/O standards to be placed by the Quartus II software in an I/O bank with a lower V_{CCIO} voltage than the voltage specified by the pins.

Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank as long as they use compatible V_{CCIO} levels for input and output pins. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V LVTTL inputs and outputs, 2.5-V LVDS-compatible inputs and outputs, and 3.3-V LVCMOS inputs only.

Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value. For example, if you choose to implement both SSTL-2 and SSTL-18 in your Cyclone II device, I/O pins using these standards—because they require different V_{REF} values—must be in different banks from each other. However, the same I/O bank can support SSTL-2 and 2.5-V LVCMOS with the V_{CCIO} set to 2.5 V and the V_{REF} set to 1.25 V.

Refer to "Pad Placement and DC Guidelines" on page 10–27 for more information.

RSDS I/O Standard Support in Cyclone II Devices

The RSDS specification is used in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the National Semiconductor Corporation RSDS Interface Specification and support the RSDS output standard. Table 11–2 shows the RSDS electrical characteristics for Cyclone II devices.

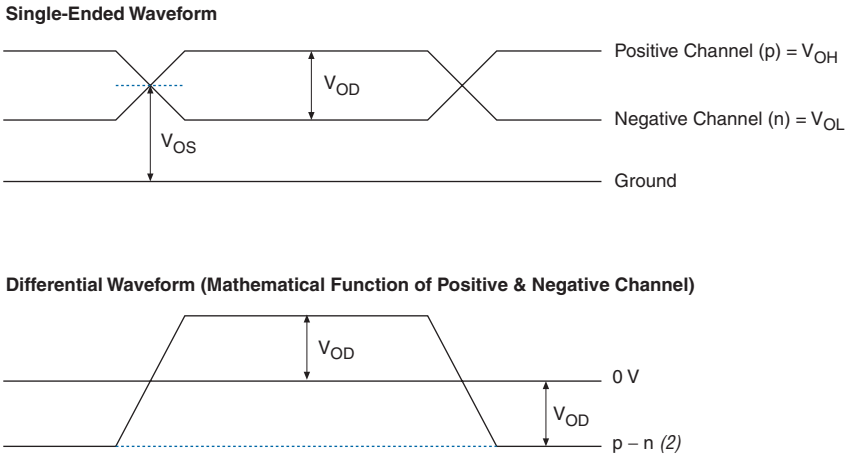
Table 11–2. RSDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	100		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
T_r/T_f	Transition time	20% to 80%		500		ps

Notes to Table 11–2:
(1) The specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

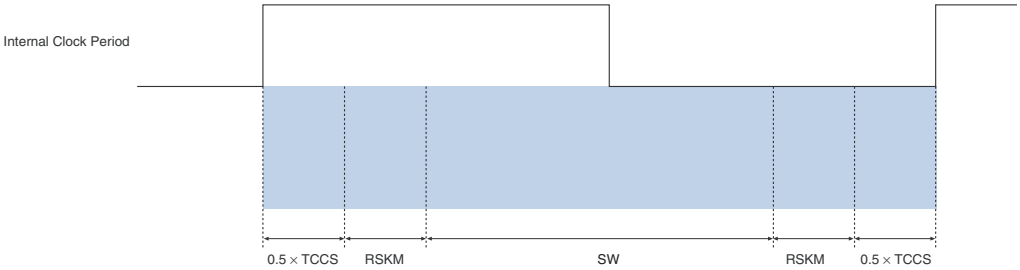
Figure 11–6 shows the RSDS transmitter output signal waveforms.

Figure 11–6. Transmitter Output Signal Level Waveforms for RSDS *Note (1)*



Notes to Figure 11–6:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 11–17. Cyclone II High-Speed I/O Timing Budget *Note (1)*



Note to Figure 11–17:
(1) The equation for the high-speed I/O timing budget is: Period = 0.5/TCCS + RSKM + SW + RSKM + 0.5/TCCS.

Design Guidelines

This section provides guidelines for designing with Cyclone II devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pins in relation to differential pads.

See the guidelines in the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook* for placing single-ended pads with respect to differential pads in Cyclone II devices.

Board Design Considerations

This section explains how to get the optimal performance from the Cyclone II I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. The critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques must be considered to get the best performance from the IC. The Cyclone II device generates signals that travel over the media at frequencies as high as 805 Mbps. Use the following general guidelines for improved signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.

All information in the "Single Device PS Configuration Using a MAX II Device as an External Host" on page 13–22 section is also applicable when using a microprocessor as an external host. Refer to that section for all configuration information.

The MicroBlaster™ software driver allows you to configure Altera FPGAs, including Cyclone II devices, through the ByteBlaster II or ByteBlasterMV cable in PS mode. The MicroBlaster software driver supports a RBF programming input file and is targeted for embedded PS configuration. The source code is developed for the Windows NT operating system, although you can customize it to run on other operating systems.

Since the Cyclone II device can decompress the compressed configuration data on-the-fly during PS configuration, the MicroBlaster software can accept a compressed RBF file as its input file.

For more information on the MicroBlaster software driver, see the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* and source files on the Altera web site at **www.altera.com**.

If you turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software, the Cyclone II devices does not enter user mode after the MicroBlaster has transmitted all the configuration data in the RBF file. You need to supply enough initialization clock cycles to `CLKUSR` pin to enter user mode.

Single Device PS Configuration Using a Configuration Device

You can use an Altera configuration device (for example, an EPC2, EPC1, or enhanced configuration device) to configure Cyclone II devices using a serial configuration bitstream. Configuration data is stored in the configuration device. Figure 13–13 shows the configuration interface connections between the Cyclone II device and a configuration device.

The figures in this chapter only show the configuration-related pins and the configuration pin connections between the configuration device and the FPGA.

For more information on enhanced configuration devices and flash interface pins (e.g., `PGM[2..0]`, `EXCLK`, `PORSEL`, `A[20..0]`, and `DQ[15..0]`), see the *Enhanced Configuration Devices (EPC4, EPC8 & EPC16) Data Sheet*.

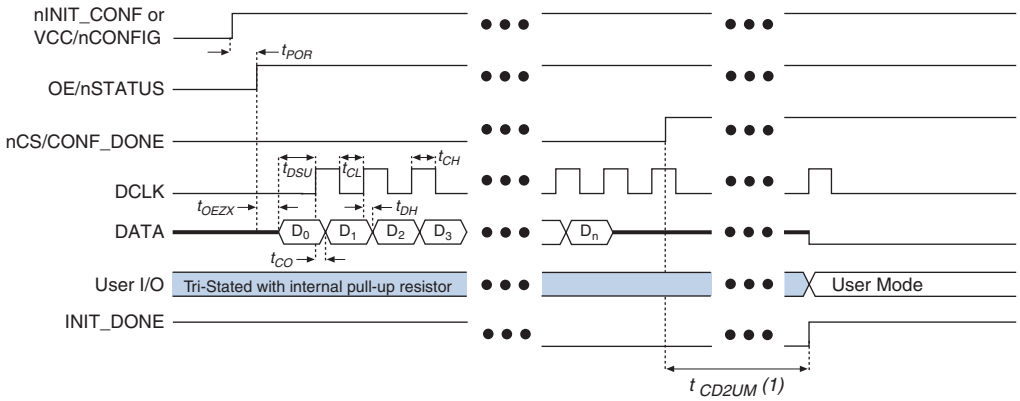
You can use a single configuration chain to configure Cyclone II devices with other Altera devices. To ensure that all devices in the chain complete configuration at the same time or that an error flagged by one device initiates reconfiguration in all devices, connect all the Cyclone II device CONF_DONE pins and connect all Cyclone II device nSTATUS pins together.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

During PS configuration, the design must meet the setup and hold timing parameters and maximum DCLK frequency. The enhanced configuration and EPC2 devices are designed to meet these interface timing specifications.

Figure 13–18 shows the timing waveform for the PS configuration scheme using a configuration device.

Figure 13–18. Cyclone II PS Configuration Using a Configuration Device Timing Waveform



Note to Figure 13–18:

(1) Cyclone II devices enter user mode 299 clock cycles after CONF_DONE goes high. The initialization clock can come from the Cyclone II internal oscillator or the CLKUSR pin.

For timing information, refer to the *Enhanced Configuration Devices (EPC4, EPC8, and EPC16) Data Sheet* or the *Configuration Devices for SRAM-based LUT Devices Data Sheet* in the *Configuration Handbook*.

For more information on device configuration options and how to create configuration files, see the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

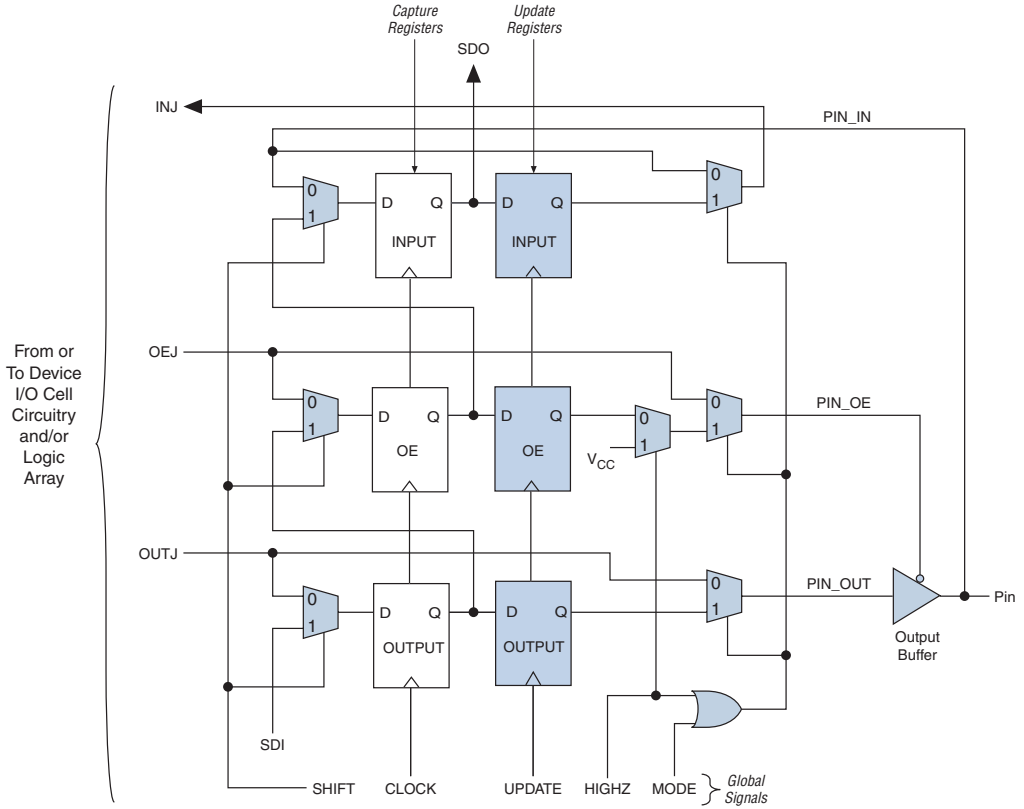
Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 2 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nSTATUS	N/A	All	Bidirectional open-drain	The Cyclone II device drives nSTATUS low immediately after power-up and releases it after the POR time. This pin provides a status output and input for the Cyclone II device. If the Cyclone II device detects an error during configuration, it drives the nSTATUS pin low to stop configuration. If an external source (for example, another Cyclone II device) drives the nSTATUS pin low during configuration or initialization, the target device enters an error state. Driving nSTATUS low after configuration and initialization does not affect the configured device. If your design uses a configuration device, driving nSTATUS low causes the configuration device to attempt to configure the FPGA, but since the FPGA ignores transitions on nSTATUS in user mode, the FPGA does not reconfigure. To initiate a reconfiguration, pull the nCONFIG pin low. The enhanced configuration devices' and EPC2 devices' OE and nCS pins are connected to the Cyclone II device's nSTATUS and CONF_DONE pins, respectively, and have optional internal programmable pull-up resistors. If you use these internal pull-up resistors on the enhanced configuration device, do not use external 10-kΩ pull-up resistors on these pins. When using EPC2 devices, you should only use external 10-kΩ pull-up resistors. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.

to external device data via the PIN_IN signal, while the update registers connect to external data through the PIN_OUT and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 14–4 shows the Cyclone II device's user I/O boundary-scan cell.

Figure 14–4. Cyclone II Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry



Section VII. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. The chapters in this section contain the required PCB layout guidelines and package specifications.

This section includes the following chapters:

- Chapter 15, Package Information for Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

256-Pin FineLine Ball-Grid Array, Option 2 – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on the package surface.

This POD is applicable to the F256 package of the Cyclone II product only.

Tables 15–11 and 15–12 show the package information and package outline figure references, respectively, for the 256-pin FineLine BGA package.

Table 15–11. 256-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MO-192 Variation: AAF-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	1.9 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–12. 256-Pin FineLine BGA Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	1.55
A1	0.25	–	–
A2	1.05 REF		
A3	–	–	0.80
D	17.00 BSC		
E	17.00 BSC		
b	0.40	0.50	0.55
e	1.00 BSC		