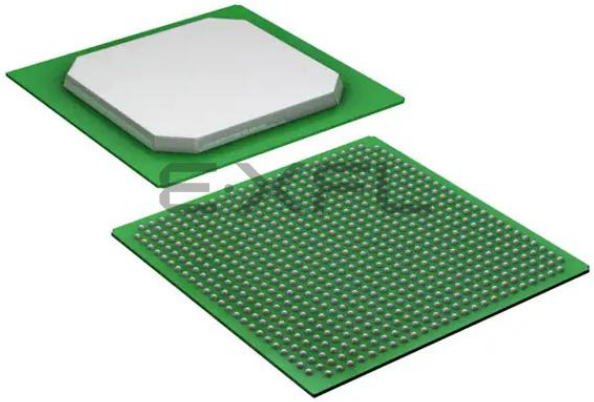

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Applications of Embedded - FPGAs

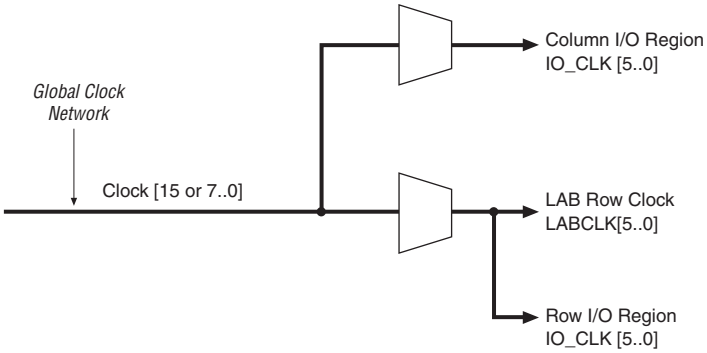
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	450
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50f672i8n

Global Clock Network Distribution

Cyclone II devices contains 16 global clock networks. The device uses multiplexers with these clocks to form six-bit buses to drive column IOE clocks, LAB row clocks, or row IOE clocks (see Figure 2–14). Another multiplexer at the LAB level selects two of the six LAB row clocks to feed the LE registers within the LAB.

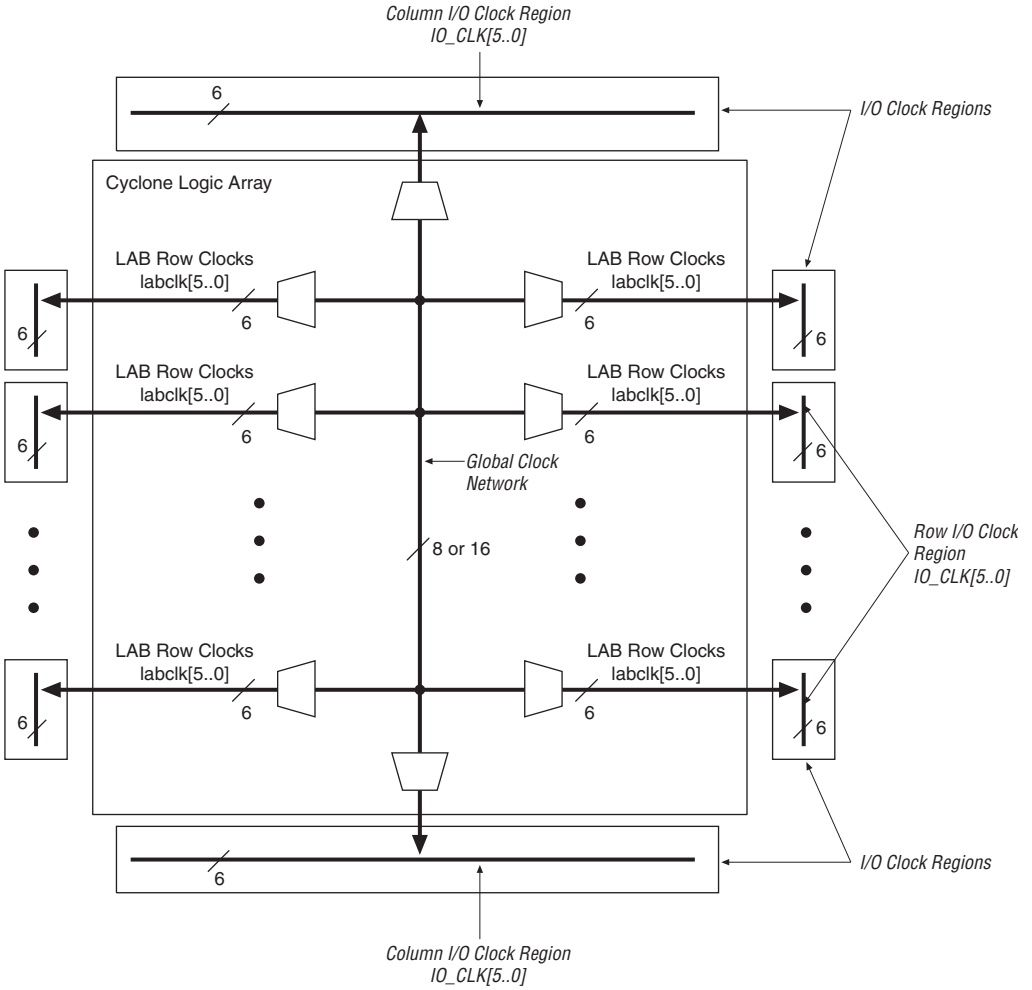
Figure 2–14. Global Clock Network Multiplexers



LAB row clocks can feed LEs, M4K memory blocks, and embedded multipliers. The LAB row clocks also extend to the row I/O clock regions.

IOE clocks are associated with row or column block regions. Only six global clock resources feed to these row and column regions. Figure 2–15 shows the I/O clock regions.

Figure 2–15. LAB & I/O Clock Regions



For more information on the global clock network and the clock control block, see the *PLLs in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Table 5–7. DC Characteristics of User I/O Pins Using Single-Ended Standards Notes (1), (2) **(Part 2 of 2)**

I/O Standard	Test Conditions		Voltage Thresholds	
	I_{OL} (mA)	I_{OH} (mA)	Maximum V_{OL} (V)	Minimum V_{OH} (V)
1.5-V HSTL class I	8	–8	0.4	V_{CCIO} – 0.4
1.5V HSTL class II	16	–16	0.4	V_{CCIO} – 0.4

Notes to Table 5–7:

(1) The values in this table are based on the conditions listed in Tables 5–2 and 5–6.

(2) This specification is supported across all the programmable drive settings available as shown in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

Differential I/O Standards

The RSDS and mini-LVDS I/O standards are only supported on output pins. The LVDS I/O standard is supported on both receiver input pins and transmitter output pins.

For more information on how these differential I/O standards are implemented, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook*.

Figure 5–1 shows the receiver input waveforms for all differential I/O standards (LVDS, LVPECL, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Table 5–8 shows the recommended operating conditions for user I/O pins with differential I/O standards.

Table 5–8. Recommended Operating Conditions for User I/O Pins Using Differential Signal I/O Standards

I/O Standard	V_{CCIO} (V)			V_{ID} (V) *(1)*			V_{ICM} (V)			V_{IL} (V)		V_{IH} (V)	
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	2.375	2.5	2.625	0.1	—	0.65	0.1	—	2.0	—	—	—	—
Mini-LVDS *(2)*	2.375	2.5	2.625	—	—	—	—	—	—	—	—	—	—
RSDS *(2)*	2.375	2.5	2.625	—	—	—	—	—	—	—	—	—	—
LVPECL *(3) (6)*	3.135	3.3	3.465	0.1	0.6	0.95	—	—	—	0	2.2	2.1	2.88
Differential 1.5-V HSTL class I and II *(4)*	1.425	1.5	1.575	0.2	—	V_{CCIO} + 0.6	0.68	—	0.9	—	V_{REF} – 0.20	V_{REF} + 0.20	—
Differential 1.8-V HSTL class I and II *(4)*	1.71	1.8	1.89	—	—	—	—	—	—	—	V_{REF} – 0.20	V_{REF} + 0.20	—
Differential SSTL-2 class I and II *(5)*	2.375	2.5	2.625	0.36	—	V_{CCIO} + 0.6	0.5 × V_{CCIO} – 0.2	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.2	—	V_{REF} – 0.35	V_{REF} + 0.35	—
Differential SSTL-18 class I and II *(5)*	1.7	1.8	1.9	0.25	—	V_{CCIO} + 0.6	0.5 × V_{CCIO} – 0.2	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.2	—	V_{REF} – 0.25	V_{REF} + 0.25	—

Notes to Table 5–8:

(1) Refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook* for measurement conditions on V_{ID}.

(2) The RSDS and mini-LVDS I/O standards are only supported on output pins.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(4) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

(5) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(6) The LVPECL clock inputs are powered by V_{CCINT} and support all V_{CCIO} settings. However, it is recommended to connect V_{CCIO} to typical value of 3.3V.

Table 5–16. LE_FF Internal Timing Microparameters (Part 2 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TPRE	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps
TCLKL	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
TCLKH	1000	—	1242	—	1242	—	ps
	—	—	1111	—	1242	—	ps
tLUT	180	438	172	545	172	651	ps
	—	—	180	—	180	—	ps

Notes to Table 5–16:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Table 5–17. IOE Internal Timing Microparameters (Part 1 of 2)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TSU	76	—	101	—	101	—	ps
	—	—	89	—	101	—	ps
TH	88	—	106	—	106	—	ps
	—	—	97	—	106	—	ps
TCO	99	155	95	171	95	187	ps
	—	—	99	—	99	—	ps
TPIN2COMBOUT_R	384	762	366	784	366	855	ps
	—	—	384	—	384	—	ps
TPIN2COMBOUT_C	385	760	367	783	367	854	ps
	—	—	385	—	385	—	ps
TCOMBIN2PIN_R	1344	2490	1280	2689	1280	2887	ps
	—	—	1344	—	1344	—	ps

Table 5–19. M4K Block Internal Timing Microparameters (Part 2 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KBEH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATAASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATAAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KADDRASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KADDRAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATABSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATABH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KRADDRBSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KRADDRBH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATACO1	466	724	445	826	445	930	ps
	—	—	466	—	466	—	ps
TM4KDATACO2	2345	3680	2234	4157	2234	4636	ps
	—	—	2345	—	2345	—	ps
TM4KCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TM4KCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

IOE Programmable Delay

Refer to Table 5–36 and 5–37 for IOE programmable delay.

Table 5–36. Cyclone II IOE Programmable Delay on Column Pins *Notes (1), (2)*

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad -> I/O dataout to core	7	0	2233	0	3827	0	4232	0	4349	ps
			0	2344	—	—	0	4088	—	—	ps
Input Delay from Pin to Input Register	Pad -> I/O input register	8	0	2656	0	4555	0	4914	0	4940	ps
			0	2788	—	—	0	4748	—	—	ps
Delay from Output Register to Output Pin	I/O output register -> Pad	2	0	303	0	563	0	638	0	670	ps
			0	318	—	—	0	617	—	—	ps

Notes to Table 5–36:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.

(3) The value in the first row for each parameter represents the fast corner timing parameter for industrial and automotive devices. The second row represents the fast corner timing parameter for commercial devices.

(4) The value in the first row is for automotive devices. The second row is for commercial devices.

Table 5–37. Cyclone II IOE Programmable Delay on Row Pins *Notes (1), (2)* ***(Part 1 of 2)***

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade (4)		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad -> I/O dataout to core	7	0	2240	0	3776	0	4174	0	4290	ps
			0	2352	—	—	0	4033	—	—	ps

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 4 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.5V_ DIFFERENTIAL_HSTL _CLASS_I	8 mA	210	170	140	210	170	140	210	170	140
	10 mA	220	180	150	—	—	—	—	—	—
	12 mA	230	190	160	—	—	—	—	—	—
1.5V_ DIFFERENTIAL_HSTL _CLASS_II	16 mA	210	170	140	—	—	—	—	—	—
LVDS	—	400	340	280	400	340	280	400	340	280
RSDS	—	400	340	280	400	340	280	400	340	280
MINI_LVDS	—	400	340	280	400	340	280	400	340	280
SIMPLE_RSDS	—	380	320	260	380	320	260	380	320	260
1.2V_HSTL	—	80	80	80	—	—	—	—	—	—
1.2V_ DIFFERENTIAL_HSTL	—	80	80	80	—	—	—	—	—	—
PCI	—	—	—	—	350	315	280	350	315	280
PCI-X	—	—	—	—	350	315	280	350	315	280
LVTTL	OCT_25_ OHMS	360	300	250	360	300	250	360	300	250
LVCMOS	OCT_25_ OHMS	360	300	250	360	300	250	360	300	250
2.5V	OCT_50_ OHMS	240	200	160	240	200	160	240	200	160
1.8V	OCT_50_ OHMS	290	240	200	290	240	200	290	240	200
SSTL_2_CLASS_I	OCT_50_ OHMS	240	200	160	240	200	160	—	—	—
SSTL_18_CLASS_I	OCT_50_ OHMS	290	240	200	290	240	200	—	—	—

Note to Table 5–45:
(1) This is based on single data rate I/Os.

Table 5–51. LVDS Receiver Timing Specification

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×8	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×7	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×4	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×2	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×1	10	—	402.5	10	—	402.5	10	—	402.5 *(3)*	MHz
HSIODR	×10	100	—	805	100	—	640	100	—	640 *(2)*	Mbps
	×8	80	—	805	80	—	640	80	—	640 *(2)*	Mbps
	×7	70	—	805	70	—	640	70	—	640 *(2)*	Mbps
	×4	40	—	805	40	—	640	40	—	640 *(2)*	Mbps
	×2	20	—	805	20	—	640	20	—	640 *(2)*	Mbps
	×1	10	—	402.5	10	—	402.5	10	—	402.5 *(4)*	Mbps
SW	—	—	—	300	—	—	400	—	—	400	ps
Input jitter tolerance	—	—	—	500	—	—	500	—	—	550	ps
t_{LOCK}	—	—	—	100	—	—	100	—	—	100 *(5)*	ps

Notes to Table 5–51:
(1) For extended temperature devices, the maximum input clock frequency for x10 through x2 modes is 275 MHz.
(2) For extended temperature devices, the maximum data rate for x10 through x2 modes is 550 Mbps.
(3) For extended temperature devices, the maximum input clock frequency for x1 mode is 340 MHz.
(4) For extended temperature devices, the maximum data rate for x1 mode is 340 Mbps.
(5) For extended temperature devices, the maximum lock time is 500 us.

External Memory Interface Specifications

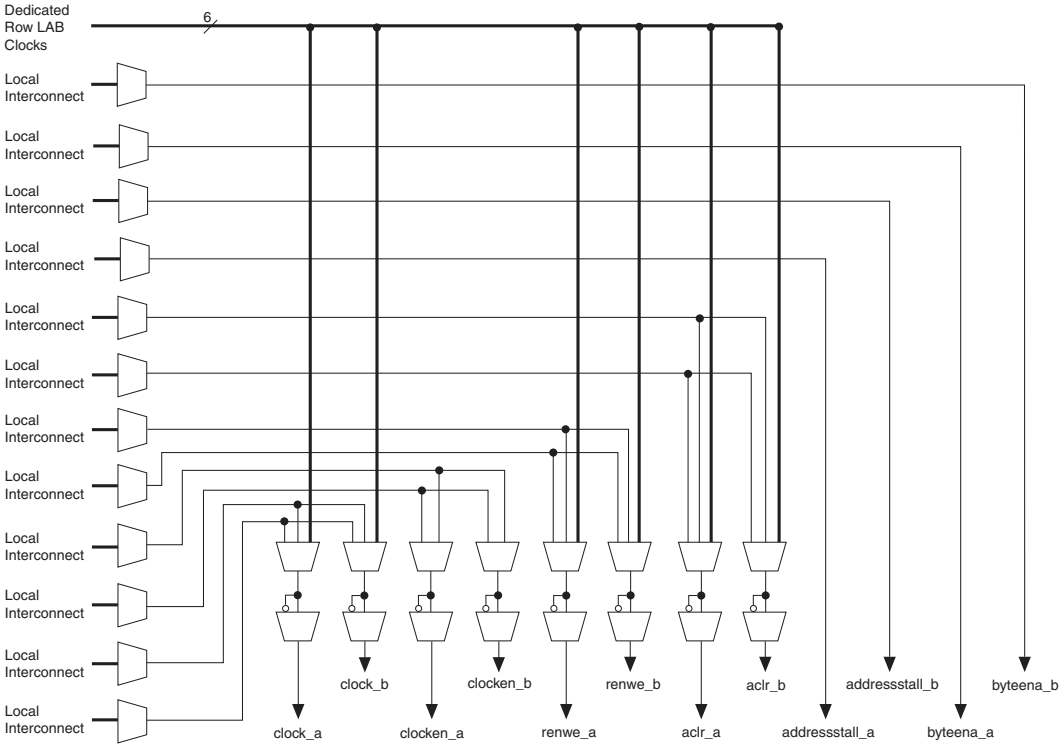
Table 5–52 shows the DQS bus clock skew adder specifications.

Table 5–52. DQS Bus Clock Skew Adder Specifications

Mode	DQS Clock Skew Adder	Unit
×9	155	ps
×18	190	ps

Note to Table 5–52:
(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a ×9 DQ group is 155 ps or ±77.5 ps.

Figure 8–1. M4K Control Signal Selection



Parity Bit Support

Error detection using parity check is possible using the parity bit, with additional logic implemented in LEs to ensure data integrity. Parity-size data words can also be used for other purposes such as storing user-specified control bits.

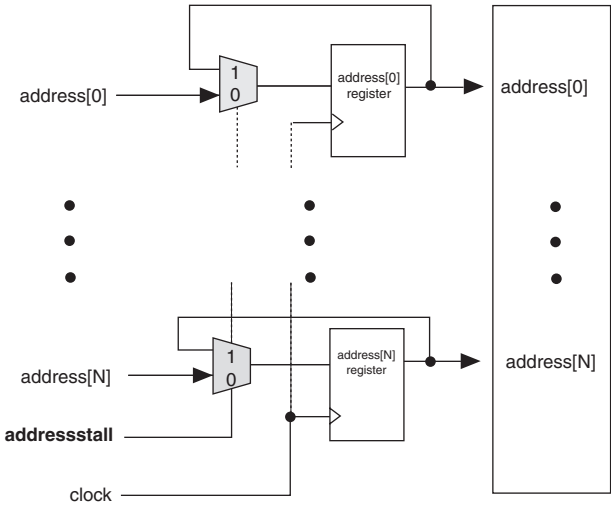
Refer to the *Using Parity to Detect Errors White Paper* for more information.

Byte Enable Support

All M4K memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable (`wren`) signals, along with the byte enable (`byteena`) signals, control the RAM block's write operations. The default value for the byte enable signals is high (enabled), in which

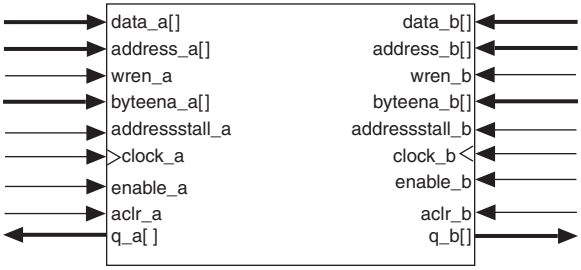
Figure 8–3 shows an address clock enable block diagram. The address register output is fed back to its input via a multiplexer. The multiplexer output is selected by the address clock enable (`addressstall`) signal. Address latching is enabled when the `addressstall` signal goes high (active high). The output of the address register is then continuously fed into the input of the register until the `addressstall` signal goes low.

Figure 8–3. Cyclone II Address Clock Enable Block Diagram



The address clock enable is typically used for cache memory applications to improve efficiency during a cache-miss. The default value for the address clock enable signals is low (disabled). Figures 8–4 and 8–5 show the address clock enable waveforms during the read and write cycles, respectively.

Figure 8–10. Cyclone II True Dual-Port Mode *Note (1)*



Note to Figure 8–10:
(1) True dual-port memory supports input and output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M4K blocks in true dual-port mode is 256 × 16-bit (18-bit with parity).

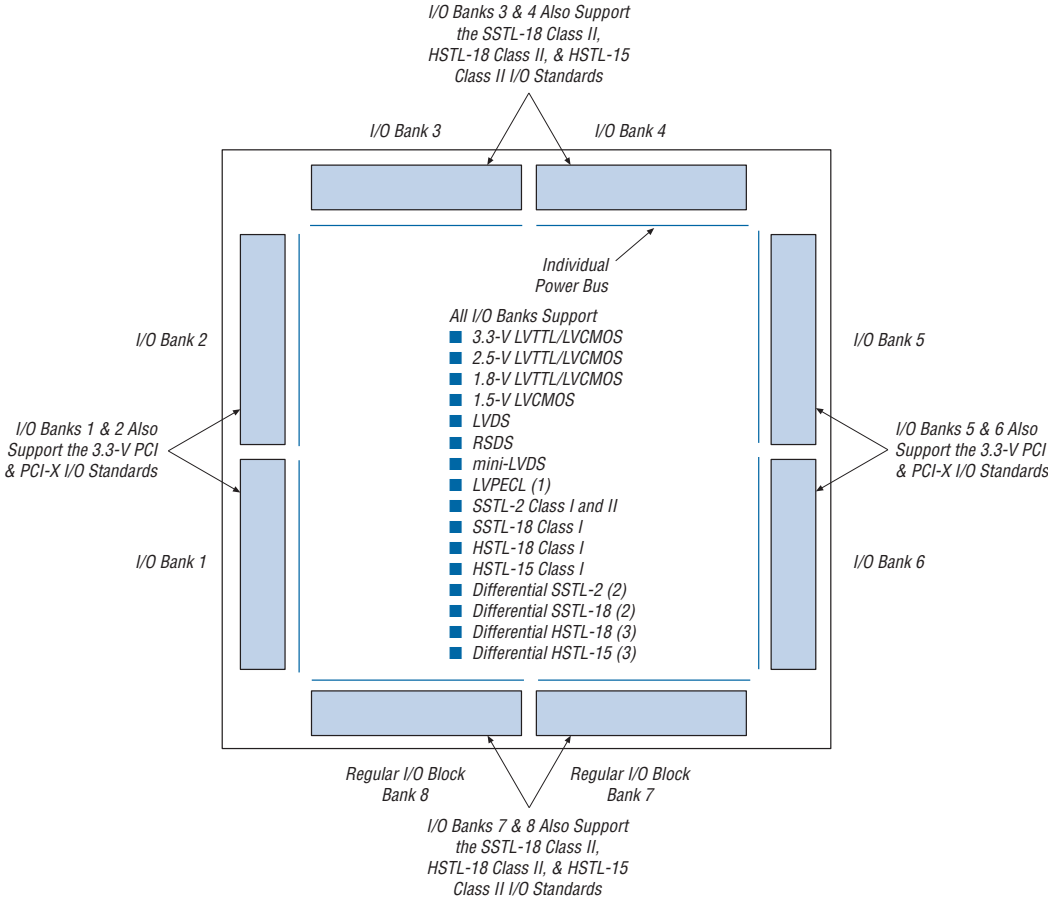
The 128 × 32-bit (36-bit with parity) configuration of the M4K block is unavailable because the number of output drivers is equivalent to the maximum bit width. The maximum width of the true dual-port RAM equals half of the total number of output drivers because true dual-port RAM has outputs on two ports. Table 8–6 lists the possible M4K block mixed-port width configurations.

Table 8–6. Cyclone II Memory Block Mixed-Port Width Configurations (True Dual-Port)

Read Port	Write Port						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

In true dual-port configuration, the RAM outputs are in read-during-write mode. This means that during a write operation, data being written to the A or B port of the RAM flows through to the A or B

Figure 11–2. I/O Banks in EP2C15, EP2C20, EP2C35, EP2C50 & EP2C70 Devices



Notes to Figure 11–2:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

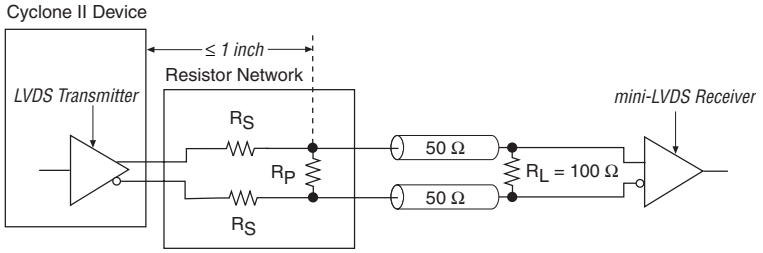
(2) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(3) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

Cyclone II High-Speed I/O Interface

Cyclone II devices provide a multi-protocol interface that allows communication between a variety of I/O standards, including LVDS, LVPECL, RSDS, mini-LVDS, differential HSTL, and differential SSTL. This feature makes the Cyclone II device family ideal for applications that require multiple I/O standards, such as protocol translation.

Figure 11–10. mini-LVDS Resistor Network



Note to Figure 11–10:
(1) R_S = 120 Ω and R_P = 170 Ω

mini-LVDS Software Support

When designing for the mini-LVDS I/O standard, assign the mini-LVDS I/O standard to the I/O pins intended for mini-LVDS in the Quartus II software. Contact Altera Applications for reference designs.

LVPECL Support in Cyclone II

The LVPECL I/O standard is a differential interface standard requiring a 3.3-V V_{CCIO} and is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS. However, LVPECL has a larger differential output voltage swing than LVDS. Cyclone II devices support the LVPECL input standard at the clock input pins only. Table 11–4 shows the LVPECL electrical characteristics for Cyclone II devices. Figure 11–11 shows the LVPECL I/O interface.

Table 11–4. LVPECL Electrical Characteristics for Cyclone II Devices

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		3.135	3.3	3.465	V
V_{IH}	Input high voltage		2,100		2,880	mV
V_{IL}	Input low voltage		0		2,200	mV
V_{ID}	Differential input voltage	Peak to peak	100	600	950	mV

13. Configuring Cyclone II Devices

CII51013-3.1

Introduction

Cyclone® II devices use SRAM cells to store configuration data. Since SRAM memory is volatile, configuration data must be downloaded to Cyclone II devices each time the device powers up. You can use the active serial (AS) configuration scheme, which can operate at a DCLK frequency up to 40 MHz, to configure Cyclone II devices. You can also use the passive serial (PS) and Joint Test Action Group (JTAG)-based configuration schemes to configure Cyclone II devices. Additionally, Cyclone II devices can receive a compressed configuration bitstream and decompress this data on-the-fly, reducing storage requirements and configuration time.

This chapter explains the Cyclone II configuration features and describes how to configure Cyclone II devices using the supported configuration schemes. This chapter also includes configuration pin descriptions and the Cyclone II configuration file format.

For more information on setting device configuration options or creating configuration files, see the *Software Settings* chapter in the *Configuration Handbook*.

Cyclone II Configuration Overview

You can use the AS, PS, and JTAG configuration schemes to configure Cyclone II devices. You can select which configuration scheme to use by driving the Cyclone II device MSEL pins either high or low as shown in Table 13–1. The MSEL pins are powered by the V_{CCIO} power supply of the bank they reside in. The MSEL[1..0] pins have 9-kΩ internal pull-down resistors that are always active. During power-on reset (POR) and reconfiguration, the MSEL pins have to be at LVTTL V_{IL} or V_{IH} levels to be considered a logic low or logic high, respectively. Therefore, to avoid any problems with detecting an incorrect configuration scheme, you should connect the MSEL[] pins to the V_{CCIO} of the I/O bank they reside in and GND without any pull-up or pull-down resistors. The MSEL[] pins should not be driven by a microprocessor or another device.

Table 13–1. Cyclone II Configuration Schemes		
Configuration Scheme	**MSEL1**	**MSEL0**
AS (20 MHz)	0	0
PS	0	1
Fast AS (40 MHz) *(1)*	1	0
JTAG-based Configuration *(2)*	*(3)*	*(3)*

Notes to Table 13–1:

(1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

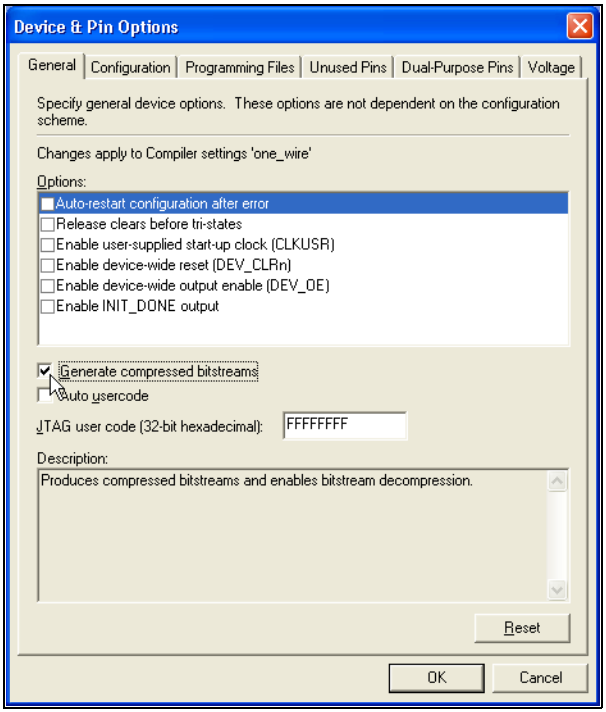
(2) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

(3) Do not leave the MSEL pins floating; connect them to V_{CCIO} or ground. These pins support the non-JTAG configuration scheme used in production. If you are only using JTAG configuration, you should connect the MSEL pins to ground.

You can download configuration data to Cyclone II FPGAs with the AS, PS, or JTAG interfaces using the options in Table 13–2.

Table 13–2. Cyclone II Device Configuration Schemes	
Configuration Scheme	**Description**
AS configuration	Configuration using serial configuration devices (EPCS1, EPCS4, EPCS16 or EPCS64 devices)
PS configuration	Configuration using enhanced configuration devices (EPC4, EPC8, and EPC16 devices), EPC2 and EPC1 configuration devices, an intelligent host (microprocessor), or a download cable
JTAG-based configuration	Configuration via JTAG pins using a download cable, an intelligent host (microprocessor), or the Jam™ Standard Test and Programming Language (STAPL)

Figure 13–1. Enabling Compression for Cyclone II Bitstreams in Compiler Settings



You can also use the following steps to enable compression when creating programming files from the Convert Programming Files window.

1. Click **Convert Programming Files** (File menu).
2. Select the Programming File type. Only Programmer Object Files (**.pof**), SRAM HEXOUT, RBF, or TTF files support compression.
3. For POFs, select a configuration device.
4. Select **Add File** and add a Cyclone II SRAM Object File(s) (**.sof**).
5. Select the name of the file you added to the SOF Data area and click on **Properties**.
6. Check the **Compression** check box.

You should put a buffer before the DATA and DCLK output from the master Cyclone II device to avoid signal strength and signal integrity issues. The buffer should not significantly change the DATA-to-DCLK relationships or delay them with respect to other AS signals (ASDI and nCS). Also, the buffer should only drive the slave Cyclone II devices, so that the timing between the master Cyclone II device and serial configuration device is unaffected.

This configuration method supports both compressed and uncompressed SOFs. Therefore, if the configuration bitstream size exceeds the capacity of a serial configuration device, you can enable the compression feature in the SOF file used or you can select a larger serial configuration device.

Estimating AS Configuration Time

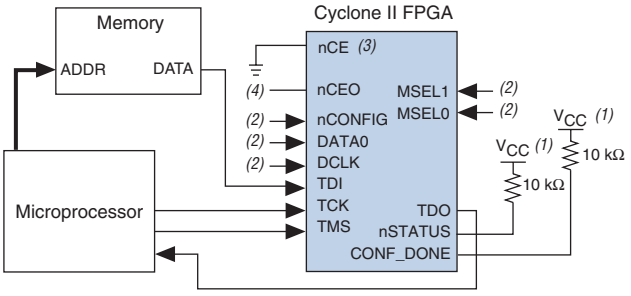
The AS configuration time is the time it takes to transfer data from the serial configuration device to the Cyclone II device. The Cyclone II DCLK output (generated from an internal oscillator) clocks this serial interface. As listed in Table 13–5, if you are using the 40-MHz oscillator, the DCLK minimum frequency is 20 MHz (50 ns). Therefore, the maximum configuration time estimate for an EP2C5 device (1,223,980 bits of uncompressed data) is:

RBF size × (maximum DCLK period / 1 bit per DCLK cycle) = estimated maximum configuration time

1,223,980 bits × (50 ns / 1 bit) = 61.2 ms

To estimate the typical configuration time, use the typical DCLK period listed in Table 13–5. With a typical DCLK period of 38.46 ns, the typical configuration time is 47.1 ms. Enabling compression reduces the amount of configuration data that is transmitted to the Cyclone II device, which also reduces configuration time. On average, compression reduces configuration time by 50%.

Figure 13–23. JTAG Configuration of a Single Device Using a Microprocessor



Notes to Figure 13–23:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain.

(2) Connect the nCONFIG and MSEL[1..0] pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the nCONFIG pin to V_{CC}, and the MSEL[1..0] pins to ground. In addition, pull DCLK and DATA0 to either high or low, whichever is convenient on your board.

(3) nCE must be connected to GND or driven low for successful JTAG configuration.

(4) If using an EPCS4 or EPCS1 device, set MSEL[1..0] to 00. See Table 13–4 for more details.

JTAG Configuration of Multiple Devices

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system using JTAG BST circuitry. Figure 13–24 shows multiple device JTAG configuration.

Table 15–2. Thermal Resistance of Cyclone II Devices for Board Meeting JEDEC Specifications (Part 2 of 2)

Device	Pin Count	Package	θ_{JA} (°C/W) Still Air	θ_{JA} (°C/W) 100 ft./min.	θ_{JA} (°C/W) 200 ft./min.	θ_{JA} (°C/W) 400 ft./min.	θ_{JC} (°C/W)
EP2C50	484	FineLine BGA	18.4	14.4	12.4	10.9	2.8
	484	Ultra FineLine BGA	19.6	15.6	13.6	11.9	4.4
	672	FineLine BGA	17.7	13.7	11.8	10.2	2.6
EP2C70	672	FineLine BGA	16.9	13	11.1	9.7	2.2
	896	FineLine BGA	16.3	11.9	10.5	9.1	2.1

Table 15–3 provides board dimension information for each package.

Table 15–3. PCB Dimensions Notes (1), (2)

2.5 mm Thick	Signal Layers	Power/Ground Layers	Package Dimension (mm)	Board Dimension (mm)
F896	10	10	31	91
F672	8	8	27	87
F672	7	7	27	87
F484	7	7	23	83
F484	6	6	23	83
U484	7	7	19	79
U484	6	6	19	79
F256	6	6	17	77

Notes to Table 15–3:
(1) Power layer Cu thickness 35 um, Cu 90%
(2) Signal layer Cu thickness 17 um, Cu 15%