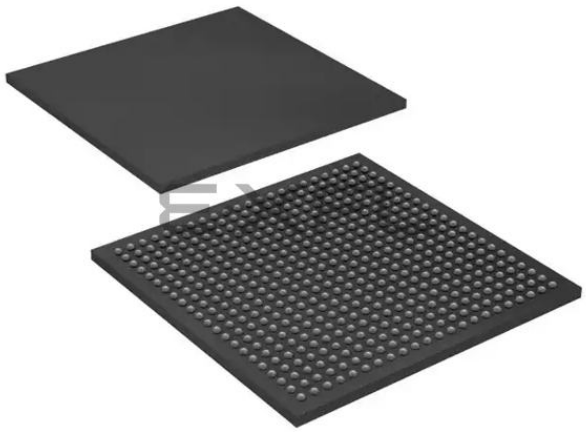

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	294
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50u484c7

A LAB-wide asynchronous load signal to control the logic for the register's preset signal is not available. The register preset is achieved by using a NOT gate push-back technique. Cyclone II devices can only support either a preset or asynchronous clear signal.

In addition to the clear port, Cyclone II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Cyclone II architecture, connections between LEs, M4K memory blocks, embedded multipliers, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

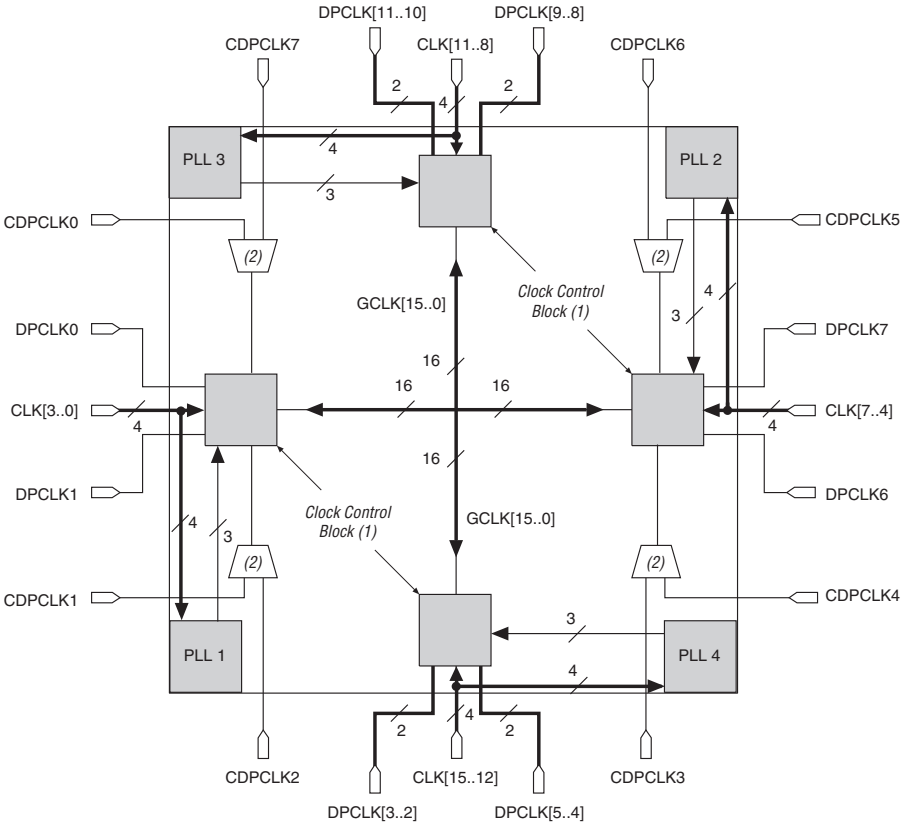
The MultiTrack interconnect consists of row (direct link, R4, and R24) and column (register chain, C4, and C16) interconnects that span fixed distances. A routing structure with fixed-length resources for all devices allows predictable and repeatable performance when migrating through different device densities.

Row Interconnects

Dedicated row interconnects route signals to and from LABs, PLLs, M4K memory blocks, and embedded multipliers within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 interconnects for high-speed access across the length of the device

Figure 2–12. EP2C15 & Larger PLL, CLK[], DPCLK[] & Clock Control Block Locations



Notes to Figure 2–12:

(1) There are four clock control blocks on each side.

(2) Only one of the corner CDPCLK pins in each corner can feed the clock control block at a time. The other CDPCLK pins can be used as general-purpose I/O pins.

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes

Clock Mode	Description
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`.
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

Table 2–9. Cyclone II M4K Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Table 2–16. Programmable Drive Strength (Part 2 of 2) Note (1)		
I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top & Bottom I/O Pins	Side I/O Pins
LVCMOS (1.5 V)	2	2
	4	4
	6	6
	8	
SSTL-2 class I	8	8
	12	12
SSTL-2 class II	16	16
	20	
	24	
SSTL-18 class I	6	6
	8	8
	10	10
	12	
SSTL-18 class II	16	
	18	
HSTL-18 class I	8	8
	10	10
	12	12
HSTL-18 class II	16	
	18	
	20	
HSTL-15 class I	8	8
	10	
	12	
HSTL-15 class II	16	

Note to Table 2–16:
(1) The default current in the Quartus II software is the maximum setting for each I/O standard.

Open-Drain Output

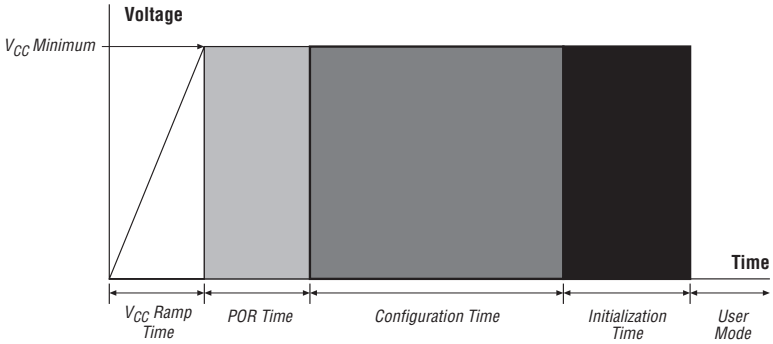
Cyclone II devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (that is, interrupt and write-enable signals) that can be asserted by any of several devices.

For Cyclone II devices, wake-up time consists of power-up, POR, configuration, and initialization. The device must properly go through all four stages to configure correctly and begin operation. You can calculate wake-up time using the following equation:

Wake-Up Time = V_{CC} Ramp Time + POR Time + Configuration Time + Initialization Time

Figure 4–3 illustrates the components of wake up time.

Figure 4–3. Cyclone II Wake-Up Time



Note to Figure 4–3:
(1) V_{CC} ramp must be monotonic.

The V_{CC} ramp time and POR time will depend on the device characteristics and the power supply used in your system. The fast-on devices require a maximum V_{CC} ramp time of 2 ms and have a maximum POR time of 12 ms.

Configuration time will depend on the configuration mode chosen and the configuration file size. You can calculate configuration time by multiplying the number of bits in the configuration file with the period of the configuration clock. For fast configuration times, you should use Passive Serial (PS) configuration mode with maximum DCLK frequency of 100 MHz. In addition, you can use compression to reduce the configuration file size and speed up the configuration time. The t_{CD2UM} or t_{CD2UMC} parameters will determine the initialization time.

For more information on the t_{CD2UM} or t_{CD2UMC} parameters, refer to the *Configuring Cyclone II Devices* chapter in the *Cyclone II Device Handbook*.

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL_18_CLASS_II	0	pF
1.5V_HSTL_CLASS_I	0	pF
1.5V_HSTL_CLASS_II	0	pF
1.8V_HSTL_CLASS_I	0	pF
1.8V_HSTL_CLASS_II	0	pF
DIFFERENTIAL_SSTL_2_CLASS_I	0	pF
DIFFERENTIAL_SSTL_2_CLASS_II	0	pF
DIFFERENTIAL_SSTL_18_CLASS_I	0	pF
DIFFERENTIAL_SSTL_18_CLASS_II	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
LVDS	0	pF
1.2V_HSTL	0	pF
1.2V_DIFFERENTIAL_HSTL	0	pF

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 1 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
LVTTL	4 mA	t_{OP}	1524	1599	2903	3125	3341	3348	ps
		t_{DIP}	1656	1738	3073	3319	3567	3567	ps
	8 mA	t_{OP}	1343	1409	2670	2866	3054	3061	ps
		t_{DIP}	1475	1548	2840	3060	3280	3280	ps
	12 mA	t_{OP}	1287	1350	2547	2735	2917	2924	ps
		t_{DIP}	1419	1489	2717	2929	3143	3143	ps
	16 mA	t_{OP}	1239	1299	2478	2665	2844	2851	ps
		t_{DIP}	1371	1438	2648	2859	3070	3070	ps
	20 mA	t_{OP}	1228	1288	2456	2641	2820	2827	ps
		t_{DIP}	1360	1427	2626	2835	3046	3046	ps
	24 mA (1)	t_{OP}	1220	1279	2452	2637	2815	2822	ps
		t_{DIP}	1352	1418	2622	2831	3041	3041	ps
LVCMOS	4 mA	t_{OP}	1346	1412	2509	2695	2873	2880	ps
		t_{DIP}	1478	1551	2679	2889	3099	3099	ps
	8 mA	t_{OP}	1240	1300	2473	2660	2840	2847	ps
		t_{DIP}	1372	1439	2643	2854	3066	3066	ps
	12 mA	t_{OP}	1221	1280	2428	2613	2790	2797	ps
		t_{DIP}	1353	1419	2598	2807	3016	3016	ps
	16 mA	t_{OP}	1203	1262	2403	2587	2765	2772	ps
		t_{DIP}	1335	1401	2573	2781	2991	2991	ps
	20 mA	t_{OP}	1194	1252	2378	2562	2738	2745	ps
		t_{DIP}	1326	1391	2548	2756	2964	2964	ps
	24 mA (1)	t_{OP}	1192	1250	2382	2566	2742	2749	ps
		t_{DIP}	1324	1389	2552	2760	2968	2968	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 6 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.5V_DIFFERENTIAL _HSTL_CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
LVDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
RSDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
MINI_LVDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
SIMPLE_RSDS	—	t_{OP}	1221	1280	2258	2435	2605	2612	ps
		t_{DIP}	1353	1419	2428	2629	2831	2831	ps
1.2V_HSTL	—	t_{OP}	2403	2522	4635	5344	6046	6053	ps
		t_{DIP}	2535	2661	4805	5538	6272	6272	ps
1.2V_DIFFERENTIAL _HSTL	—	t_{OP}	2403	2522	4635	5344	6046	6053	ps
		t_{DIP}	2535	2661	4805	5538	6272	6272	ps

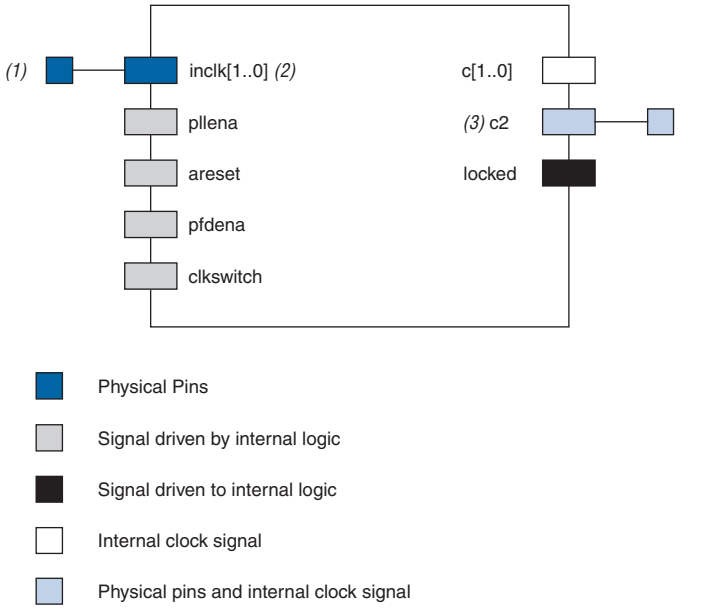
Notes to Table 5–42:

(1) This is the default setting in the Quartus II software.
(2) These numbers are for commercial devices.
(3) These numbers are for automotive devices.

Software Overview

You can use the altpll megafunction in the Quartus II software to enable Cyclone II PLLs. Figure 7–3 shows the available ports in Cyclone II PLLs and their sources and destinations. The c0 and c1 counters feed the internal global clock networks and the c2 counter can feed the global clock network and a dedicated external clock output pin (PLL<#>_OUT) at the same time.

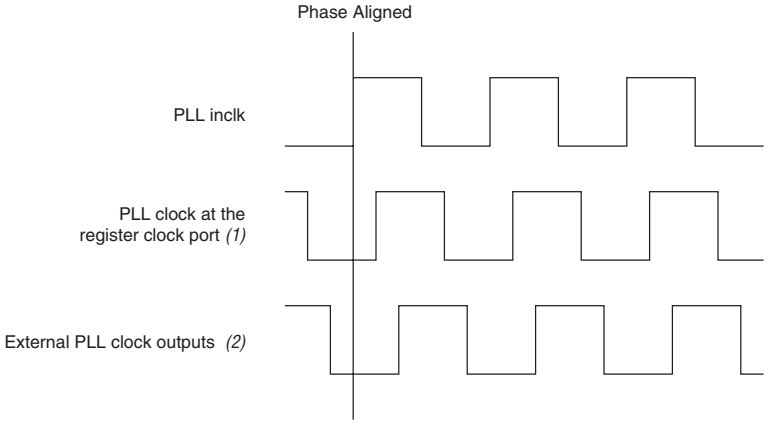
Figure 7–3. Cyclone II PLL Signals



Notes to Figure 7–3:

(1) These signals can be assigned to either a single-ended or differential I/O standard.
(2) The inclk must be driven by one of two dedicated clock input pins.
(3) This counter output can drive both a dedicated external clock output (PLL<#>_OUT) and the global clock network.

Figure 7–6. Phase Relationship between Cyclone II PLL Clocks in No Compensation Mode



Notes to Figure 7–6:
(1) Internal clocks fed by the PLL are in phase with each other.
(2) The external clock outputs can lead or lag the PLL internal clocks.

Source-Synchronous Mode

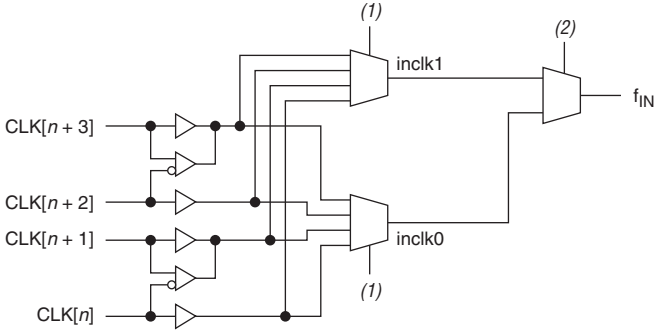
If data and clock arrive at the same time at the input pins, they are guaranteed to keep the same phase relationship at the clock and data ports of any IOE input register. Figure 7–7 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfer. Data and clock signals at the IOE experience similar buffer delays as long as the same I/O standard is used.

Manual Clock Switchover

The Cyclone II PLLs support manual switchover of the reference clock through internal logic. This enables you to switch between two reference input clocks. Use this feature for a dual clock domain application such as in a system that turns on the redundant clock if the primary clock stops running.

Figure 7–10 shows how the PLL input clock (f_{IN}) is generated from one of four possible clock sources. The first stage multiplexing consists of two dedicated multiplexers that generate two single-ended or two differential clocks from four dedicated clock pins. These clock signals are then multiplexed to generate f_{IN} by using another dedicated 2-to-1 multiplexer. The first stage multiplexers are controlled by configuration bit settings in the configuration file generated by the Quartus II software, while the second stage multiplexer is either controlled by the configuration bit settings or logic array signal to allow the f_{IN} to be controlled dynamically. This allows the implementation of a manual clock switchover circuit where the PLL reference clock can be switched during user mode for applications that requires clock redundancy.

Figure 7–10. Cyclone II PLL Input Clock Generation



Notes to Figure 7–10:

(1) This select line is set through the configuration file.

(2) This select line can either be set through the configuration file or it can be dynamically set in user mode when using the manual switchover feature.

ROM Mode

Cyclone II memory blocks support ROM mode. A MIF initializes the ROM contents of these blocks. The address lines of the ROM are registered. The outputs can be registered or unregistered. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Buffer Mode

A single clock or dual clock FIFO buffer may be implemented in the memory blocks. Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain. All FIFO memory configurations have synchronous inputs. However, the FIFO buffer outputs are always combinational (i.e., not registered). Simultaneous read and write from an empty FIFO buffer is not supported.

For more information on FIFO buffers, refer to the *Single- & Dual-Clock FIFO Megafunctions User Guide*.

Clock Modes

Depending on which memory mode is selected, the following clock modes are available:

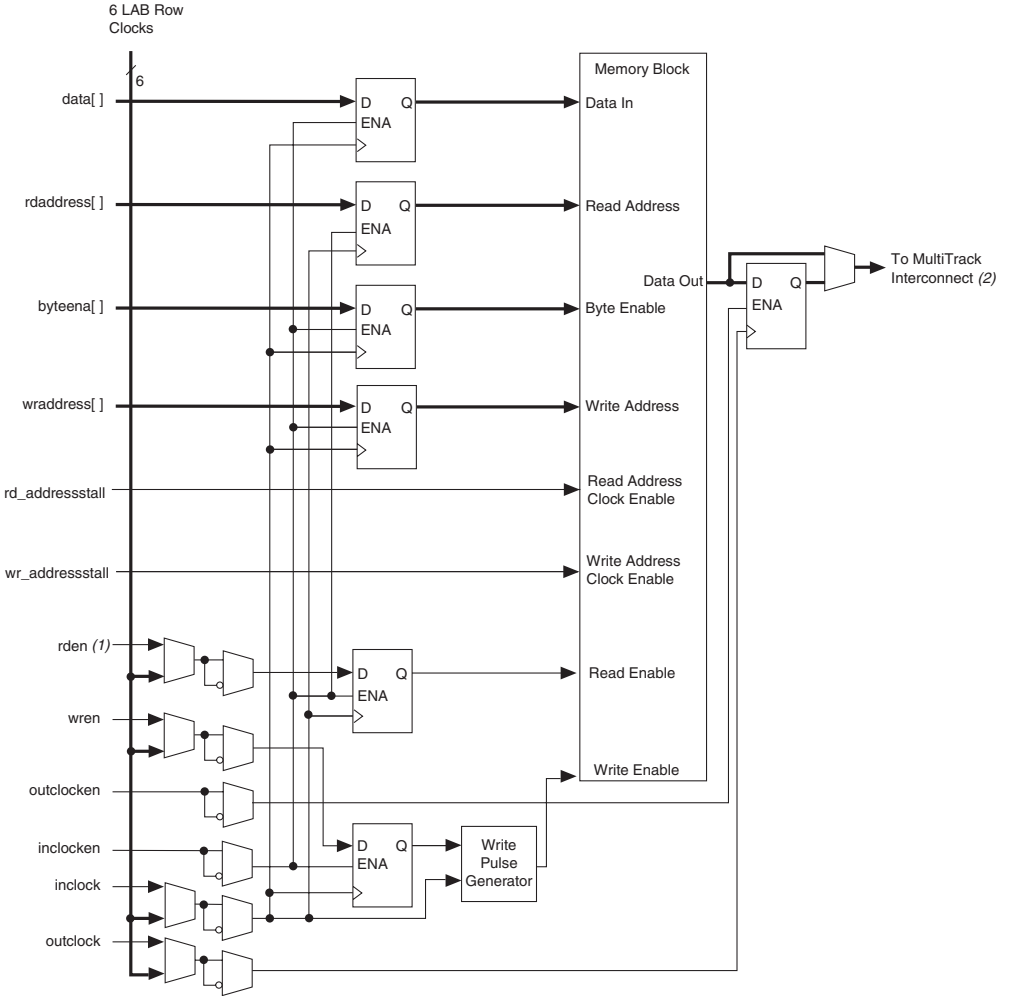
- Independent
- Input/output
- Read/write
- Single-clock

Table 8–7 shows these clock modes supported by all memory blocks when configured in each respective memory modes.

Table 8–7. Cyclone II Memory Clock Modes

Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

Figure 8–15. Cyclone II Input/Output Clock Mode in Simple Dual-Port Mode *Notes (1), (2)*



Notes to Figure 8–15:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack™ interconnect.

The DQS pins are listed in the Cyclone II pin tables as DQS[1..0]T, DQS[1..0]B, DQS[1..0]L, and DQS[1..0]R for the EP2C5 and EP2C8 devices and DQS[5..0]T, DQS[5..0]B, DQS[3..0]L, and DQS[3..0]R for the larger devices. The T denotes pins on the top of the device, the B denotes pins on the bottom of the device, the L denotes pins on the left of the device, and the R denotes pins on the right of the device. The corresponding DQ pins are marked as DQ[5..0]T[8..0], where [5..0] indicates which DQS group the pins belong to.

In the Cyclone II pinouts, the DQ groups with 9 DQ pins are also used in the ×8 mode with the corresponding DQS pins, leaving the unused DQ pin available as a regular I/O pin. The DQ groups that have 18 DQ pins are also used in the ×16 mode with the corresponding DQS pins, leaving the two unused DQ pins available as regular I/O pins. For example, DQ1T[8..0] can be used in the ×8 mode, provided it is used with DQS1T. The remaining unused DQ pin, DQ1T8, is available as a regular I/O pin.

When not used as DQ or DQS pins, these pins are available as regular I/O pins. Table 9–3 shows the number of DQS pins supported in each I/O bank in each Cyclone II device density.

Table 9–3. Available DQS Pins in Each I/O Bank & Each Device *Note (1)*

Device	Top I/O Bank	Bottom I/O Bank	Left I/O Bank	Right I/O Bank
EP2C5, EP2C8	DQS[1..0]T	DQS[1..0]B	DQS[1..0]L	DQS[1..0]R
EP2C15, EP2C20, EP2C35, EP2C50, EP2C70	DQS[5..0]B	DQS[5..0]T	DQS[3..0]L	DQS[3..0]R

Note to Table 9–3:
(1) Numbers are preliminary.

The DQ pin numbering is based on ×8/×9 mode. There are up to 8 DQS/DQ groups in ×8 mode or 4 DQS/DQ groups in ×9 mode in I/O banks for EP2C5 and EP2C8. For the larger devices, there are up to 20 DQS/DQ groups in ×8 mode or 8 DQS/DQ groups in ×9 mode. Although there are up to 20 DQS/DQ groups in the ×8 mode available in the larger Cyclone II devices, but because of the available clock resources in the Cyclone II devices, only 16 DQS/DQ groups can be utilized for the external memory interface. There is a total of 16 global clock buses available for routing DQS signals but 2 of them are needed for routing the –90° write clock and the system clock to the external memory devices. This reduces the global clock resources to 14 global clock buses for routing DQS signals. Incoming DQS signals are all routed to the clock control block, and are then routed to the global clock bus to clock the DDR LE registers. For EP2C5 and EP2C8 devices, the DQS signals are routed

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
Differential HSTL-15 class I or class II	Pseudo differential *(3)*	*(4)*	1.5 V	—	—	—	✓ *(6)*	—
		1.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential HSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—	—	✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
LVDS	Differential	2.5 V	2.5 V	✓	✓	✓	✓	✓
RSDS and mini-LVDS *(7)*	Differential	*(4)*	2.5 V	—	✓	—	✓	✓
LVPECL *(8)*	Differential	3.3 V/ 2.5 V/ 1.8 V/ 1.5 V	*(4)*	✓	—	✓	—	—

Notes to Table 10–1:

(1) These pins support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.
(2) PCI-X does not meet the IV curve requirement at the linear region. PCI-clamp diode is not available on top and bottom I/O pins.
(3) Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Pseudo-differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them.
(4) This I/O standard is not supported on these I/O pins.
(5) This I/O standard is only supported on the dedicated clock pins.
(6) `PLL_OUT` does not support differential SSTL-18 class II and differential 1.8 and 1.5-V HSTL class II.
(7) mini-LVDS and RSDS are only supported on output pins.
(8) LVPECL is only supported on clock inputs, not DQS and dual-purpose clock pins.

3.3-V LVTTL (EIA/JEDEC Standard JESD8-B)

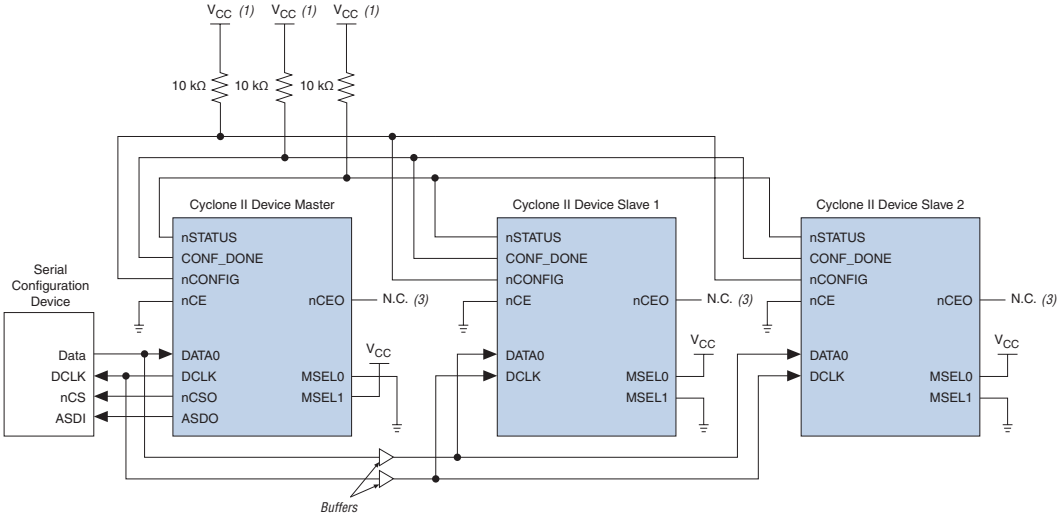
The 3.3-V LVTTL I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVTTL standard defines the DC interface parameters for digital circuits operating from a 3.0-/3.3-V power supply and driving or being driven by LVTTL-compatible devices.

The LVTTL input standard specifies a wider input voltage range of $-0.3\ V \leq V_I \leq 3.9\ V$. Altera recommends an input voltage range of $-0.5\ V \leq V_I \leq 4.1\ V$.

Single SOF

The second method configures both the master and slave Cyclone II devices with the same SOF. The serial configuration device stores one copy of the SOF file. This setup is shown in Figure 13–6 where the master is setup in AS mode, and the slave devices are setup in PS mode (MSEL=01). You could setup one or more slave devices in the chain and all the slave devices are setup in the same way as shown in Figure 13–6.

Figure 13–6. Multiple Device AS Configuration When FPGAs Receive the Same Data with a Single SOF



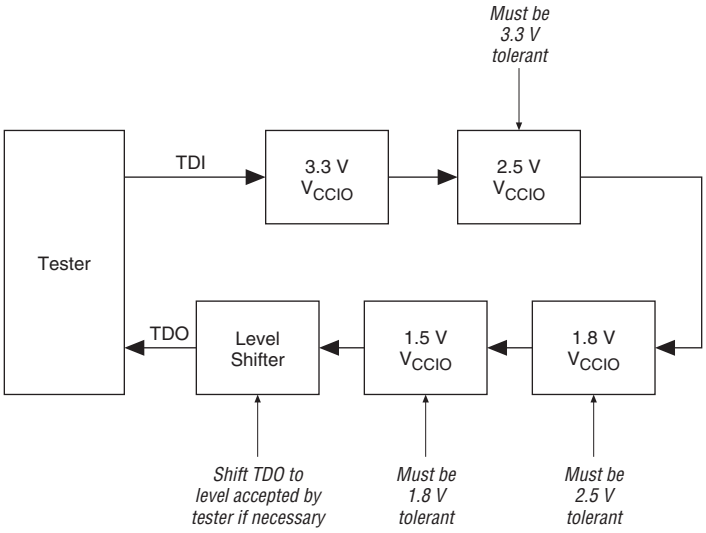
Notes to Figure 13–6:

(1) Connect the pull-up resistors to a 3.3-V supply.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

In this setup, all the Cyclone II devices in the chain are connected for concurrent configuration. This can reduce the AS configuration time because all the Cyclone II devices are configured in one configuration cycle. Connect the nCE input pins of all the Cyclone II devices to ground. You can either leave the nCEO output pins on all the Cyclone II devices unconnected or use the nCEO output pins as normal user I/O pins. The DATA and DCLK pins are connected in parallel to all the Cyclone II devices.

Figure 14–13. JTAG Chain of Mixed Voltages



Using IEEE Std. 1149.1 BST Circuitry

Cyclone II devices have dedicated JTAG pins, and the IEEE Std. 1149.1 BST circuitry is enabled upon device power-up. You can perform BST on Cyclone II FPGAs not only before and after configuration, but also during configuration. Cyclone II FPGAs support the BYPASS, IDCODE, and SAMPLE instructions during configuration without interrupting configuration. To send all other JTAG instructions, you must interrupt configuration using the CONFIG_IO instruction.

The CONFIG_IO instruction allows you to configure I/O buffers via the JTAG port, and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Cyclone II FPGA or waiting for a configuration device to complete configuration. Once configuration has been interrupted and JTAG BST is complete, the part must be reconfigured via JTAG (PULSE_CONFIG instruction) or by pulsing nCONFIG low.

When you perform JTAG boundary-scan testing before configuration, the nCONFIG pin must be held low.

The device-wide reset (DEV_CLRn) and device-wide output enable (DEV_OE) pins on Cyclone II devices do not affect JTAG boundary-scan or configuration operations. Toggling these pins does not disrupt BST operation any more than usual.

Figure 15–5 shows a 484-pin FineLine BGA package outline.

Figure 15–5. 484-Pin FineLine BGA Package Outline