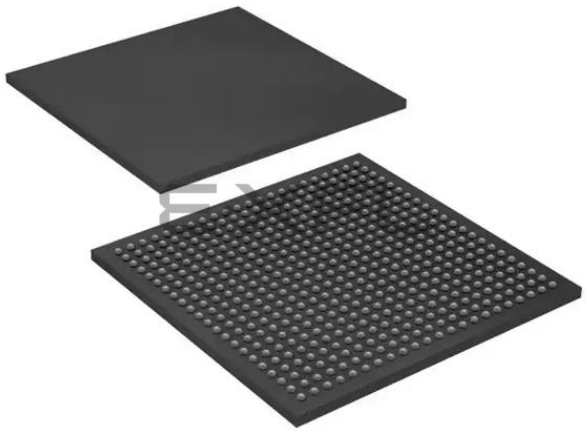

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Details	
Product Status	Active
Number of LABs/CLBs	3158
Number of Logic Elements/Cells	50528
Total RAM Bits	594432
Number of I/O	294
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c50u484c8n

Programmable delays can increase the register-to-pin delays for output registers. Table 2–13 shows the programmable delays for Cyclone II devices.

Table 2–13. Cyclone II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to internal LE registers that reside in two different areas of the device. You set the two combinational input delays by selecting different delays for two different paths under the **Input delay from pin to internal cells logic** option in the Quartus II software. However, if the pin uses the input register, one of delays is disregarded because the IOE only has two paths to internal logic. If the input register is used, the IOE uses one input path. The other input path is then available for the combinational path, and only one input delay assignment is applied.

The IOE registers in each I/O block share the same source for clear or preset. You can program preset or clear for each individual IOE, but both features cannot be used simultaneously. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available for the IOE registers.

External Memory Interfacing

Cyclone II devices support a broad range of external memory interfaces such as SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature dedicated high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The programmable DQS delay chain allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Table 2–16. Programmable Drive Strength (Part 2 of 2) Note (1)		
I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top & Bottom I/O Pins	Side I/O Pins
LVCMOS (1.5 V)	2	2
	4	4
	6	6
	8	
SSTL-2 class I	8	8
	12	12
SSTL-2 class II	16	16
	20	
	24	
SSTL-18 class I	6	6
	8	8
	10	10
	12	
SSTL-18 class II	16	
	18	
HSTL-18 class I	8	8
	10	10
	12	12
HSTL-18 class II	16	
	18	
	20	
HSTL-15 class I	8	8
	10	
	12	
HSTL-15 class II	16	

Note to Table 2–16:
(1) The default current in the Quartus II software is the maximum setting for each I/O standard.

Open-Drain Output

Cyclone II devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (that is, interrupt and write-enable signals) that can be asserted by any of several devices.

Table 5–19. M4K Block Internal Timing Microparameters (Part 2 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KBEH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATAASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATAAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KADDRASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KADDRAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATABSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATABH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KRADDRBSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KRADDRBH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATACO1	466	724	445	826	445	930	ps
	—	—	466	—	466	—	ps
TM4KDATACO2	2345	3680	2234	4157	2234	4636	ps
	—	—	2345	—	2345	—	ps
TM4KCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TM4KCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

EP2C70 Clock Timing Parameters

Tables 5–33 and 5–34 show the clock timing parameters for EP2C70 devices.

Table 5–33. EP2C70 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.575	1.651	2.914	3.105	3.174	ns
t_{COUT}	1.589	1.666	2.948	3.137	3.203	ns
t_{PLLCIN}	–0.149	–0.158	0.27	0.268	0.089	ns
$t_{PLLCOUT}$	–0.135	–0.143	0.304	0.3	0.118	ns

Table 5–34. EP2C70 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.463	1.533	2.753	2.927	3.010	ns
t_{COUT}	1.465	1.535	2.769	2.940	3.018	ns
t_{PLLCIN}	–0.261	–0.276	0.109	0.09	–0.075	ns
$t_{PLLCOUT}$	–0.259	–0.274	0.125	0.103	–0.067	ns

Clock Network Skew Adders

Table 5–35 shows the clock network specifications.

Table 5–35. Clock Network Specifications

Name	Description	Max	Unit
Clock skew adder EP2C5/A, EP2C8/A *(1)*	Inter-clock network, same bank	±88	ps
	Inter-clock network, same side and entire chip	±88	ps
Clock skew adder EP2C15A, EP2C20/A, EP2C35, EP2C50, EP2C70 *(1)*	Inter-clock network, same bank	±118	ps
	Inter-clock network, same side and entire chip	±138	ps

Note to Table 5–35:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Table 5–43. Cyclone II I/O Output Delay for Row Pins (Part 1 of 4)

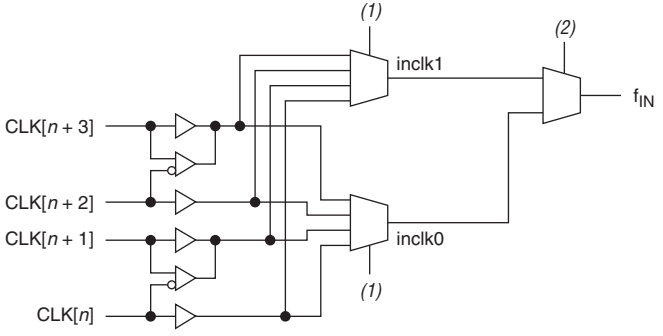
I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial /Auto-motive	Commer-cial					
LVTTL	4 mA	t_{OP}	1343	1408	2539	2694	2885	2891	ps
		t_{DIP}	1467	1540	2747	2931	3158	3158	ps
	8 mA	t_{OP}	1198	1256	2411	2587	2756	2762	ps
		t_{DIP}	1322	1388	2619	2824	3029	3029	ps
	12 mA	t_{OP}	1156	1212	2282	2452	2614	2620	ps
		t_{DIP}	1280	1344	2490	2689	2887	2887	ps
	16 mA	t_{OP}	1124	1178	2286	2455	2618	2624	ps
		t_{DIP}	1248	1310	2494	2692	2891	2891	ps
	20 mA	t_{OP}	1112	1165	2245	2413	2574	2580	ps
		t_{DIP}	1236	1297	2453	2650	2847	2847	ps
	24 mA (1)	t_{OP}	1105	1158	2253	2422	2583	2589	ps
		t_{DIP}	1229	1290	2461	2659	2856	2856	ps
LVCMOS	4 mA	t_{OP}	1200	1258	2231	2396	2555	2561	ps
		t_{DIP}	1324	1390	2439	2633	2828	2828	ps
	8 mA	t_{OP}	1125	1179	2260	2429	2591	2597	ps
		t_{DIP}	1249	1311	2468	2666	2864	2864	ps
	12 mA (1)	t_{OP}	1106	1159	2217	2383	2543	2549	ps
		t_{DIP}	1230	1291	2425	2620	2816	2816	ps
2.5V	4 mA	t_{OP}	1126	1180	2350	2477	2598	2604	ps
		t_{DIP}	1250	1312	2558	2714	2871	2871	ps
	8 mA (1)	t_{OP}	1105	1158	2177	2296	2409	2415	ps
		t_{DIP}	1229	1290	2385	2533	2682	2682	ps

Manual Clock Switchover

The Cyclone II PLLs support manual switchover of the reference clock through internal logic. This enables you to switch between two reference input clocks. Use this feature for a dual clock domain application such as in a system that turns on the redundant clock if the primary clock stops running.

Figure 7–10 shows how the PLL input clock (f_{IN}) is generated from one of four possible clock sources. The first stage multiplexing consists of two dedicated multiplexers that generate two single-ended or two differential clocks from four dedicated clock pins. These clock signals are then multiplexed to generate f_{IN} by using another dedicated 2-to-1 multiplexer. The first stage multiplexers are controlled by configuration bit settings in the configuration file generated by the Quartus II software, while the second stage multiplexer is either controlled by the configuration bit settings or logic array signal to allow the f_{IN} to be controlled dynamically. This allows the implementation of a manual clock switchover circuit where the PLL reference clock can be switched during user mode for applications that requires clock redundancy.

Figure 7–10. Cyclone II PLL Input Clock Generation



Notes to Figure 7–10:

(1) This select line is set through the configuration file.

(2) This select line can either be set through the configuration file or it can be dynamically set in user mode when using the manual switchover feature.

Table 7–8. Global Clock Network Connections (Part 3 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DPCLK3 *(1)*																✓

Notes to Table 7–8:
(1) See the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook* for more information on DPCLK pins.
(2) This pin only applies to EP2C5 and EP2C8 devices.
(3) These pins only apply to EP2C15 devices and larger. Only one of the two CDPCLK pins can feed the clock control block. The other pin can be used as a regular I/O pin.

If the dedicated clock pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the logic array using the MultiTrack interconnect. However, if they are used as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Clock Control Block

Every global clock network is driven by a clock control block residing either on the top, bottom, left, or right side of the Cyclone II device. The global clock network has been optimized for minimum clock skew and delay.

Table 7–9 lists the sources that can feed the clock control block, which in turn feeds the global clock networks.

Table 7–9. Clock Control Block Inputs (Part 1 of 2)

Input	Description
Dedicated clock inputs	Dedicated clock input pins can drive clocks or global signals, such as asynchronous clears, presets, or clock enables onto a given global clock network.
Dual-purpose clock (DPCLK and CDPCLK) I/O inputs	DPCLK and CDPCLK I/O pins are bidirectional dual function pins that can be used for high fan-out control signals, such as protocol signals, TRDY and IRDY signals for PCI, or DQS for DDR, via the global clock network.

Independent Clock Mode

Cyclone II memory blocks can implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables for port A and B registers. However, ports do not support asynchronous clear signals for the registers.

Figure 8–13 shows a memory block in independent clock mode.

Document Revision History

Table 8–8 shows the revision history for this document.

Table 8–8. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v2.4	Corrected Figure 8–12.	—
February 2007 v2.3	• Added document revision history. • Updated "Packed Mode Support" section. • Updated "Mixed-Port Read-During-Write Mode" section and added new Figure 8–24.	• In packed mode support, the maximum data width for each of the two memory block is 18 bits wide. • Added don't care mode information to mixed-port read-during-write mode section.
November 2005 v2.1	Updated Figures 8–13 through 8–20.	—
July 2005 v2.0	Added Clear Signals section.	—
February 2005 v1.1	Added a note to Figures 8-13 through 8-20 regarding violating the setup and hold time on address registers.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Phase Lock Loop (PLL)

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two outputs is needed to generate the system clock and the write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock shifts by –90° from the system clock and generates the DQ signals during writes.

Clock Delay Control

Clock delay control circuit on each DQS pin allows a phase shift that center-aligns the incoming DQS signals within the data window of their corresponding DQ data signals. The phase-shifted DQS signals drive the global clock network. This global DQS signal then clocks the DQ signals on internal LE registers. The clock delay control circuitry is used during the read operations where the DQS signals are acting as input clocks or strobes.

Figure 9–8 illustrates DDR SDRAM interfacing from the I/O pins through the dedicated circuitry to the logic array.

Figure 9–8. DDR SDRAM Interfacing

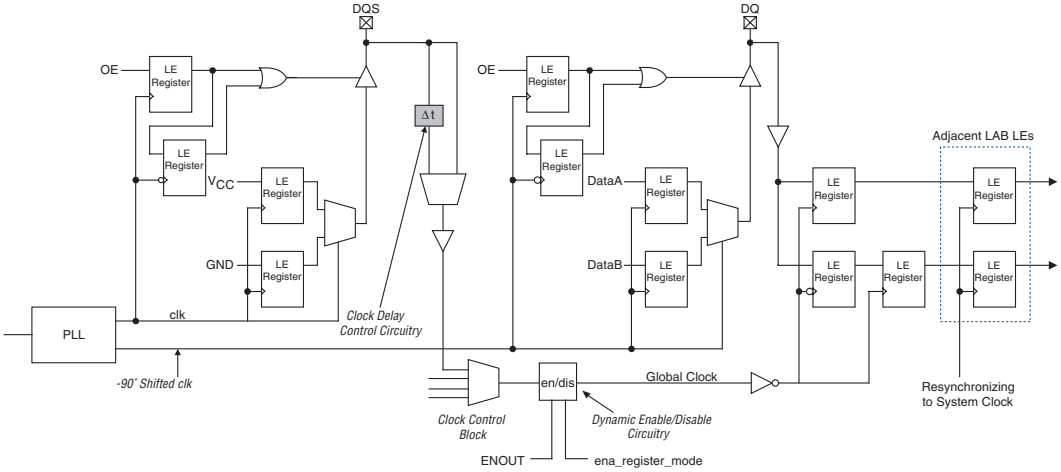
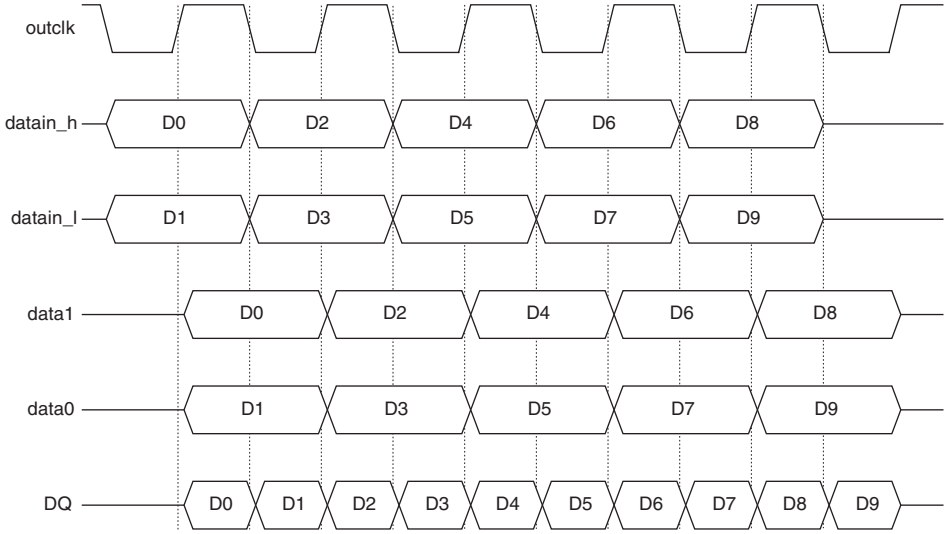


Figure 9–1 on page 9–4 shows an example where the DQS signal is shifted by 90°. The DQS signal goes through the 90° shift delay set by the clock delay control circuitry and global clock routing delay from the clock delay control circuitry to the DQ LE registers. The DQ signals only goes through routing delays from the DQ pin to the DQ LE registers. The delay from

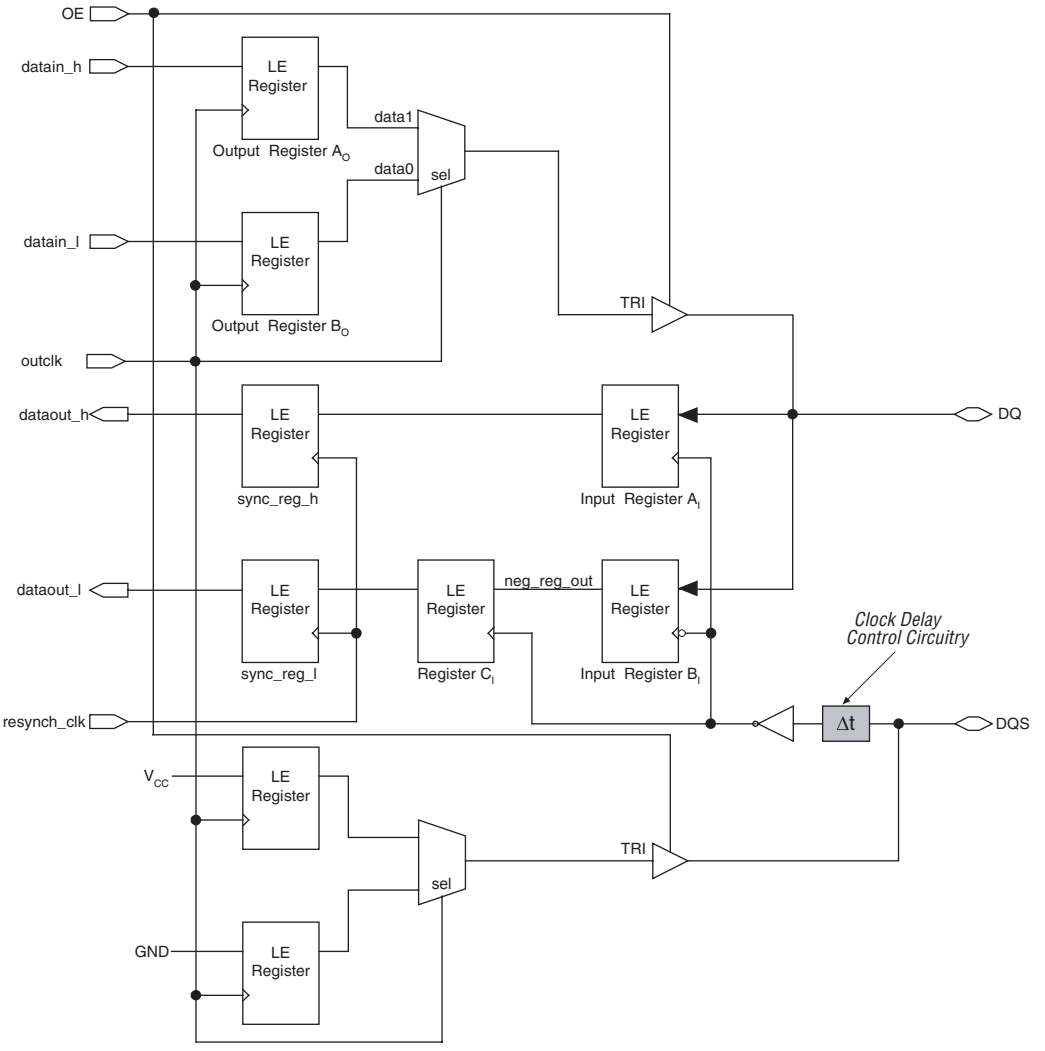
Figure 9–15. DDR Output Waveforms



Bidirectional DDR Registers

Figure 9–16 shows a bidirectional DDR interface constructed using the DDR input and DDR output examples described in the previous two sections. As with the DDR input and DDR output examples, the bidirectional DDR pin can be any available user I/O pin. The registers that implement DDR bidirectional logic are LEs in the LAB adjacent to that pin. The tri-state buffer controls when the device drives data onto the bidirectional DDR pin.

Figure 9–16. Bidirectional DDR Implementation for DDR Memory Interfaces *Note (1)*



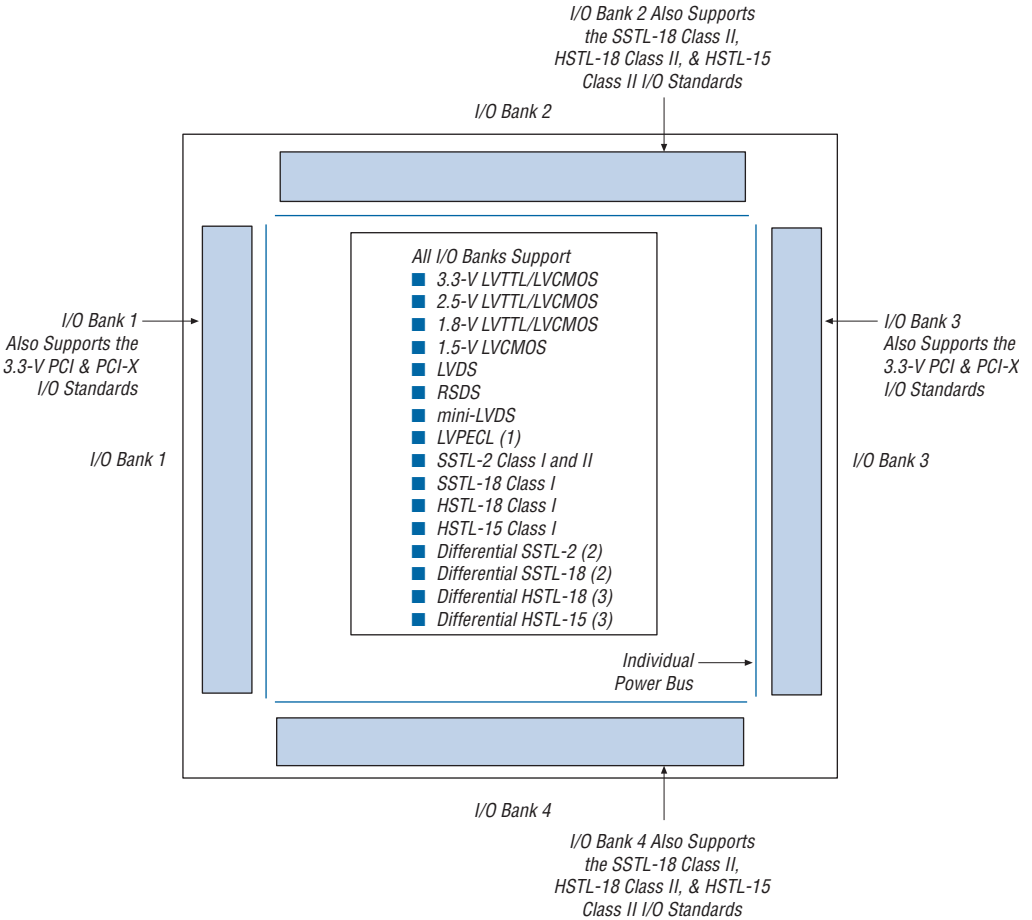
Note to Figure 9–16:

(1) You can use the `altdq` and `altdqs` megafunctions to generate the DQ and DQS signals.

Figure 9–17 shows example waveforms from a bidirectional DDR implementation.

pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. Cyclone II pin tables list the pins that support the high-speed I/O interface.

Figure 11–1. I/O Banks in EP2C5 & EP2C8 Devices



Notes to Figure 11–1:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(2) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(3) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

RSDS I/O Standard Support in Cyclone II Devices

The RSDS specification is used in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the National Semiconductor Corporation RSDS Interface Specification and support the RSDS output standard. Table 11–2 shows the RSDS electrical characteristics for Cyclone II devices.

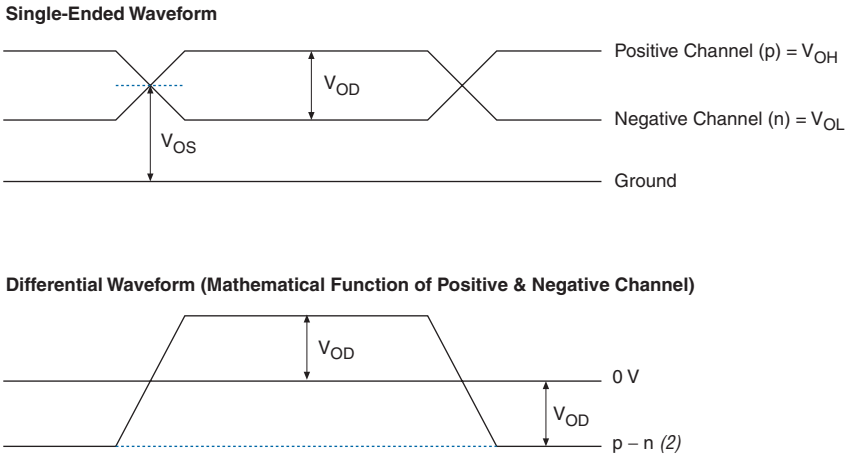
Table 11–2. RSDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	100		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
T_r/T_f	Transition time	20% to 80%		500		ps

Notes to Table 11–2:
(1) The specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

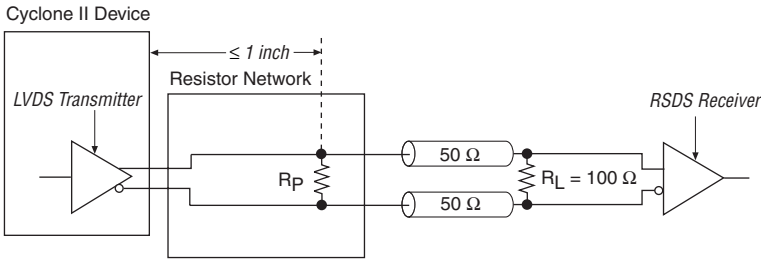
Figure 11–6 shows the RSDS transmitter output signal waveforms.

Figure 11–6. Transmitter Output Signal Level Waveforms for RSDS *Note (1)*



Notes to Figure 11–6:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 11–8. RSDS Single Resistor Network *Note (1)*



Note to Figure 11–8:
(1) R_p = 100 Ω

RSDS Software Support

When designing for the RSDS I/O standard, assign the RSDS I/O standard to the I/O pins intended for RSDS in the Quartus® II software. Contact Altera Applications for reference designs.

mini-LVDS Standard Support in Cyclone II Devices

The mini-LVDS specification defines its use in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the Texas Instruments mini-LVDS Interface Specification and support the mini-LVDS output standard. Table 11–3 shows the mini-LVDS electrical characteristics for Cyclone II devices.

Table 11–3. mini-LVDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	300		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1125	1250	1375	mV
T_r / T_f	Transition time	20% to 80%			500	ps

Notes to Table 11–3:
(1) The V_{OD} specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

Section V. DSP

This section provides information for design and optimization of digital signal processing (DSP) functions and arithmetic operations using the embedded multiplier blocks.

This section includes the following chapter:

- Chapter 12, Embedded Multipliers in Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

device releases its nSTATUS pin after a reset time-out period (maximum of 40 µs). When the nSTATUS pin is released and pulled high by a pull-up resistor, the configuration device reconfigures the chain. If this option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 2 µs to restart configuration. The external system can pulse the nCONFIG pin if the pin is under system control rather than tied to V_{CC}.

Additionally, if the configuration device sends all of its data and then detects that the CONF_DONE pin has not transitioned high, it recognizes that the FPGA has not configured successfully. Enhanced configuration devices wait for 64 DCLK cycles after the last configuration bit was sent for the CONF_DONE pin to transition high. EPC2 devices wait for 16 DCLK cycles. After that, the configuration device pulls its OE pin low, which in turn drives the target device's nSTATUS pin low. If you turn on the **Auto-restart configuration after error** option in the Quartus II software, the target device resets and then releases its nSTATUS pin after a reset time-out period (maximum of 40 µs). When nSTATUS transitions high again, the configuration device reconfigures the FPGA.

For more information on configuration issues, see the *Debugging Configuration Problems* chapter of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site (**www.altera.com**).

Multiple Device PS Configuration Using a Configuration Device

You can use Altera enhanced configuration devices (EPC16, EPC8, and EPC4 devices) or EPC2 and EPC1 configuration devices to configure multiple Cyclone II devices in a PS configuration chain.

Figure 13–14 shows how to configure multiple devices with an enhanced configuration device. This circuit is similar to the configuration device circuit for a single device, except Cyclone II devices are cascaded for multiple device configuration.

feature. To use this feature successfully, set the MSEL[1..0] pins of the master Cyclone II device to select the AS configuration scheme or fast AS configuration scheme (see Table 13–1).

The Quartus II software version 4.1 and higher supports serial configuration device ISP through an FPGA JTAG interface using a JIC file.

The serial configuration device in-system programming through the Cyclone II JTAG interface has three stages, which are described in the following sections.

Loading the Serial Flash Loader Design

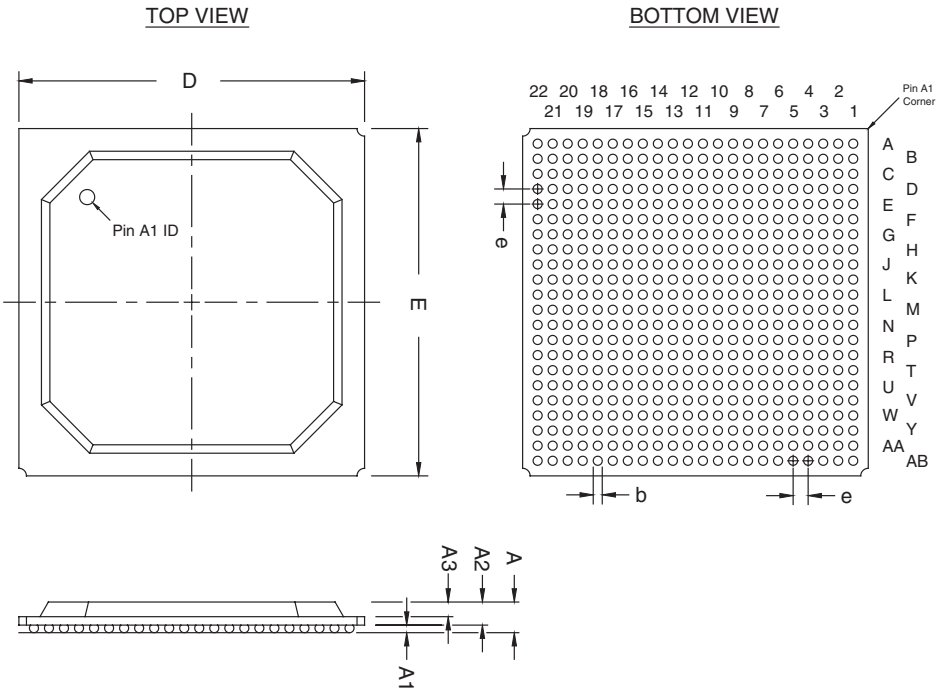
The serial flash loader design is a design inside the Cyclone II device that bridges the JTAG interface and AS interface inside the Cyclone II device using glue logic.

The intelligent host uses the JTAG interface to configure the master Cyclone II device with a serial flash loader design. The serial flash loader design allows the master Cyclone II device to control the access of four serial configuration device pins, also known as the Active Serial Memory Interface (ASMI) pins, through the JTAG interface. The ASMI pins are the serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS) pins.

If you configure a master Cyclone II device with a serial flash loader design, the master Cyclone II device can enter user mode even though the slave devices in the multiple device chain are not being configured. The master Cyclone II device can enter user mode with a serial flash loader design even though the CONF_DONE signal is externally held low by the other slave devices in chain. Figure 13–25 shows the JTAG configuration of a single Cyclone II device with a serial flash loader design.

Figure 15–5 shows a 484-pin FineLine BGA package outline.

Figure 15–5. 484-Pin FineLine BGA Package Outline



Document Revision History

Table 15–21 shows the revision history for this document.

Table 15–21. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.3	Added document revision history.	
November 2005 v2.1	Updated information throughout.	
July 2005 v2.0	Updated packaging information.	
November 2004 v1.0	Added document to the Cyclone II Device Handbook.	