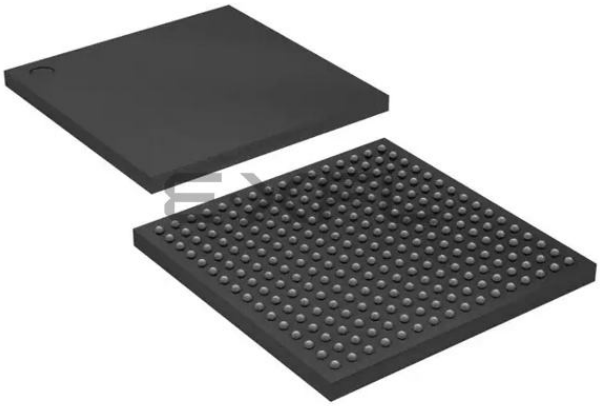


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Not For New Designs
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	158
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5f256c6n

- DSP intellectual property (IP) cores
- DSP Builder interface to The Mathworks Simulink and Matlab design environment
- DSP Development Kit, Cyclone II Edition

Cyclone II devices include a powerful FPGA feature set optimized for low-cost applications including a wide range of density, memory, embedded multiplier, and packaging options. Cyclone II devices support a wide range of common external memory interfaces and I/O protocols required in low-cost applications. Parameterizable IP cores from Altera and partners make using Cyclone II interfaces and protocols fast and easy.

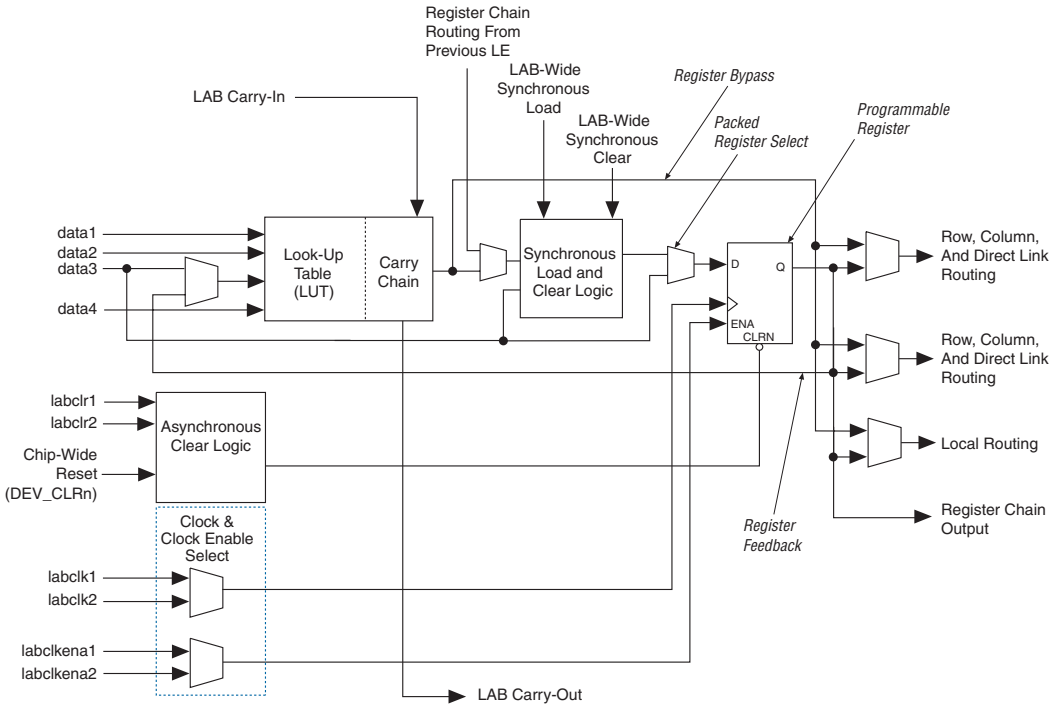
Features

The Cyclone II device family offers the following features:

- High-density architecture with 4,608 to 68,416 LEs
  - M4K embedded memory blocks
  - Up to 1.1 Mbits of RAM available without reducing available logic
  - 4,096 memory bits per block (4,608 bits per block including 512 parity bits)
  - Variable port configurations of ×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
  - True dual-port (one read and one write, two reads, or two writes) operation for ×1, ×2, ×4, ×8, ×9, ×16, and ×18 modes
  - Byte enables for data input masking during writes
  - Up to 260-MHz operation
- Embedded multipliers
  - Up to 150 18- × 18-bit multipliers are each configurable as two independent 9- × 9-bit multipliers with up to 250-MHz performance
  - Optional input and output registers
- Advanced I/O support
  - High-speed differential I/O standard support, including LVDS, RSDS, mini-LVDS, LVPECL, differential HSTL, and differential SSTL
  - Single-ended I/O standard support, including 2.5-V and 1.8-V, SSTL class I and II, 1.8-V and 1.5-V HSTL class I and II, 3.3-V PCI and PCI-X 1.0, 3.3-, 2.5-, 1.8-, and 1.5-V LVCMOS, and 3.3-, 2.5-, and 1.8-V LVTTL
  - Peripheral Component Interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 3.0* compliance for 3.3-V operation at 33 or 66 MHz for 32- or 64-bit interfaces
  - PCI Express with an external TI PHY and an Altera PCI Express ×1 Megacore® function

Figure 2–2 shows a Cyclone II LE.

Figure 2–2. Cyclone II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, clock, clock enable, and clear inputs. Signals that use the global clock network, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources, allowing the LUT to drive one output while the register drives another output. This feature, register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. When using register packing, the LAB-wide synchronous load control signal is not available. See "LAB Control Signals" on page 2–8 for more information.

Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT, providing another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

In addition to the three general routing outputs, the LEs within an LAB have register chain outputs. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 2–10 for more information on register chain connections.

LE Operating Modes

The Cyclone II LE operates in one of the following modes:

- Normal mode
- Arithmetic mode

Each mode uses LE resources differently. In each mode, six available inputs to the LE—the four data inputs from the LAB local interconnect, the LAB carry-in from the previous carry-chain LAB, and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus® II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–3). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. LEs in normal mode support packed registers and register feedback.

Devices Can Be Driven before Power-Up

You can drive signals into the I/O pins, dedicated input pins, and dedicated clock pins of Cyclone II devices before or during power-up or power-down without damaging the device. Cyclone II devices support any power-up or power-down sequence (V_{CCIO} and V_{CCINT}) to simplify system level design.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot-socketing situation, the Cyclone II device's output buffers are turned off during system power-up or power-down. The Cyclone II device also does not drive out until the device is configured and has attained proper operating conditions. The I/O pins are tri-stated until the device enters user mode with a weak pull-up resistor (R) to 3.3V. Refer to Figure 4–1 for more information.

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. The V_{CCIO} and V_{CCINT} must have monotonic rise to their steady state levels. (Refer to Figure 4–3 for more information.) The power supply ramp rates can range from 100 µs to 100 ms for non "A" devices. Both V_{CC} supplies must power down within 100 ms of each other to prevent I/O pins from driving out. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF. Cyclone II devices meet the following hot-socketing specification.

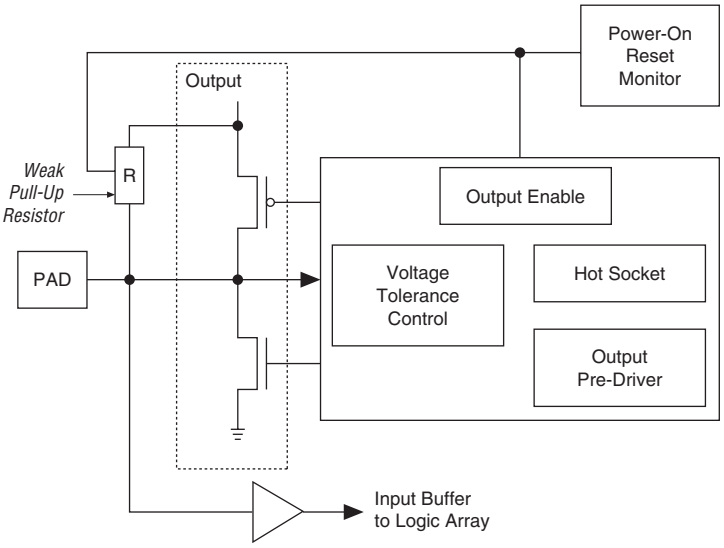
- The hot-socketing DC specification is $| I_{IOPIN} | < 300$ µA.
- The hot-socketing AC specification is $| I_{IOPIN} | < 8$ mA for 10 ns or less.

This specification takes into account the pin capacitance but not board trace and external loading capacitance. You must consider additional capacitance for trace, connector, and loading separately.

I_{IOPIN} is the current at any user I/O pin on the device. The DC specification applies when all V_{CC} supplies to the device are stable in the powered-up or powered-down conditions. For the AC specification, the peak current duration due to power-up transients is 10 ns or less.

A possible concern for semiconductor devices in general regarding hot socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins may be connected and driven by the active system before

Figure 4–1. Hot-Socketing Circuit Block Diagram for Cyclone II Devices



The POR circuit monitors V_{CCINT} voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} keeps the I/O pins from floating. The voltage tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

For more information, see the *DC Characteristics & Timing Specifications* chapter in Volume 1 of the *Cyclone II Device Handbook* for the value of the internal weak pull-up resistors.

Figure 4–2 shows a transistor level cross section of the Cyclone II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot socketing. The V_{PAD} leakage current charges the voltage tolerance control circuit capacitance.

5. DC Characteristics and Timing Specifications

CII51005-4.0

Operating Conditions

Cyclone® II devices are offered in commercial, industrial, automotive, and extended temperature grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the parameter values in this chapter apply to all Cyclone II devices. AC and DC characteristics are specified using the same numbers for commercial, industrial, and automotive grades. All parameters representing voltages are measured with respect to ground.

Tables 5–1 through 5–4 provide information on absolute maximum ratings.

Table 5–1. Cyclone II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Output supply voltage		–0.5	4.6	V
V_{CCA_PLL} [1..4]	PLL supply voltage		–0.5	1.8	V
V_{IN}	DC input voltage *(3)*	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	—	125	°C

Notes to Table 5–1:

(1) Conditions beyond those listed in this table cause permanent damage to a device. These are stress ratings only. Functional operation at these levels or any other conditions beyond those specified in this chapter is not implied. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effect on the device reliability.

(2) Refer to the *Operating Requirements for Altera Devices Data Sheet* for more information.

(3) During transitions, the inputs may overshoot to the voltage shown in Table 5–4 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transition, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5–8 shows the recommended operating conditions for user I/O pins with differential I/O standards.

Table 5–8. Recommended Operating Conditions for User I/O Pins Using Differential Signal I/O Standards

I/O Standard	V_{CCIO} (V)			V_{ID} (V) *(1)*			V_{ICM} (V)			V_{IL} (V)		V_{IH} (V)	
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	2.375	2.5	2.625	0.1	—	0.65	0.1	—	2.0	—	—	—	—
Mini-LVDS *(2)*	2.375	2.5	2.625	—	—	—	—	—	—	—	—	—	—
RSDS *(2)*	2.375	2.5	2.625	—	—	—	—	—	—	—	—	—	—
LVPECL *(3) (6)*	3.135	3.3	3.465	0.1	0.6	0.95	—	—	—	0	2.2	2.1	2.88
Differential 1.5-V HSTL class I and II *(4)*	1.425	1.5	1.575	0.2	—	V_{CCIO} + 0.6	0.68	—	0.9	—	V_{REF} – 0.20	V_{REF} + 0.20	—
Differential 1.8-V HSTL class I and II *(4)*	1.71	1.8	1.89	—	—	—	—	—	—	—	V_{REF} – 0.20	V_{REF} + 0.20	—
Differential SSTL-2 class I and II *(5)*	2.375	2.5	2.625	0.36	—	V_{CCIO} + 0.6	0.5 × V_{CCIO} – 0.2	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.2	—	V_{REF} – 0.35	V_{REF} + 0.35	—
Differential SSTL-18 class I and II *(5)*	1.7	1.8	1.9	0.25	—	V_{CCIO} + 0.6	0.5 × V_{CCIO} – 0.2	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.2	—	V_{REF} – 0.25	V_{REF} + 0.25	—

Notes to Table 5–8:

(1) Refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook* for measurement conditions on V_{ID}.

(2) The RSDS and mini-LVDS I/O standards are only supported on output pins.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(4) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

(5) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(6) The LVPECL clock inputs are powered by V_{CCINT} and support all V_{CCIO} settings. However, it is recommended to connect V_{CCIO} to typical value of 3.3V.

Table 5–19. M4K Block Internal Timing Microparameters (Part 2 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KBEH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATAASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATAAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KADDRASU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KADDRAH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATABSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KDATABH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KRADDRBSU	35	—	46	—	46	—	ps
	—	—	40	—	46	—	ps
TM4KRADDRBH	234	—	267	—	267	—	ps
	—	—	250	—	267	—	ps
TM4KDATACO1	466	724	445	826	445	930	ps
	—	—	466	—	466	—	ps
TM4KDATACO2	2345	3680	2234	4157	2234	4636	ps
	—	—	2345	—	2345	—	ps
TM4KCLKH	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps
TM4KCLKL	1923	—	2769	—	2769	—	ps
	—	—	2307	—	2769	—	ps

Table 5–23. EP2C8/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.179	–0.189	0.089	0.047	0.045	0.055	ns

Notes to Table 5–23:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–24. EP2C8/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.256	1.314	2.270	2.416	2.596	2.606	ns
t_{COUT}	1.258	1.316	2.286	2.429	2.604	2.614	ns
t_{PLLCIN}	–0.276	–0.294	–0.08	–0.134	–0.152	–0.142	ns
$t_{PLLCOUT}$	–0.274	–0.292	–0.064	–0.121	–0.144	–0.134	ns

Notes to Table 5–24:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C15A Clock Timing Parameters

Tables 5–25 and 5–26 show the clock timing parameters for EP2C15A devices.

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

Phase-Shifting Implementation

Cyclone II devices use fine or coarse phase shifts for clock delays because they are more efficient than delay elements and are independent of process, voltage, and temperature.

Phase shift is implemented by using a combination of the VCO phase output and the counter starting time. The VCO phase taps and counter starting time are independent of process, voltage, and temperature. The VCO phase taps allow you to phase shift the Cyclone II PLL output clocks with fine resolution. The counter starting time allows you to phase shift the Cyclone II PLL output clocks with coarse resolution.

Fine-resolution phase shifting is implemented using any of the eight VCO phases for the output counters (`c[2..0]`) or the feedback counter (*m*) reference clock. This provides the finest resolution for phase shift. The minimum delay time that may be inserted using this method is defined by the equation:

$$\Delta t_{FINE} = \frac{1}{8} t_{VCO} = \frac{1}{8 \times f_{VCO}} = \frac{n}{8 \times m \times f_{IN}}$$

f_{IN} is input reference clock frequency.

For example, if f_{IN} is 100 MHz, *n* is 1 and *m* is 8, then f_{VCO} is 800 MHz and Δt is 156.25 ps. This delay time is defined by the PLL operating frequency which is governed by the reference clock and the counter settings.

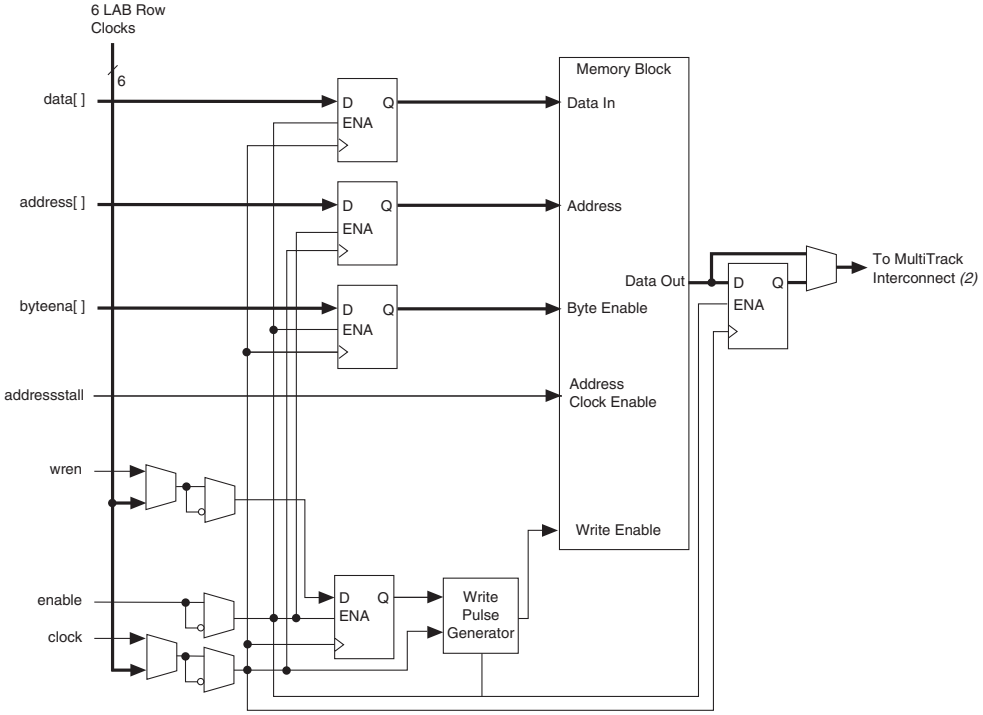
The second way to implement phase shifts is by delaying the start of the *m* and post-scale counters for a predetermined number of counter clocks. This delay time may be expressed as:

$$\Delta t_{COARSE} = \frac{S - 1}{f_{VCO}} = \frac{(S - 1) \times n}{m \times f_{IN}}$$

where S is the value set for the counter starting time. The counter starting time is called the **Initial** setting in the PLL Usage section of the compilation report in the Quartus II software.

Figure 7–8 shows an example of delay insertion using these two methods. The eight phases from the VCO are shown and labeled for reference. For this example, `OUTCLK0` is based off the 0° phase from the VCO and has the S value for the counter set to 1. It is divided by 4 (two VCO clocks for high time and two VCO clocks for low time). `OUTCLK1` is based off the 135° phase tap from the VCO and also has the S value for the counter set to 1. It is also divided by 4. In this case, the two clocks are offset by three

Figure 8–20. Cyclone II Single-Clock Mode in Single-Port Mode *Notes (1), (2)*



Notes to Figure 8–20:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in Volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

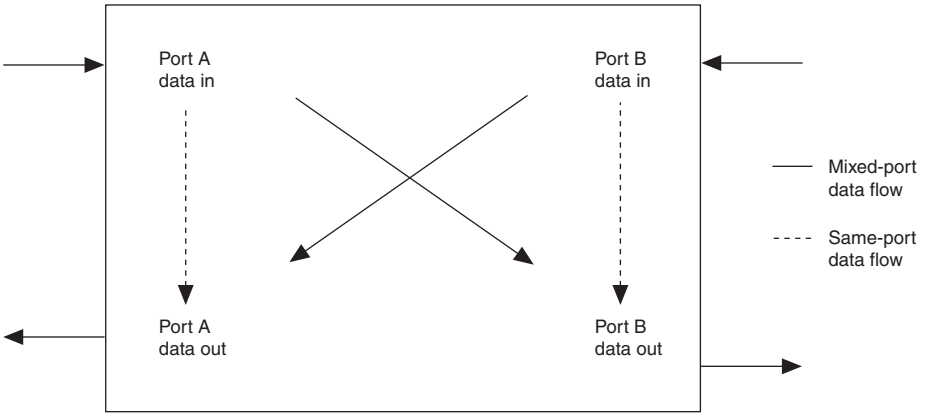
Power-Up Conditions & Memory Initialization

The Cyclone II memory block outputs always power-up to zero, regardless of whether the output registers are used or bypassed. Even if an MIF pre-loads the contents of the memory block, the outputs still power up cleared. For example, if address 0 is pre-initialized to `FF`, M4K blocks power up with the output at `00`. A subsequent read after power up from address 0 outputs the pre-initialized value of `FF`.

Read-During-Write Operation at the Same Address

The "Same-Port Read-During-Write Mode" and "Mixed-Port Read-During-Write Mode" sections describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two read-during-write data flows: same-port and mixed-port. Figure 8–21 shows the difference between these flows.

Figure 8–21. Cyclone II Read-During-Write Data Flow



Same-Port Read-During-Write Mode

For read-during-write operation of a single-port RAM or the same port of a true dual-port RAM, the new data is available on the rising edge of the same clock cycle on which it was written. Figure 8–22 shows a sample functional waveform. When using byte enables in true dual-port RAM mode, the outputs for the masked bytes on the same port are unknown (see Figure 8–2 on page 8–6). The non-masked bytes are read out as shown in Figure 8–22.

I/O Termination

The majority of the Cyclone II I/O standards are single-ended, non-voltage-referenced I/O standards and, as such, the following I/O standards do not specify a recommended termination scheme:

- 3.3-V LVTTL and LVCMOS
- 2.5-V LVTTL and LVCMOS
- 1.8-V LVTTL and LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI and PCI-X

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

For more information on termination for voltage-referenced I/O standards, refer to "Supported I/O Standards" on page 10–1.

Differential I/O Standard Termination

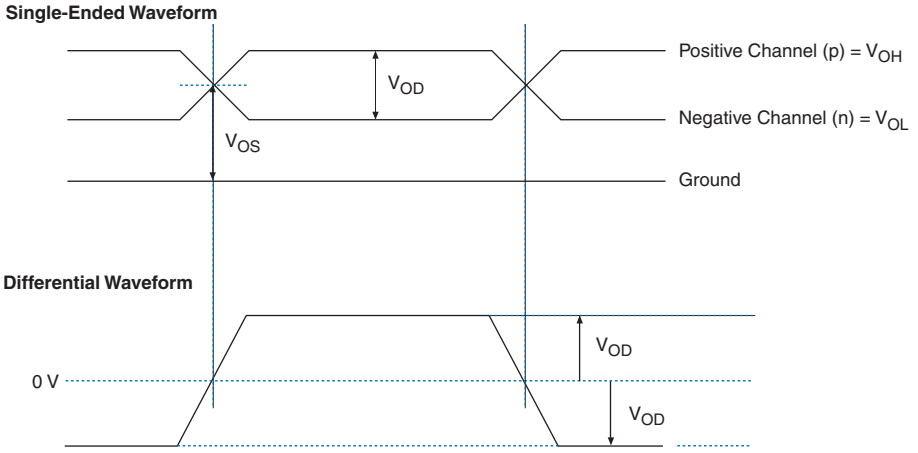
Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus.

Cyclone II devices support differential I/O standards LVDS, RSDS, and mini-LVDS, and differential LVPECL.

For more information on termination for differential I/O standards, refer to "Supported I/O Standards" on page 10–1.

Figure 11–9 shows the mini-LVDS receiver and transmitter signal waveforms.

Figure 11–9. Transmitter Output Signal Level Waveforms for mini-LVDS *Note (1)*



Note to Figure 11–9:
(1) The V_{OD} specifications apply at the resistor network output.

Designing with mini-LVDS

Similar to RSDS, Cyclone II devices support the mini-LVDS output standard using the LVDS I/O buffer types. For transmitters, the LVDS output buffer can be used with the external resistor network shown in Figure 11–10. The resistor values chosen should satisfy the equation on page 11-8.

data A signal through a register and send the data B signal directly to the multiplier). The following control signals are available to each register within the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers within a single embedded multiplier are fed by the same clock, clock enable, or asynchronous clear signal.

Multiplier Stage

The multiplier stage supports 9 × 9 or 18 × 18 multipliers as well as other smaller multipliers in between these configurations. See "Operational Modes" on page 12–6 for details. Depending on the data width or operational mode of the multiplier, a single embedded multiplier can perform one or two multiplications in parallel.

Each multiplier operand can be a unique signed or unsigned number. Two signals, `signa` and `signb`, control whether a multiplier's input is a signed or unsigned value. If the `signa` signal is high, the data A operand is a signed number, and if the `signa` signal is low, the data A operand is an unsigned number. Table 12–3 shows the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

Table 12–3. Multiplier Sign Representation

Data A		Data B		Result
signa Value	Logic Level	signb Value	Logic Level	
Unsigned	Low	Unsigned	Low	Unsigned
Unsigned	Low	Signed	High	Signed
Signed	High	Unsigned	Low	Signed
Signed	High	Signed	High	Signed

There is only one `signa` and one `signb` signal for each embedded multiplier. The `signa` and `signb` signals can be changed dynamically to modify the sign representation of the input operands at run time. You can send the `signa` and `signb` signals through a dedicated input register. The multiplier offers full precision regardless of the sign representation.

For more information on configuration issues, see the *Debugging Configuration Problems* chapter of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site (**www.altera.com**).

Multiple Device AS Configuration

You can configure multiple Cyclone II devices using a single serial configuration device. You can cascade multiple Cyclone II devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. Connect the nCE pin of the first device in the chain to ground and connect the nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO signal high to its V_{CCIO} level to help the internal weak pull-up resistor. When the first device captures all of its configuration data from the bitstream, it transitions its nCEO pin low, initiating the configuration of the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in chain is a Cyclone II device.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the device is in a chain, and the nCEO pin is connected to the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O pin after configuration. The software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

The first Cyclone II device in the chain is the configuration master and controls the configuration of the entire chain. Select the AS configuration scheme for the first Cyclone II device and the PS configuration scheme for the remaining Cyclone II devices (configuration slaves). Any other Altera® device that supports PS configuration can also be part of the chain as a configuration slave. In a multiple device chain, the nCONFIG, nSTATUS, CONF_DONE, DCLK, and DATA0 pins of each device in the chain are connected (see Figure 13–4). Figure 13–4 shows the pin connections for this setup.

Programming Serial Configuration Devices

Serial configuration devices are non-volatile, flash-memory-based devices. You can program these devices in-system using the USB-Blaster™ or ByteBlaster™ II download cable. Alternatively, you can program them using the Altera Programming Unit (APU), supported third-party programmers, or a microprocessor with the SRunner software driver.

You can use the AS programming interface to program serial configuration devices in-system. During in-system programming, the download cable disables FPGA access to the AS interface by driving the `nCE` pin high. Cyclone II devices are also held in reset by pulling the `nCONFIG` signal low. After programming is complete, the download cable releases the `nCE` and `nCONFIG` signals, allowing the pull-down and pull-up resistor to drive GND and V_{CC}, respectively. Figure 13–7 shows the download cable connections to the serial configuration device.

For more information on the USB-Blaster download cable, see the *USB-Blaster USB Port Download Cable Data Sheet*. For more information on the ByteBlaster II cable, see the *ByteBlaster II Download Cable Data Sheet*.

A device operating in JTAG mode uses the TDI, TDO, TMS, and TCK pins. The TCK pin has a weak internal pull-down resistor while the other JTAG input pins, TDI and TMS, have weak internal pull-up resistors. All user I/O pins are tri-stated during JTAG configuration. Table 13–9 explains each JTAG pin's function.

Table 13–9. Dedicated JTAG Pins

Pin Name	Pin Type	Description
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to GND.

The TDO output is powered by the V_{CCIO} power supply. If V_{CCIO} is tied to 3.3-V, both the I/O pins and the JTAG TDO port drive at 3.3-V levels.

Table 14–2 describes the capture and update register capabilities of all types of boundary-scan cells within Cyclone II devices.

Table 14–2. Cyclone II Device Boundary Scan Cell Descriptions *Note (1)*

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Dedicated clock input	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to clock network or logic array
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to control logic
Dedicated bidirectional (open drain) *(4)*	0	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to configuration control
Dedicated bidirectional *(5)*	OUTJ	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	OUTJ drives to output buffer

Notes to Table 14–2:

(1) TDI, TDO, TMS, TCK, all V_{CC} and GND pin types do not have BSCs.
(2) N.C.: no connect.
(3) This includes nCONFIG, MSEL0, MSEL1, DATA0, and nCE pins and DCLK (when not used in Active Serial mode).
(4) This includes CONF_DONE and nSTATUS pins.
(5) This includes DCLK (when not used in Active Serial mode).

IEEE Std. 1149.1 BST Operation Control

Cyclone II devices implement the following IEEE Std. 1149.1 BST instructions: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE, USERCODE, CLAMP, and HIGHZ. The BST instruction length is 10 bits. These instructions are described later in this chapter.

For summaries of the BST instructions and their instruction codes, see the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

The IEEE Std. 1149.1 test access port (TAP) controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 14–5 shows the TAP controller state machine.

Figure 15–1 shows a 144-pin TQFP package outline.

Figure 15–1. 144-Pin TQFP Package Outline