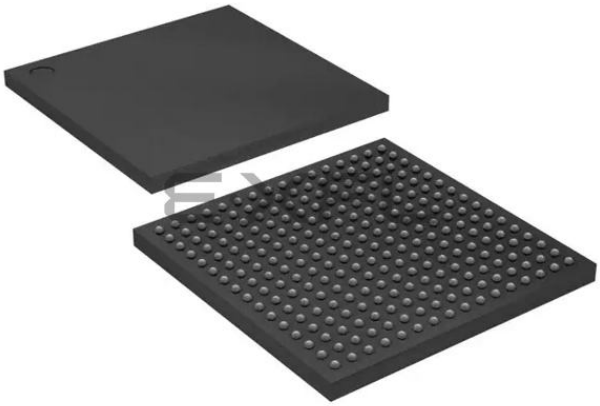

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	158
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5f256c7

Section I. Cyclone II Device Family Data Sheet

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. It contains the required PCB layout guidelines, device pin tables, and package specifications.

This section includes the following chapters:

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Cyclone II devices are available in up to three speed grades: –6, –7, and –8, with –6 being the fastest. Table 1–4 shows the Cyclone II device speed-grade offerings.

Table 1–4. Cyclone II Device Speed Grades

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA	896-Pin FineLine BGA
EP2C5 *(1)*	–6, –7, –8	–7, –8	—	–6, –7, –8	—	—	—	—
EP2C8	–6, –7, –8	–7, –8	—	–6, –7, –8	—	—	—	—
EP2C8A *(2)*	—	—	—	–8	—	—	—	—
EP2C15A	—	—	—	–6, –7, –8	–6, –7, –8	—	—	—
EP2C20	—	—	–8	–6, –7, –8	–6, –7, –8	—	—	—
EP2C20A *(2)*	—	—	—	–8	–8	—	—	—
EP2C35	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	—
EP2C50	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	—
EP2C70	—	—	—	—	—	—	–6, –7, –8	–6, –7, –8

Notes to Table 1–4:

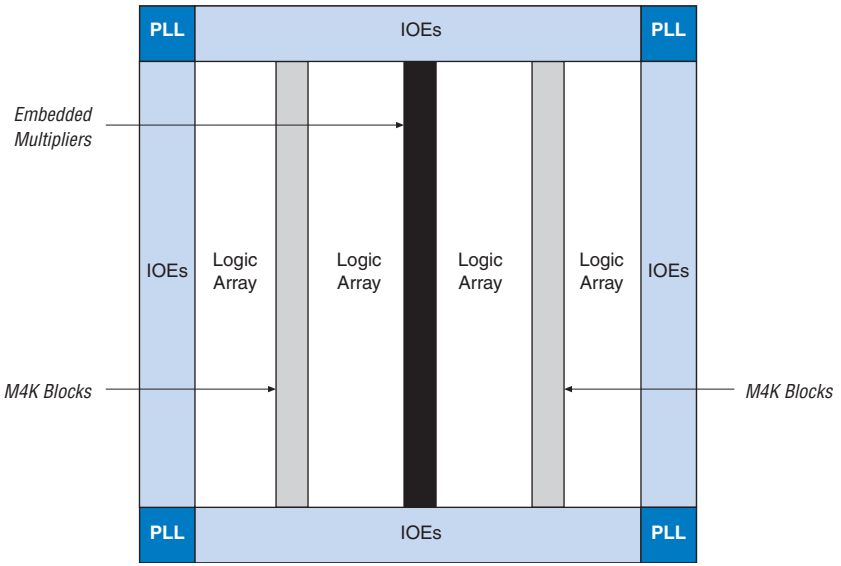
(1) The EP2C5 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. Refer to the Cyclone II section in the *Automotive-Grade Device Handbook* for detailed information.

(2) EP2C8A and EP2C20A are only available in industrial grade.

phase-align double data rate (DDR) signals) provide interface support for external memory devices such as DDR, DDR2, and single data rate (SDR) SDRAM, and QDRII SRAM devices at up to 167 MHz.

Figure 2–1 shows a diagram of the Cyclone II EP2C20 device.

Figure 2–1. Cyclone II EP2C20 Device Block Diagram



The number of M4K memory blocks, embedded multiplier blocks, PLLs, rows, and columns vary per device.

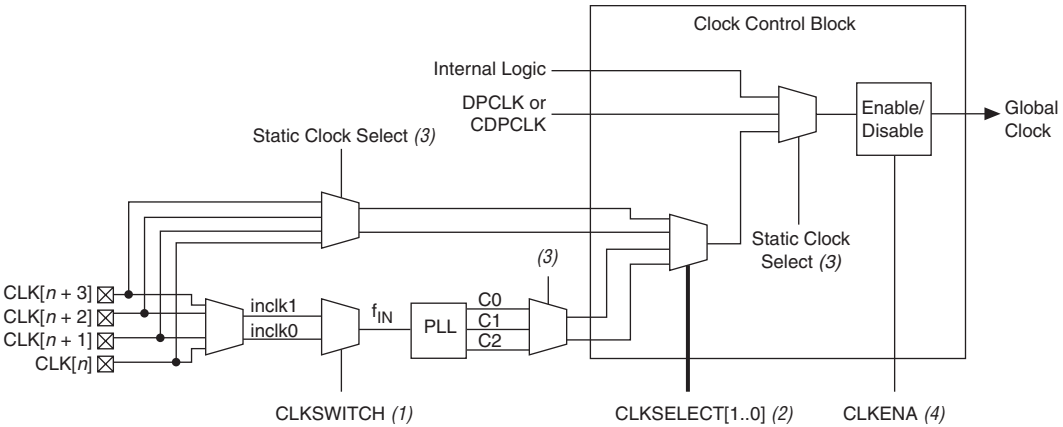
Logic Elements

The smallest unit of logic in the Cyclone II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE features:

- A four-input look-up table (LUT), which is a function generator that can implement any function of four variables
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and direct link interconnects
- Support for register packing
- Support for register feedback

Of the sources listed, only two clock pins, two PLL clock outputs, one DPCLK pin, and one internally-generated signal are chosen to drive into a clock control block. Figure 2–13 shows a more detailed diagram of the clock control block. Out of these six inputs, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of DPCLK and the signal from internal logic.

Figure 2–13. Clock Control Block



Notes to Figure 2–13:

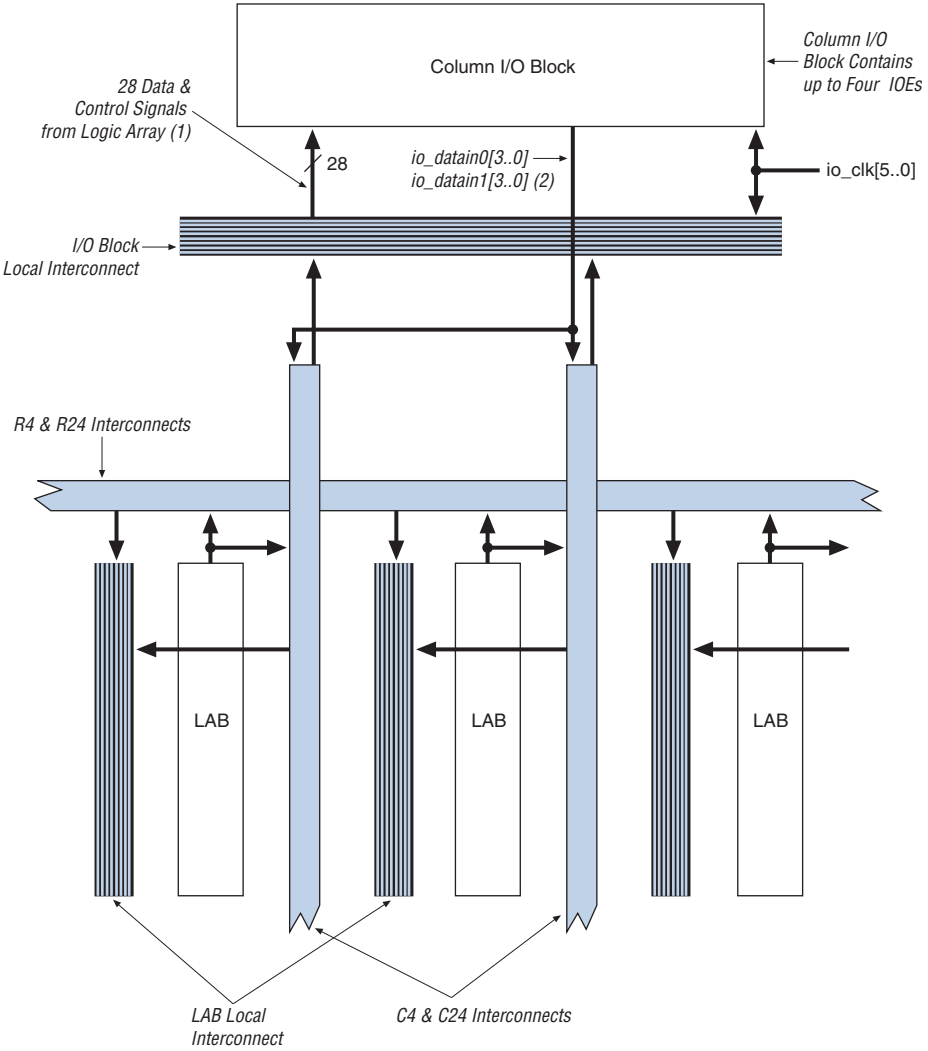
(1) The CLKSWITCH signal can either be set through the configuration file or it can be dynamically set when using the manual PLL switchover feature. The output of the multiplexer is the input reference clock (f_{IN}) for the PLL.

(2) The CLKSELECT[1..0] signals are fed by internal logic and can be used to dynamically select the clock source for the global clock network when the device is in user mode.

(3) The static clock select signals are set in the configuration file and cannot be dynamically controlled when the device is in user mode.

(4) Internal logic can be used to enabled or disabled the global clock network in user mode.

Figure 2–22. Column I/O Block Connection to the Interconnect



Notes to Figure 2–22:

(1) The 28 data and control signals consist of four data out lines, `io_dataout[3..0]`, four output enables, `io_coe[3..0]`, four input clock enables, `io_cce_in[3..0]`, four output clock enables, `io_cce_out[3..0]`, four clocks, `io_cclk[3..0]`, four asynchronous clear signals, `io_caclr[3..0]`, and four synchronous clear signals, `io_csclr[3..0]`.

(2) Each of the four IOEs in the column I/O block can have two `io_datain` (combinational or registered) inputs.

I/O Banks

The I/O pins on Cyclone II devices are grouped together into I/O banks and each bank has a separate power bus. EP2C5 and EP2C8 devices have four I/O banks (see Figure 2–28), while EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices have eight I/O banks (see Figure 2–29). Each device I/O pin is associated with one I/O bank. To accommodate voltage-referenced I/O standards, each Cyclone II I/O bank has a VREF bus. Each bank in EP2C5, EP2C8, EP2C15, EP2C20, EP2C35, and EP2C50 devices supports two VREF pins and each bank of EP2C70 supports four VREF pins. When using the VREF pins, each VREF pin must be properly connected to the appropriate voltage level. In the event these pins are not used as VREF pins, they may be used as regular I/O pins.

The top and bottom I/O banks (banks 2 and 4 in EP2C5 and EP2C8 devices and banks 3, 4, 7, and 8 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support all I/O standards listed in Table 2–17, except the PCI/PCI-X I/O standards. The left and right side I/O banks (banks 1 and 3 in EP2C5 and EP2C8 devices and banks 1, 2, 5, and 6 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support I/O standards listed in Table 2–17, except SSTL-18 class II, HSTL-18 class II, and HSTL-15 class II I/O standards. See Table 2–17 for a complete list of supported I/O standards.

The top and bottom I/O banks (banks 2 and 4 in EP2C5 and EP2C8 devices and banks 3, 4, 7, and 8 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support DDR2 memory up to 167 MHz/333 Mbps and QDR memory up to 167 MHz/668 Mbps. The left and right side I/O banks (1 and 3 of EP2C5 and EP2C8 devices and 1, 2, 5, and 6 of EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) only support SDR and DDR SDRAM interfaces. All the I/O banks of the Cyclone II devices support SDR memory up to 167 MHz/167 Mbps and DDR memory up to 167 MHz/333 Mbps.

DDR2 and QDRII interfaces may be implemented in Cyclone II side banks if the use of class I I/O standard is acceptable.

standards (e.g., SSTL-2) independently. If an I/O bank does not use voltage-referenced standards, the VREF pins are available as user I/O pins.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs. Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value.

MultiVolt I/O Interface

The Cyclone II architecture supports the MultiVolt I/O interface feature, which allows Cyclone II devices in all packages to interface with systems of different supply voltages. Cyclone II devices have one set of V_{CC} pins (VCCINT) that power the internal device logic array and input buffers that use the LVPECL, LVDS, HSTL, or SSTL I/O standards. Cyclone II devices also have four or eight sets of VCC pins (VCCIO) that power the I/O output drivers and input buffers that use the LVTTL, LVCMOS, or PCI I/O standards.

The Cyclone II VCCINT pins must always be connected to a 1.2-V power supply. If the V_{CCINT} level is 1.2 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V systems. Table 2–20 summarizes Cyclone II MultiVolt I/O support.

Table 2–20. Cyclone II MultiVolt I/O Support (Part 1 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
1.5	✓	✓	✓ *(2)*	✓ *(2)*	✓			
1.8	✓ *(4)*	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓		
2.5			✓	✓	✓ *(5)*	✓ *(5)*	✓	

4. Hot Socketing & Power-On Reset

CII51004-3.1

Introduction

Cyclone® II devices offer hot socketing (also known as hot plug-in, hot insertion, or hot swap) and power sequencing support without the use of any external devices. You can insert or remove a Cyclone II board in a system during system operation without causing undesirable effects to the board or to the running system bus.

The hot-socketing feature lessens the board design difficulty when using Cyclone II devices on printed circuit boards (PCBs) that also contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices. With the Cyclone II hot-socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Cyclone II hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

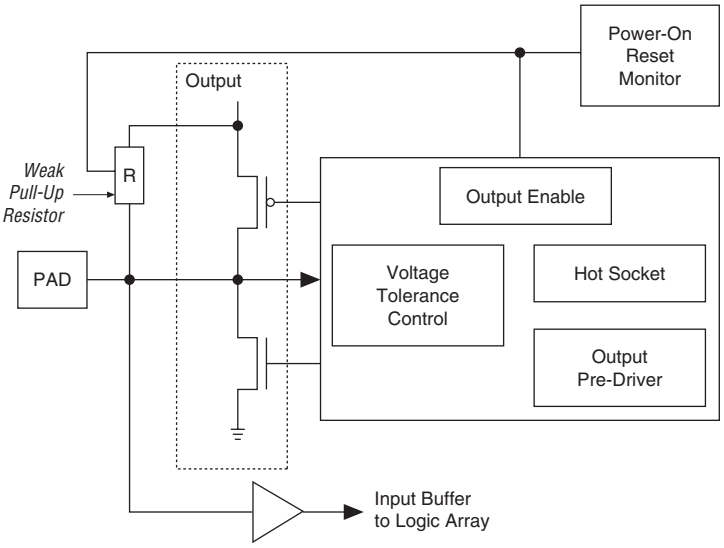
This chapter also discusses the power-on reset (POR) circuitry in Cyclone II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Cyclone II Hot-Socketing Specifications

Cyclone II devices offer hot-socketing capability with all three features listed above without any external components or special design requirements. The hot-socketing feature in Cyclone II devices offers the following:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.

Figure 4–1. Hot-Socketing Circuit Block Diagram for Cyclone II Devices



The POR circuit monitors V_{CCINT} voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} keeps the I/O pins from floating. The voltage tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

For more information, see the *DC Characteristics & Timing Specifications* chapter in Volume 1 of the *Cyclone II Device Handbook* for the value of the internal weak pull-up resistors.

Figure 4–2 shows a transistor level cross section of the Cyclone II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot socketing. The V_{PAD} leakage current charges the voltage tolerance control circuit capacitance.

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 2 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVCMOS	4 mA	250	210	170	250	210	170	250	210	170
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	310	260	210	310	260	210	310	260	210
	16 mA	320	270	220	—	—	—	—	—	—
	20 mA	350	290	240	—	—	—	—	—	—
	24 mA	370	310	250	—	—	—	—	—	—
2.5V	4 mA	180	150	120	180	150	120	180	150	120
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	440	370	300	—	—	—	—	—	—
	16 mA	450	405	350	—	—	—	—	—	—
1.8V	2 mA	120	100	80	120	100	80	120	100	80
	4 mA	180	150	120	180	150	120	180	150	120
	6 mA	220	180	150	220	180	150	220	180	150
	8 mA	240	200	160	240	200	160	240	200	160
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	350	290	240	350	290	240	350	290	240
1.5V	2 mA	80	60	50	80	60	50	80	60	50
	4 mA	130	110	90	130	110	90	130	110	90
	6 mA	180	150	120	180	150	120	180	150	120
	8 mA	230	190	160	—	—	—	—	—	—
SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
SSTL_18_CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—

Single-Clock Mode

Cyclone II memory blocks support single-clock mode for true dual-port, simple dual-port, and single-port memory. In this mode, a single clock, together with a clock enable, controls all registers of the memory block. This mode does not support asynchronous clear signals for the registers. Figures 8–18 through 8–20 show the memory block in single-clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

DQS pin to the DQ LE register does not necessarily match the delay from the DQ pin to the DQ LE register. Therefore, you must adjust the clock delay control circuitry to compensate for this difference in delays.

DQS Postamble

For external memory interfaces that use a bidirectional read strobe, such as DDR and DDR2 SDRAM, the DQS signal is low before going to or coming from the high-impedance state (see Figure 9–1). The state where DQS is low just after high-impedance is called the preamble and the state where DQS is low just before it goes to high-impedance is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR and DDR2 SDRAM. If the Cyclone II device or the DDR/DDR2 SDRAM device does not drive the DQ and DQS pins, the signals go to a high-impedance state. Because a pull-up resistor terminates both DQ and DQS to V_{TT} (1.25 V for SSTL-2 and 0.9 V for SSTL-18), the effective voltage on the high-impedance line is either 1.25 V or 0.9 V. According to the JEDEC JESD8-9 specification for SSTL-2 I/O standard and the JESD8-15A specification for SSTL-18 I/O standard, this is an indeterminate logic level, and the input buffer can interpret this as either a logic high or logic low. If there is any noise on the DQS line, the input buffer may interpret that noise as actual strobe edges.

Cyclone II devices have non-dedicated logic that can be configured to prevent a false edge trigger at the end of the DQS postamble. Each Cyclone II DQS signal is connected to postamble logic that consists of a D flip flop (see Figure 9–9). This register is clocked by the shifted DQS signal. Its input is connected to ground. The controller needs to include extra logic to tell the reset signal to release the preset signal on the falling DQS edge at the start of the postamble. This disables any glitches that happen right after the postamble. This postamble logic is automatically implemented by the Altera MegaCore DDR/DDR2 SDRAM Controller in the LE register as part of the open-source datapath.

For information about the I/O standards supported for external memory applications, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(1)*	*(1)*	*(1)*
PCI and PCI-X *(2)*	Single ended	3.3 V	3.3 V	—	—	✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(3)*	*(4)*	2.5 V	—	—	—	✓	—
		2.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential SSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—		✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—

- Cyclone II FPGA (EP2C15 or larger)
- Altera PCI Express Compiler ×1 MegaCore® function
- External PCI Express transceiver/PHY

2.5-V LVTTL (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVTTL.

2.5-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVCMOS.

SSTL-2 Class I and II (EIA/JEDEC Standard JESD8-9A)

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operations in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of $-0.3\ V \leq V_I \leq V_{CCIO} + 0.3\ V$. SSTL-2 requires a V_{REF} value of 1.25 V and a V_{TT} value of 1.25 V connected to the termination resistors (refer to Figures 10–1 and 10–2).

Software Support

Altera provides two methods for implementing multipliers in your design using embedded multiplier resources: instantiation and inference. Both methods use the following three Quartus II megafunctions:

- `lpm_mult`
- `altmult_add`
- `altmult_accum`

You can instantiate the megafunctions in the Quartus II software to use the embedded multipliers. You can use the `lpm_mult` and `altmult_add` megafunctions to implement multipliers. Additionally, you can use the `altmult_add` megafunctions to implement multiplier-adders where the embedded multiplier is used to implement the multiply function and the adder function is implemented in LEs. The `altmult_accum` megafunction implements multiply accumulate functions where the embedded multiplier implements the multiplier and the accumulator function is implemented in LEs.

See Quartus II On-Line Help for instructions on using the megafunctions and the MegaWizard Plug-In Manager.

For information on our complete DSP Design and Intellectual Property offerings, see **www.Altera.com**.

You can also infer the megafunctions by creating an HDL design and synthesize it using Quartus II integrated synthesis or a third-party synthesis tool that recognizes and infers the appropriate multiplier megafunction. Using either method, the Quartus II software maps the multiplier functionality to the embedded multipliers during compilation.

See the Synthesis section in Volume 1 of the ***Quartus II Handbook*** for more information.

Conclusion

The Cyclone II device embedded multipliers are optimized to support multiplier-intensive DSP applications such as FIR filters, FFT functions and encoders. These embedded multipliers can be configured to implement multipliers of various bit widths up to 18-bits to suit a particular application resulting in efficient resource utilization and improved performance and data throughput. The Quartus II software, together with the LeonardoSpectrum and Synplify software provide a complete and easy-to-use flow for implementing multiplier functions using embedded multipliers.

If your design has multiple Cyclone II devices of the same density and package that contain the same configuration data, connect the nCE inputs to GND and leave the nCEO pins floating. You can also use the nCEO pin as a user I/O pin. Connect the configuration device nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE pins to each Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Make sure that the DCLK and DATA lines are buffered for every fourth device. All devices start and complete configuration at the same time. Figure 13–16 shows multiple device PS configuration when the Cyclone II devices are receiving the same configuration data.

operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

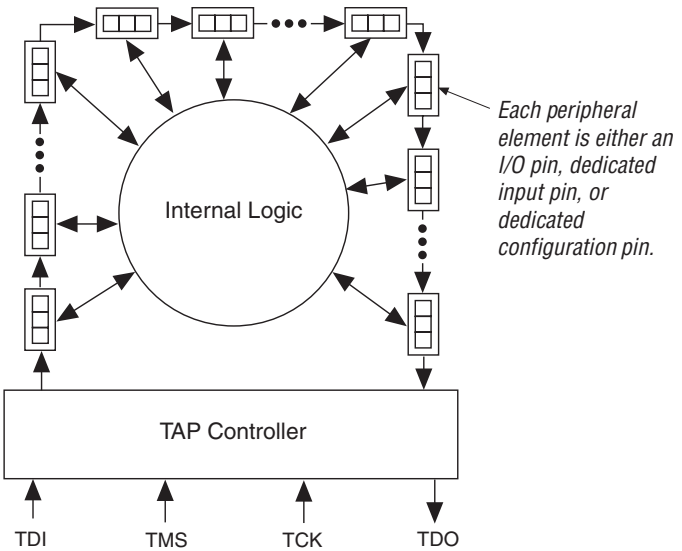
IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are associated with Cyclone II I/O pins. You can use the boundary-scan register to test external pin connections or to capture internal data.

See the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook* for the Cyclone II device boundary-scan register lengths.

Figure 14–3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 14–3. Boundary-Scan Register



Boundary-Scan Cells of a Cyclone II Device I/O Pin

The Cyclone II device 3-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data via the OUTJ and OEJ signals, and connect

to external device data via the PIN_IN signal, while the update registers connect to external data through the PIN_OUT and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 14–4 shows the Cyclone II device's user I/O boundary-scan cell.

Figure 14–4. Cyclone II Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry

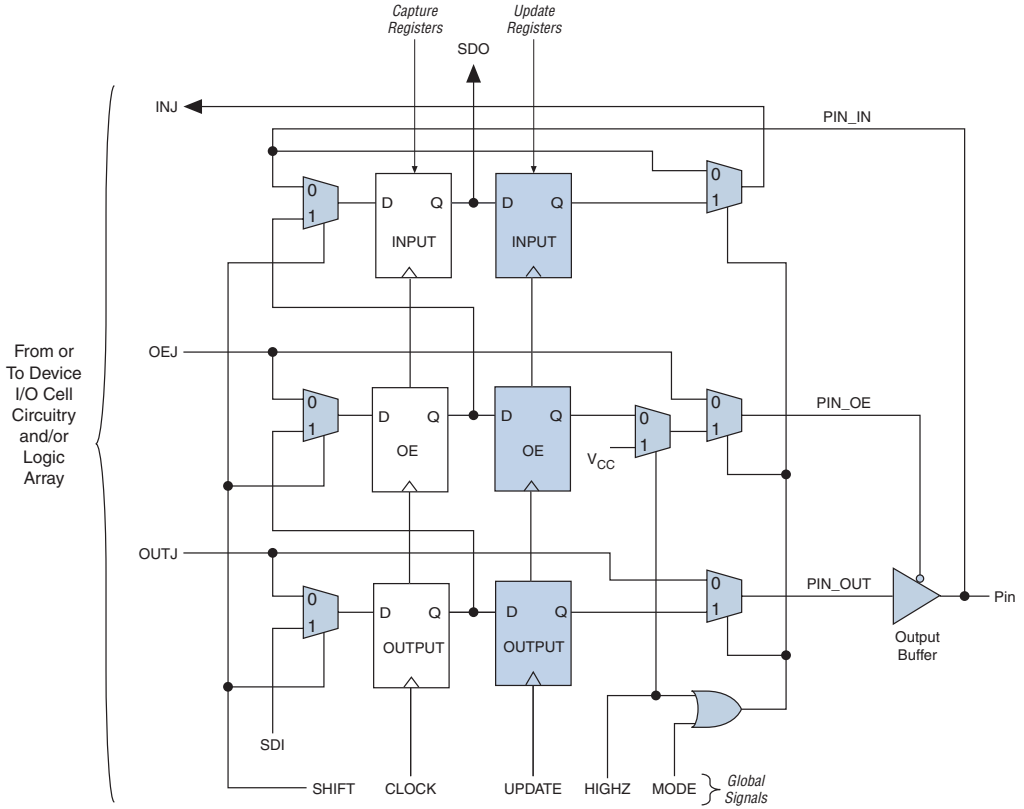


Figure 14–5. IEEE Std. 1149.1 TAP Controller State Machine

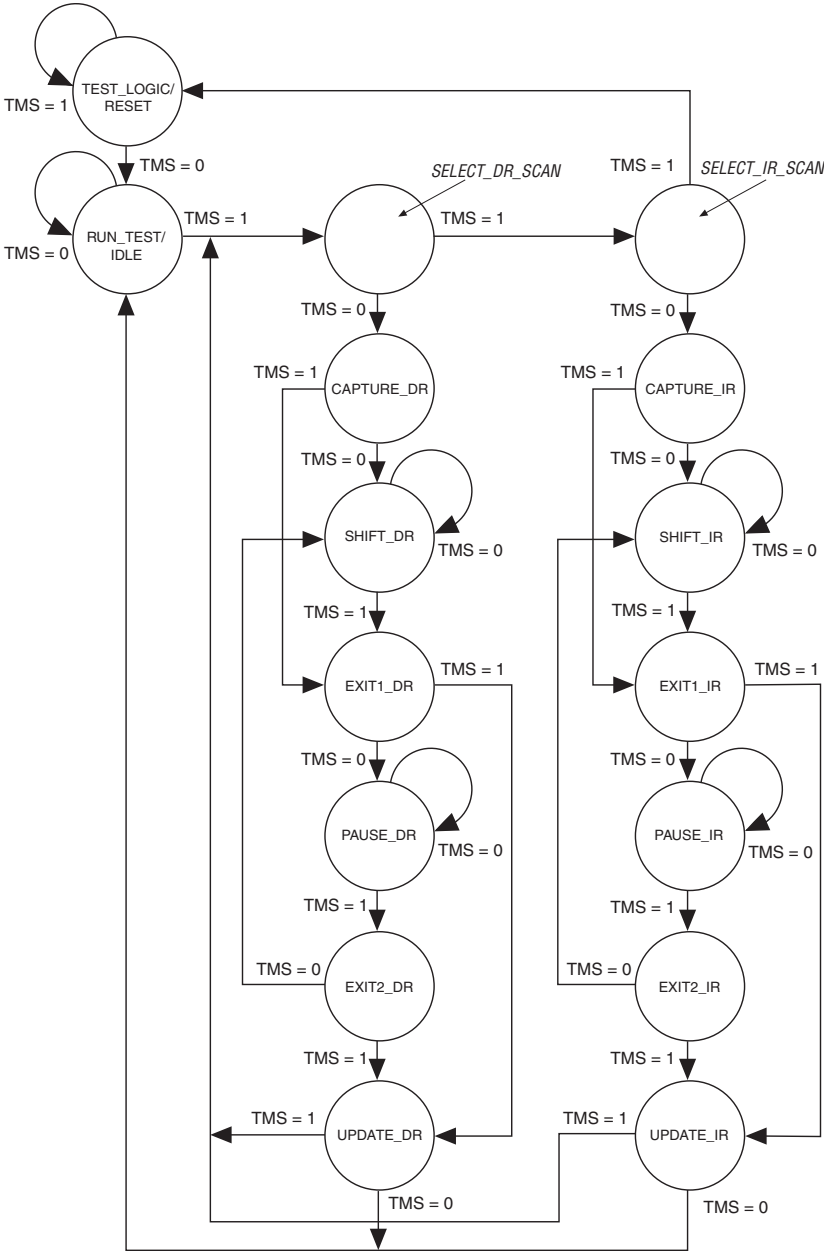


Figure 15–1 shows a 144-pin TQFP package outline.

Figure 15–1. 144-Pin TQFP Package Outline