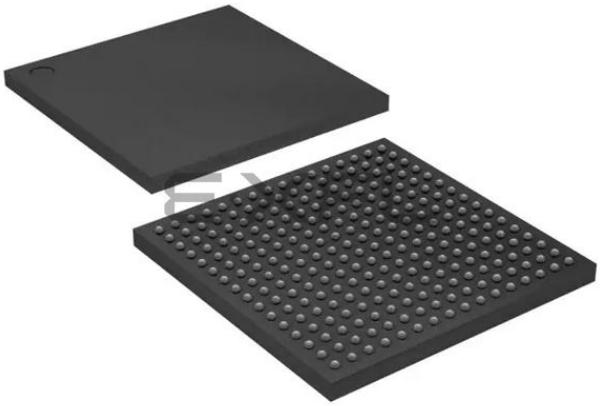


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	158
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5f256c8n

- DSP intellectual property (IP) cores
- DSP Builder interface to The Mathworks Simulink and Matlab design environment
- DSP Development Kit, Cyclone II Edition

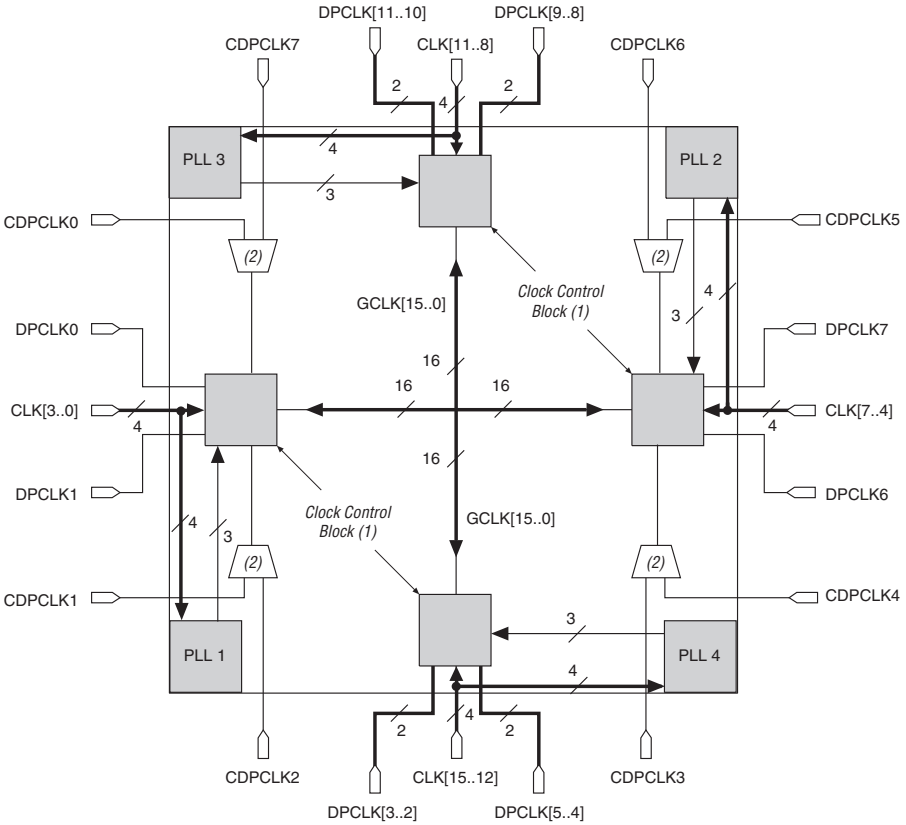
Cyclone II devices include a powerful FPGA feature set optimized for low-cost applications including a wide range of density, memory, embedded multiplier, and packaging options. Cyclone II devices support a wide range of common external memory interfaces and I/O protocols required in low-cost applications. Parameterizable IP cores from Altera and partners make using Cyclone II interfaces and protocols fast and easy.

Features

The Cyclone II device family offers the following features:

- High-density architecture with 4,608 to 68,416 LEs
  - M4K embedded memory blocks
  - Up to 1.1 Mbits of RAM available without reducing available logic
  - 4,096 memory bits per block (4,608 bits per block including 512 parity bits)
  - Variable port configurations of ×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
  - True dual-port (one read and one write, two reads, or two writes) operation for ×1, ×2, ×4, ×8, ×9, ×16, and ×18 modes
  - Byte enables for data input masking during writes
  - Up to 260-MHz operation
- Embedded multipliers
  - Up to 150 18- × 18-bit multipliers are each configurable as two independent 9- × 9-bit multipliers with up to 250-MHz performance
  - Optional input and output registers
- Advanced I/O support
  - High-speed differential I/O standard support, including LVDS, RSDS, mini-LVDS, LVPECL, differential HSTL, and differential SSTL
  - Single-ended I/O standard support, including 2.5-V and 1.8-V, SSTL class I and II, 1.8-V and 1.5-V HSTL class I and II, 3.3-V PCI and PCI-X 1.0, 3.3-, 2.5-, 1.8-, and 1.5-V LVCMOS, and 3.3-, 2.5-, and 1.8-V LVTTL
  - Peripheral Component Interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 3.0* compliance for 3.3-V operation at 33 or 66 MHz for 32- or 64-bit interfaces
  - PCI Express with an external TI PHY and an Altera PCI Express ×1 Megacore® function

Figure 2–12. EP2C15 & Larger PLL, CLK[], DPCLK[] & Clock Control Block Locations



Notes to Figure 2–12:

(1) There are four clock control blocks on each side.

(2) Only one of the corner CDPCLK pins in each corner can feed the clock control block at a time. The other CDPCLK pins can be used as general-purpose I/O pins.

Cyclone II devices support driver impedance matching to the impedance of the transmission line, typically 25 or 50 Ω When used with the output drivers, on-chip termination sets the output driver impedance to 25 or 50 Ω Cyclone II devices also support I/O driver series termination (R_S = 50 Ω) for SSTL-2 and SSTL-18. Table 2–19 lists the I/O standards that support impedance matching and series termination.

Table 2–19. I/O Standards Supporting Series Termination *Note (1)*

I/O Standards	Target R_S (Ω)	V_{CCIO} (V)
3.3-V LVTTL and LVCMOS	25 *(2)*	3.3
2.5-V LVTTL and LVCMOS	50 *(2)*	2.5
1.8-V LVTTL and LVCMOS	50 *(2)*	1.8
SSTL-2 class I	50 *(2)*	2.5
SSTL-18 class I	50 *(2)*	1.8

Notes to Table 2–19:

(1) Supported conditions are $V_{CCIO} = V_{CCIO} \pm 50$ mV.

(2) These R_S values are nominal values. Actual impedance varies across process, voltage, and temperature conditions.

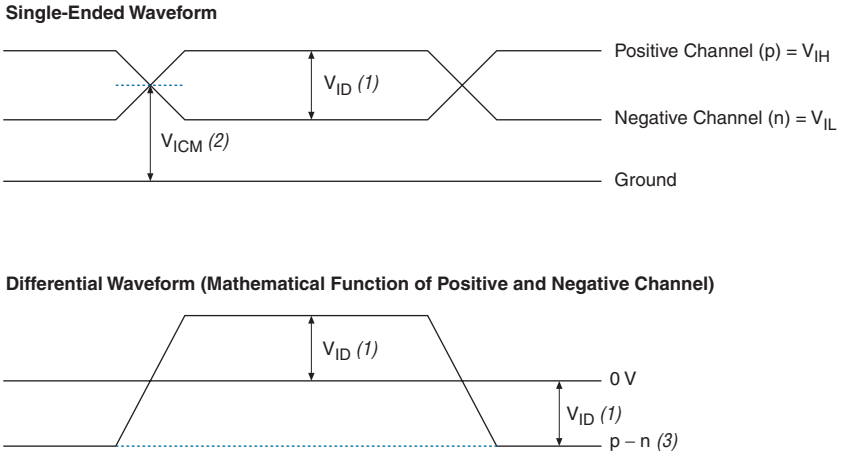
The recommended frequency range of operation is pending silicon characterization.

On-chip series termination can be supported on any I/O bank. V_{CCIO} and V_{REF} must be compatible for all I/O pins in order to enable on-chip series termination in a given I/O bank. I/O standards that support different R_S values can reside in the same I/O bank as long as their V_{CCIO} and V_{REF} are not conflicting.

When using on-chip series termination, programmable drive strength is not available.

Impedance matching is implemented using the capabilities of the output driver and is subject to a certain degree of variation, depending on the process, voltage and temperature. The actual tolerance is pending silicon characterization.

Figure 5–1. Receiver Input Waveforms for Differential I/O Standards



Notes to Figure 5–1:

(1) V_{ID} is the differential input voltage. $V_{ID} = |p - n|$.

(2) V_{ICM} is the input common mode voltage. $V_{ICM} = (p + n)/2$.

(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.337	–0.357	0.079	0.04	0.075	0.045	ns

Notes to Table 5–25:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–26. EP2C15A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.542	1.615	2.490	2.651	2.886	2.866	ns
t_{COUT}	1.544	1.617	2.506	2.664	2.894	2.874	ns
t_{PLLCIN}	–0.424	–0.448	–0.057	–0.107	–0.077	–0.107	ns
$t_{PLLCOUT}$	–0.422	–0.446	–0.041	–0.094	–0.069	–0.099	ns

Notes to Table 5–26:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C20/A Clock Timing Parameters

Tables 5–27 and 5–28 show the clock timing parameters for EP2C20/A devices.

Table 5–27. EP2C20/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL_18_CLASS_II	0	pF
1.5V_HSTL_CLASS_I	0	pF
1.5V_HSTL_CLASS_II	0	pF
1.8V_HSTL_CLASS_I	0	pF
1.8V_HSTL_CLASS_II	0	pF
DIFFERENTIAL_SSTL_2_CLASS_I	0	pF
DIFFERENTIAL_SSTL_2_CLASS_II	0	pF
DIFFERENTIAL_SSTL_18_CLASS_I	0	pF
DIFFERENTIAL_SSTL_18_CLASS_II	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
LVDS	0	pF
1.2V_HSTL	0	pF
1.2V_DIFFERENTIAL_HSTL	0	pF

Table 5–47. High-Speed I/O Timing Definitions (Part 2 of 2)

Parameter	Symbol	Description
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. Sampling window is the sum of the setup time, hold time, and jitter. The window of t_{SU} + t_H is expected to be centered in the sampling window. SW = TUI – TCCS – (2 × RSKM)
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2
Input jitter (peak to peak)	—	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak to peak)	—	Peak-to-peak output jitter on high-speed PLLs.
Signal rise time	t_{RISE}	Low-to-high transmission time.
Signal fall time	t_{FALL}	High-to-low transmission time.
Lock time	t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Figure 5–3. High-Speed I/O Timing Diagram

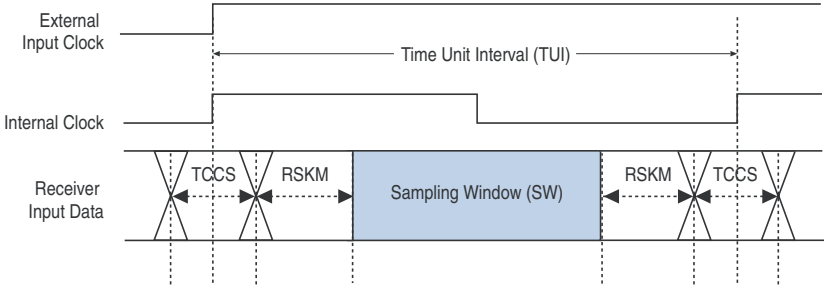
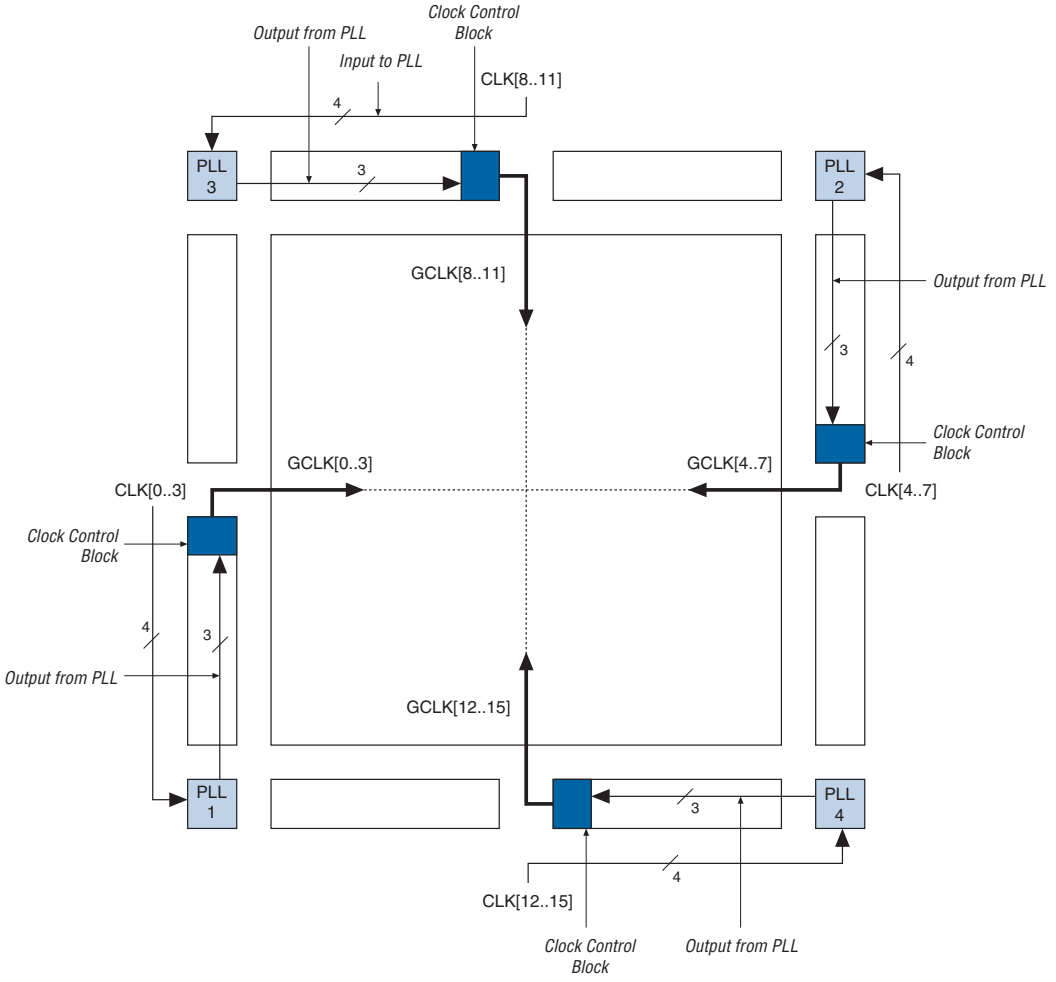


Figure 5–4 shows the high-speed I/O timing budget.

Figure 7–12. Cyclone II Clock Control Blocks Placement



The inputs to the four clock control blocks on each side are chosen from among the following clock sources:

- Four clock input pins
- Three PLL counter outputs
- Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins and two CDPCLK pins from both the top and bottom
- Four signals from internal logic

Document Revision History

Table 7–10 shows the revision history for this document.

Table 7–10. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	• Added document revision history. • Updated handpara note in "Introduction". • Updated *Note (3)* in Table 7–2. • Updated Figure 7–5. • Updated "Control Signals" section. • Updated "Thick VCCA Trace" section.	• Updated chapter with extended temperature information. • Updated `pllena` information in "Control Signals" section. • Corrected capacitor unit from10-F to 10 µF.
December 2005 v2.2	Updated industrial temperature range	
November 2005 v2.1	• Updated Figure 7–12. • Updated Figure 7–17.	
July 2005 v2.0	• Updated Table 7–6. • Updated "Hardware Features" section. • Updated "areset" section. • Updated Table 7–8. • Added "Board Layout" section.	
February 2005 v1.2	Updated information concerning signals. Added a note to Figures 7-9 through 7-13 regarding violating the setup or hold time on address registers.	
November, 2004 v1.1	Updated "Introduction" section.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Input/Output Clock Mode

Cyclone II memory blocks can implement the input/output clock mode for true and simple dual-port memory. On each of the two ports, A and B, one clock controls all registers for the data, write enable, and address inputs into the memory block. The other clock controls the blocks' data output registers. Each memory block port also supports independent clock enables for input and output registers. Asynchronous clear signals for the registers are not supported.

Figures 8–14 through 8–16 show the memory block in input/output clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

Section IV. I/O Standards

This section provides information on Cyclone® II single-ended, voltage referenced, and differential I/O standards.

This section includes the following chapters:

- Chapter 10, Selectable I/O Standards in Cyclone II Devices
- Chapter 11, High-Speed Differential Interfaces in Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 10–15. 1.5-V Differential HSTL Class I Termination

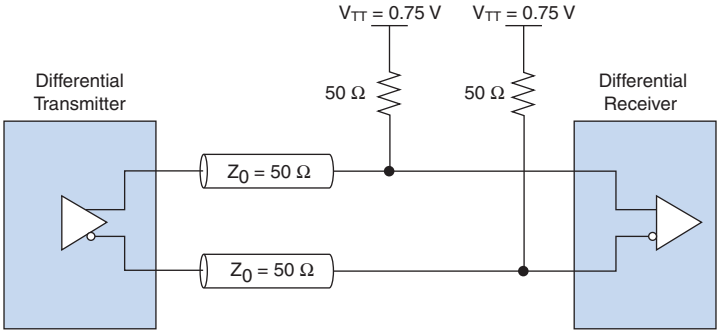
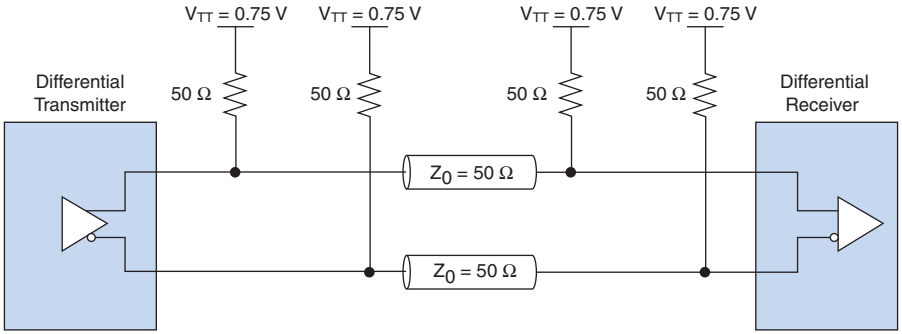


Figure 10–16. 1.5-V Differential HSTL Class II Termination



LVDS, RSDS and mini-LVDS

The LVDS standard is formulated under ANSI/TIA/EIA Standard, ANSI/TIA/EIA-644: Electrical Characteristics of Low Voltage Differential Signaling Interface Circuits.

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. This standard is used in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. Cyclone II devices are capable of running at a maximum data rate of 805 Mbps for input and 640 Mbps for output and still meet the ANSI/TIA/EIA-644 standard.

Because of the low voltage swing of the LVDS I/O standard, the electromagnetic interference (EMI) effects are much smaller than complementary metal-oxide semiconductor (CMOS),

Document Revision History

Table 12–4 shows the revision history for this document.

Table 12–4. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v1.2	• Added document revision history. • Updated "Software Support" section.	• Removed reference to third-party synthesis tool: LeonardoSpectrum and Synplify.
November 2005 v2.1	Updated Introduction.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Section VI. Configuration & Test

This section provides configuration information for all of the supported configuration schemes for Cyclone® II devices. These configuration schemes use either a microprocessor, configuration device, or download cable. There is detailed information on how to design with Altera® configuration devices. The last chapter provides information on JTAG support in Cyclone II devices.

This section includes the following chapters:

- Chapter 13, Configuring Cyclone II Devices
- Chapter 14, IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Configuration File Format

Table 13–3 shows the approximate uncompressed configuration file sizes for Cyclone II devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

Table 13–3. Cyclone II Raw Binary File (.rbf) Sizes *Note (1)*

Device	Data Size (Bits)	Data Size (Bytes)
EP2C5	1,265,792	152,998
EP2C8	1,983,536	247,974
EP2C15	3,892,496	486,562
EP2C20	3,892,496	486,562
EP2C35	6,858,656	857,332
EP2C50	9,963,392	1,245,424
EP2C70	14,319,216	1,789,902

Note to Table 13–3:
(1) These values are preliminary.

Use the data in Table 13–3 only to estimate the file size before design compilation. Different configuration file formats, such as a Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) format, have different file sizes. However, for any specific version of the Quartus® II software, any design targeted for the same device has the same uncompressed configuration file size. If compression is used, the file size can vary after each compilation since the compression ratio is dependent on the design.

Configuration Data Compression

Cyclone II devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Cyclone II devices. During configuration, the Cyclone II device decompresses the bitstream in real time and programs its SRAM cells.

Preliminary data indicates that compression reduces configuration bitstream size by 35 to 55%.

Cyclone II devices support decompression in the AS and PS configuration schemes. Decompression is not supported in JTAG-based configuration.

Cyclone II devices offer an optional INIT_DONE pin which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** window. If you use the INIT_DONE pin, an external 10-kΩ pull-up resistor is required to pull the signal high when nCONFIG is low and during the beginning of configuration. Once the optional bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. This low-to-high transition signals that the FPGA has entered user mode. If you do not use the INIT_DONE pin, the initialization period is complete after CONF_DONE goes high and 299 clock cycles are sent to the CLKUSR pin or after the time t_{CF2UM} (see Table 13–8) if the Cyclone II device uses the internal oscillator.

User Mode

When initialization is complete, the FPGA enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

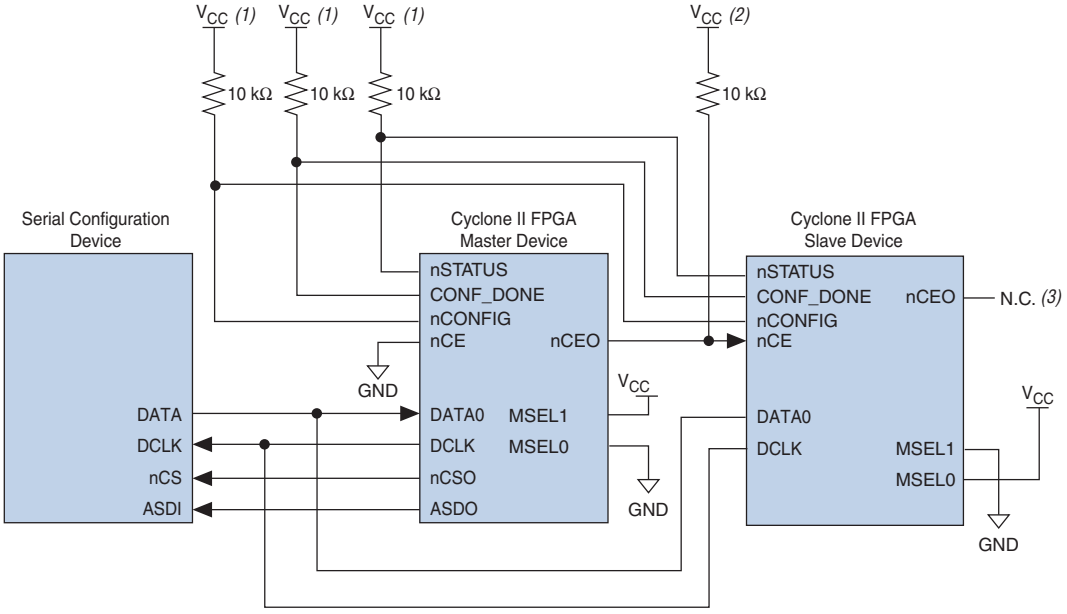
When the Cyclone II device is in user mode, you can initiate reconfiguration by pulling the nCONFIG signal low. The nCONFIG signal should be low for at least 2 µs. When nCONFIG is pulled low, the Cyclone II device is reset and enters the reset stage. The Cyclone II device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. Once nCONFIG returns to a logic high level and nSTATUS is released by the Cyclone II device, reconfiguration begins.

Error During Configuration

If an error occurs during configuration, the Cyclone II device drives the nSTATUS signal low to indicate a data frame error, and the CONF_DONE signal stays low. If you enable the **Auto-restart configuration after error** option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box, the Cyclone II device resets the serial configuration device by pulsing nCSO, releases nSTATUS after a reset time-out period (about 40 µs), and retries configuration. If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pull nCONFIG low for at least 2 µs to restart configuration.

If you use the optional CLKUSR pin and the nCONFIG pin is pulled low to restart configuration during device initialization, ensure CLKUSR continues to toggle during the time nSTATUS is low (a maximum of 40 µs).

Figure 13–4. Multiple Device AS Configuration



Notes to Figure 13–4:

(1) Connect the pull-up resistors to a 3.3-V supply.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

As shown in Figure 13–4, the nSTATUS and CONF_DONE pins on all target FPGAs are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the FPGAs. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep the CONF_DONE signal low until they receive their configuration data. When all the target FPGAs in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor pulls this signal high, and all devices simultaneously enter initialization mode.

A device operating in JTAG mode uses the TDI, TDO, TMS, and TCK pins. The TCK pin has a weak internal pull-down resistor while the other JTAG input pins, TDI and TMS, have weak internal pull-up resistors. All user I/O pins are tri-stated during JTAG configuration. Table 13–9 explains each JTAG pin's function.

Table 13–9. Dedicated JTAG Pins

Pin Name	Pin Type	Description
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to GND.

The TDO output is powered by the V_{CCIO} power supply. If V_{CCIO} is tied to 3.3-V, both the I/O pins and the JTAG TDO port drive at 3.3-V levels.

Thermal Resistance

Thermal resistance values for Cyclone II devices are provided for a board meeting JEDEC specifications and for a typical board. The values provided are as follows:

- θ_{JA} (°C/W) Still Air—Junction-to-ambient thermal resistance with no airflow when a heat sink is not being used.
- θ_{JA} (°C/W) 100 ft./minute—Junction-to-ambient thermal resistance with 100 ft./minute airflow when a heat sink is not being used.
- θ_{JA} (°C/W) 200 ft./minute—Junction-to-ambient thermal resistance with 200 ft./minute airflow when a heat sink is not being used.
- θ_{JA} (°C/W) 400 ft./minute—Junction-to-ambient thermal resistance with 400 ft./minute airflow when a heat sink is not being used.
- θ_{JC} (°C/W)—Junction-to-case thermal resistance for device.
- θ_{JB} (°C/W)—Junction-to-board thermal resistance for specific board being used.

Table 15–2 provides θ_{JA} (junction-to-ambient thermal resistance) values and θ_{JC} (junction-to-case thermal resistance) values for Cyclone II devices on a board meeting JEDEC specifications for thermal resistance calculation. The JEDEC board specifications require two signal and two power/ground planes and are available at **www.jedec.org**.

Table 15–2. Thermal Resistance of Cyclone II Devices for Board Meeting JEDEC Specifications (Part 1 of 2)

Device	Pin Count	Package	θ_{JA} (°C/W) Still Air	θ_{JA} (°C/W) 100 ft./min.	θ_{JA} (°C/W) 200 ft./min.	θ_{JA} (°C/W) 400 ft./min.	θ_{JC} (°C/W)
EP2C5	144	TQFP	31	29.3	27.9	25.5	10
	208	PQFP	30.4	29.2	27.3	22.3	5.5
	256	FineLine BGA	30.2	26.1	23.6	21.7	8.7
EP2C8	144	TQFP	29.8	28.3	26.9	24.9	9.9
	208	PQFP	30.2	28.8	26.9	21.7	5.4
	256	FineLine BGA	27	23	20.5	18.5	7.1
EP2C15	256	FineLine BGA	24.2	20	17.8	16	5.5
	484	FineLine BGA	21	17	14.8	13.1	4.2
EP2C20	240	PQFP	26.6	24	21.4	17.4	4.2
	256	FineLine BGA	24.2	20	17.8	16	5.5
	484	FineLine BGA	21	17	14.8	13.1	4.2
EP2C35	484	FineLine BGA	19.4	15.4	13.3	11.7	3.3
	484	Ultra FineLine BGA	20.6	16.6	14.5	12.8	5
	672	FineLine BGA	18.6	14.6	12.6	11.1	3.1

896-Pin FineLine BGA Package – Wirebond

- All dimensions and tolerances conform to ASME Y14.5M - 1994.
- Controlling dimension is in millimeters.
- Pin A1's location may be indicated by an ID dot in its proximity on the package surface.

Tables 15–19 and 15–20 show the package information and package outline figure references, respectively, for the 896-pin FineLine BGA.

Table 15–19. 896-Pin FineLine BGA Package Information

Description	Specification
Ordering code reference	F
Package acronym	FineLine BGA
Substrate material	BT
Solder ball composition	Regular: 63Sn: 37Pb (typical) Pb-free: Sn: 3.0Ag: 0.5Cu (typical)
JEDEC outline reference	MS-034 variation AAN-1
Maximum lead coplanarity	0.008 inches (0.20 mm)
Weight	11.5 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–20. 896-Pin FineLine BGA Package Outline Dimensions

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	–	–	2.60
A1	0.30	–	–
A2	–	–	2.20
A3	–	–	1.80
D	31.00 BSC		
E	31.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		