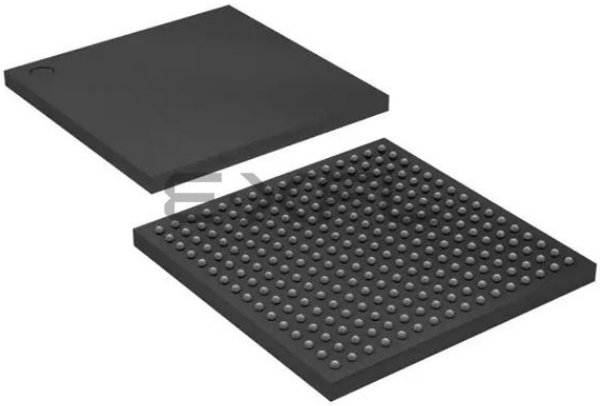

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	158
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5f256i8n

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, M4K memory blocks, embedded multipliers, and IOEs. C16 column interconnects drive to other row and column interconnects at every fourth LAB. C16 column interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. C16 interconnects can drive R24, R4, C16, and C4 interconnects.

Device Routing

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (for example, M4K memory, embedded multiplier, or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 2–1 shows the Cyclone II device's routing scheme.

Table 2–1. Cyclone II Device Routing Scheme (Part 1 of 2)

Source	Destination												
	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	LE	M4K RAM Block	Embedded Multiplier	PLL	Column IOE	Row IOE
Register Chain								✓					
Local Interconnect								✓	✓	✓	✓	✓	✓
Direct Link Interconnect		✓											
R4 Interconnect		✓		✓	✓	✓	✓						
R24 Interconnect				✓	✓	✓	✓						
C4 Interconnect		✓		✓	✓	✓	✓						
C16 Interconnect				✓	✓	✓	✓						

Global Clock Network

The 16 or 8 global clock networks drive throughout the entire device. Dedicated clock pins (CLK[]), PLL outputs, the logic array, and dual-purpose clock (DPCLK[]) pins can also drive the global clock network.

The global clock network can provide clocks for all resources within the device, such as IOEs, LEs, memory blocks, and embedded multipliers. The global clock lines can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin, or DQS signals for DDR SDRAM or QDRII SRAM interfaces. Internal logic can also drive the global clock network for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fan-out.

Clock Control Block

There is a clock control block for each global clock network available in Cyclone II devices. The clock control blocks are arranged on the device periphery and there are a maximum of 16 clock control blocks available per Cyclone II device. The larger Cyclone II devices (EP2C15 devices and larger) have 16 clock control blocks, four on each side of the device. The smaller Cyclone II devices (EP2C5 and EP2C8 devices) have eight clock control blocks, four on the left and right sides of the device.

The control block has these functions:

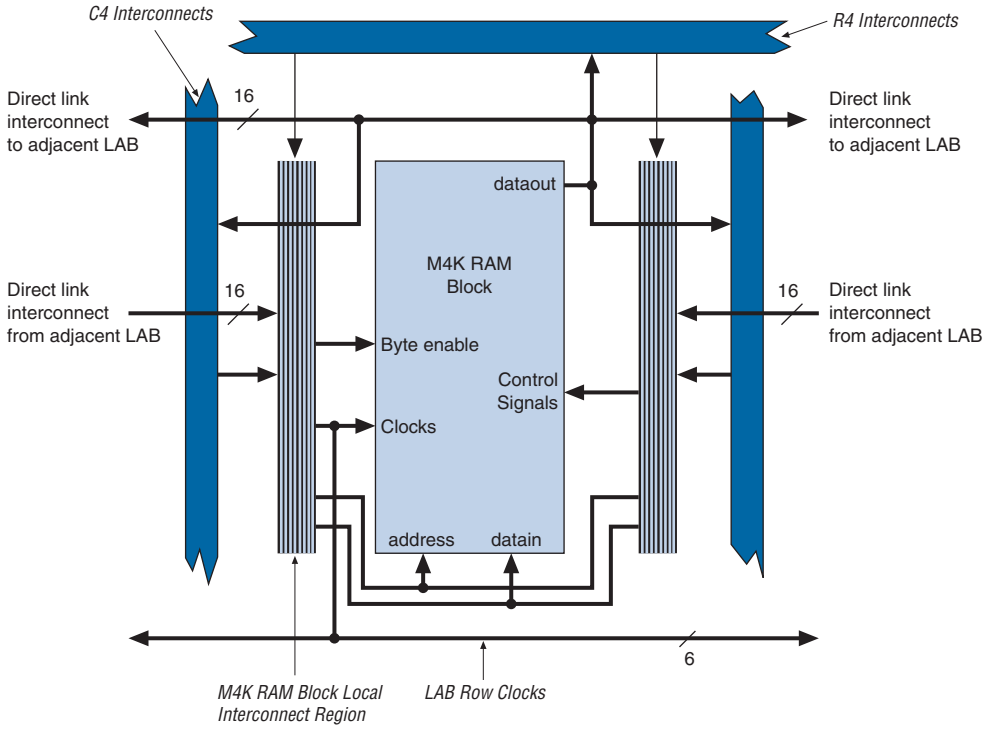
- Dynamic global clock network clock source selection
- Dynamic enable/disable of the global clock network

In Cyclone II devices, the dedicated CLK[] pins, PLL counter outputs, DPCLK[] pins, and internal logic can all feed the clock control block. The output from the clock control block in turn feeds the corresponding global clock network.

The following sources can be inputs to a given clock control block:

- Four clock pins on the same side as the clock control block
- Three PLL clock outputs from a PLL
- Four DPCLK pins (including CDPCLK pins) on the same side as the clock control block
- Four internally-generated signals

Figure 2–17. M4K RAM Block LAB Row Interface



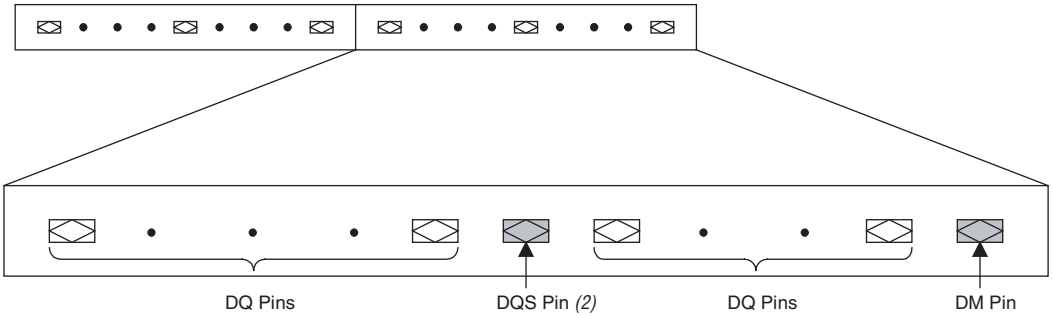
For more information on Cyclone II embedded memory, see the *Cyclone II Memory Blocks* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Embedded Multipliers

Cyclone II devices have embedded multiplier blocks optimized for multiplier-intensive digital signal processing (DSP) functions, such as finite impulse response (FIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions. You can use the embedded multiplier in one of two basic operational modes, depending on the application needs:

- One 18-bit multiplier
- Up to two independent 9-bit multipliers

Figure 2–26. Cyclone II Device DQ & DQS Groups in ×8/×9 Mode *Notes (1), (2)*



Notes to Figure 2–26:
(1) Each DQ group consists of a DQS pin, DM pin, and up to nine DQ pins.
(2) This is an idealized pin layout. For actual pin layout, refer to the pin table.

Cyclone II devices support the data strobe or read clock signal (DQS) used in DDR and DDR2 SDRAM. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. The dedicated external memory interface in Cyclone II devices also includes programmable delay circuitry that can shift the incoming DQS signals to center align the DQS signals within the data window.

The DQS signal is usually associated with a group of data (DQ) pins. The phase-shifted DQS signals drive the global clock network, which is used to clock the DQ signals on internal LE registers.

Table 2–15 shows the number of DQ pin groups per device.

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups (5), (6)	Number of ×16 Groups	Number of ×18 Groups (5), (6)
EP2C5	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
EP2C8	144-pin TQFP (2)	3	3	0	0
	208-pin PQFP	7 (3)	4	3	3
	256-pin FineLine BGA®	8 (3)	4	4	4
EP2C15	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8
EP2C20	256-pin FineLine BGA	8	4	4	4
	484-pin FineLine BGA	16 (4)	8	8	8

Table 2–20. Cyclone II MultiVolt I/O Support (Part 2 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
3.3			✓ *(4)*	✓	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓

Notes to Table 2–20:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on **Allow voltage overdrive for LVTTL/LVCMOS input pins** option in Device setting option in the Quartus II software.

(3) When V_{CCIO} = 1.8-V, a Cyclone II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(4) When V_{CCIO} = 3.3-V and a 2.5-V input signal feeds an input pin or when V_{CCIO} = 1.8-V and a 1.5-V input signal feeds an input pin, the V_{CCIO} supply current will be slightly larger than expected. The reason for this increase is that the input signal level does not drive to the V_{CCIO} rail, which causes the input buffer to not completely shut off.

(5) When V_{CCIO} = 2.5-V, a Cyclone II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(6) When V_{CCIO} = 3.3-V, a Cyclone II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Table 5–51. LVDS Receiver Timing Specification

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×8	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×7	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×4	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×2	10	—	402.5	10	—	320	10	—	320 *(1)*	MHz
	×1	10	—	402.5	10	—	402.5	10	—	402.5 *(3)*	MHz
HSIODR	×10	100	—	805	100	—	640	100	—	640 *(2)*	Mbps
	×8	80	—	805	80	—	640	80	—	640 *(2)*	Mbps
	×7	70	—	805	70	—	640	70	—	640 *(2)*	Mbps
	×4	40	—	805	40	—	640	40	—	640 *(2)*	Mbps
	×2	20	—	805	20	—	640	20	—	640 *(2)*	Mbps
	×1	10	—	402.5	10	—	402.5	10	—	402.5 *(4)*	Mbps
SW	—	—	—	300	—	—	400	—	—	400	ps
Input jitter tolerance	—	—	—	500	—	—	500	—	—	550	ps
t_{LOCK}	—	—	—	100	—	—	100	—	—	100 *(5)*	ps

Notes to Table 5–51:
(1) For extended temperature devices, the maximum input clock frequency for x10 through x2 modes is 275 MHz.
(2) For extended temperature devices, the maximum data rate for x10 through x2 modes is 550 Mbps.
(3) For extended temperature devices, the maximum input clock frequency for x1 mode is 340 MHz.
(4) For extended temperature devices, the maximum data rate for x1 mode is 340 Mbps.
(5) For extended temperature devices, the maximum lock time is 500 us.

External Memory Interface Specifications

Table 5–52 shows the DQS bus clock skew adder specifications.

Table 5–52. DQS Bus Clock Skew Adder Specifications

Mode	DQS Clock Skew Adder	Unit
×9	155	ps
×18	190	ps

Note to Table 5–52:
(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a ×9 DQ group is 155 ps or ±77.5 ps.

locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals

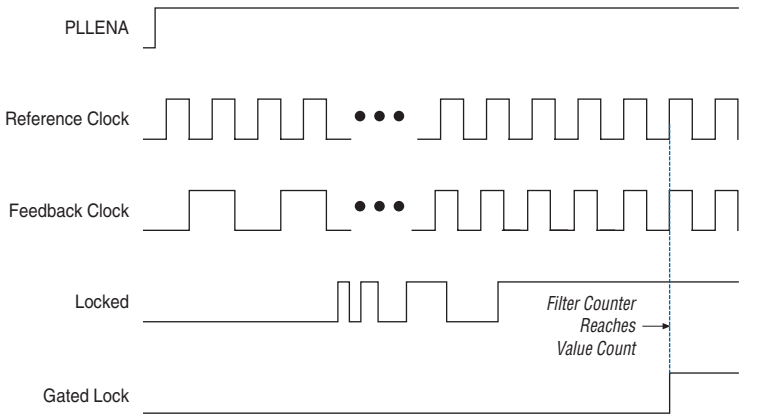


Table 7–8. Global Clock Network Connections (Part 2 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PLL4_c0													✓	✓		✓
PLL4_c1													✓		✓	✓
PLL4_c2														✓	✓	
DPCLK0 *(1)*	✓															
DPCLK1 *(1)*		✓														
DPCLK10 *(1)*, *(2)* CDPCLK0 or CDPCLK7 *(3)*			✓													
DPCLK2 *(1)*, *(2)* CDPCLK1 or CDPCLK2 *(3)*				✓												
DPCLK7 *(1)*					✓											
DPCLK6 *(1)*						✓										
DPCLK8 *(1)*, *(2)* CDPCLK5 or CDPCLK6 *(3)*							✓									
DPCLK4 *(1)*, *(2)* CDPCLK4 or CDPCLK3 *(3)*								✓								
DPCLK8 *(1)*									✓							
DPCLK11 *(1)*										✓						
DPCLK9 *(1)*											✓					
DPCLK10 *(1)*												✓				
DPCLK5 *(1)*													✓			
DPCLK2 *(1)*														✓		
DPCLK4 *(1)*															✓	

Figure 8–4. Cyclone II Address Clock Enable During Read Cycle Waveform

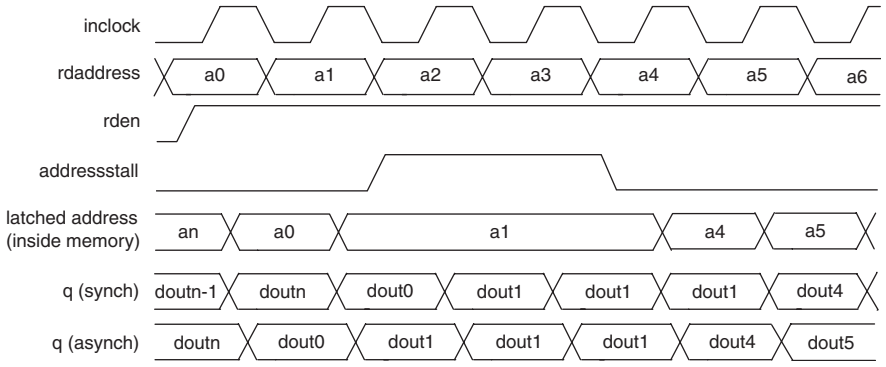
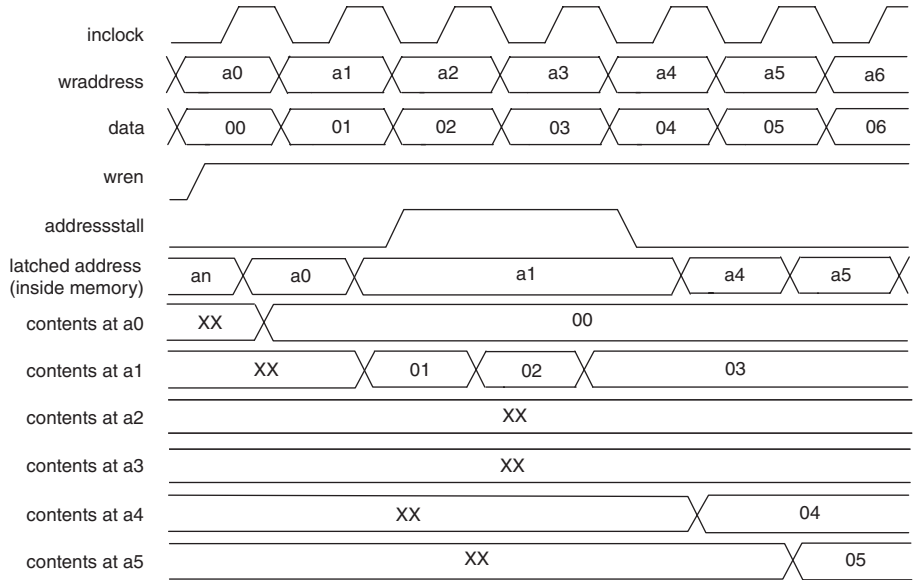


Figure 8–5. Cyclone II Address Clock Enable During Write Cycle Waveform



Memory Modes

Cyclone II M4K memory blocks include input registers that synchronize writes and output registers to pipeline data, thereby improving system performance. All M4K memory blocks are fully synchronous, meaning that you must send all inputs through a register, but you can either send outputs through a register (pipelined) or bypass the register (flow-through).

M4K memory blocks do not support asynchronous memory (unregistered inputs).

The M4K memory blocks support the following modes:

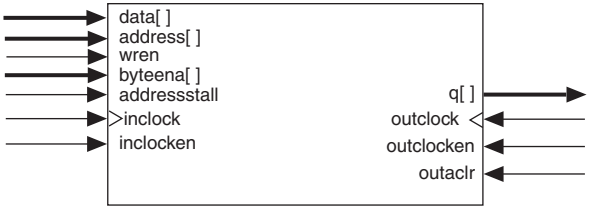
- Single-port
- Simple dual-port
- True dual-port (bidirectional dual-port)
- Shift register
- ROM
- FIFO buffers

Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Single-Port Mode

Single-port mode supports non-simultaneous read and write operations. Figure 8–6 shows the single-port memory configuration for Cyclone II memory blocks.

Figure 8–6. Single-Port Mode *Note (1)*



Note to Figure 8–6:
(1) Two single-port memory blocks can be implemented in a single M4K block in packed mode.

In single-port mode, the outputs are in read-during-write mode, which means that during the write operation, data written to the RAM flows through to the RAM outputs. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle on which it was written.

See "Read-During- Write Operation at the Same Address" on page 8–28 for more information about read-during-write mode.

The port width configurations for M4K blocks in single-port mode are as follows:

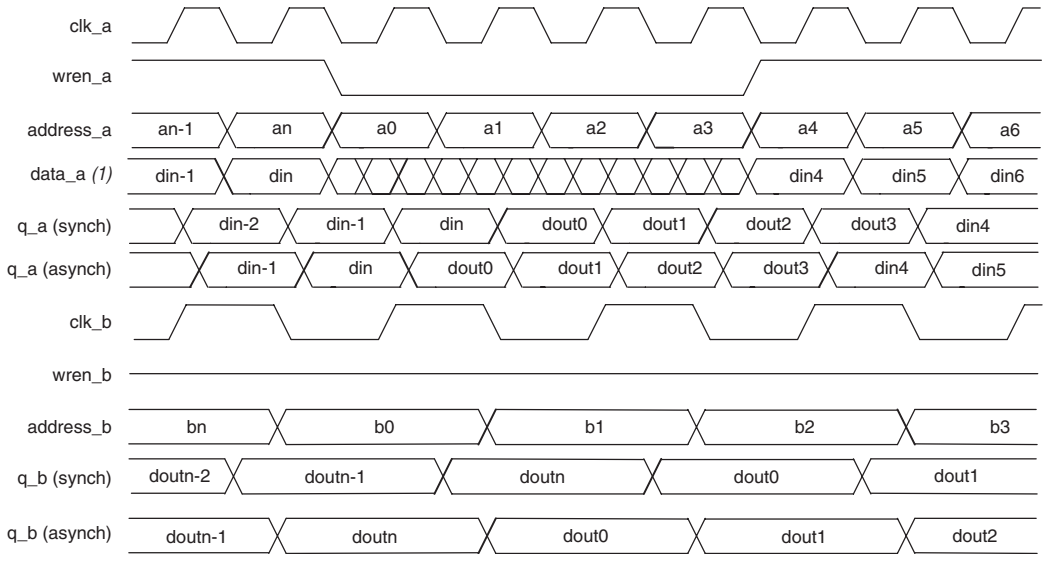
outputs, respectively. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle on which it was written. See "Read-During- Write Operation at the Same Address" on page 8–28 for waveforms and information on mixed-port read-during-write mode.

Potential write contentions must be resolved external to the RAM because writing to the same address location at both ports results in unknown data storage at that location.

For the maximum synchronous write cycle time, refer to the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Figure 8–11 shows true dual-port timing waveforms for the write operation at port A and the read operation at port B.

Figure 8–11. Cyclone II True Dual-Port Timing Waveforms

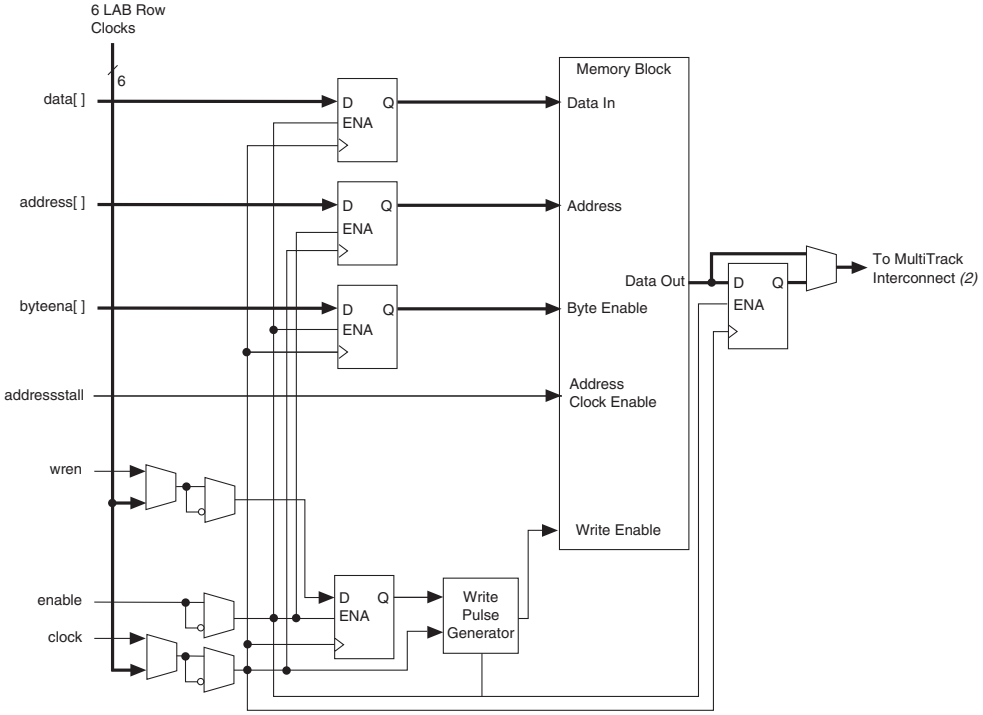


Note to Figure 8–11:
(1) The crosses in the `data_a` waveform during write indicate "don't care."

Shift Register Mode

Cyclone II memory blocks can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto-correlation and cross-correlation functions. These and other DSP

Figure 8–20. Cyclone II Single-Clock Mode in Single-Port Mode *Notes (1), (2)*



Notes to Figure 8–20:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

(2) See the *Cyclone II Device Family Data Sheet* in Volume 1 of the *Cyclone II Device Handbook* for more information on the MultiTrack interconnect.

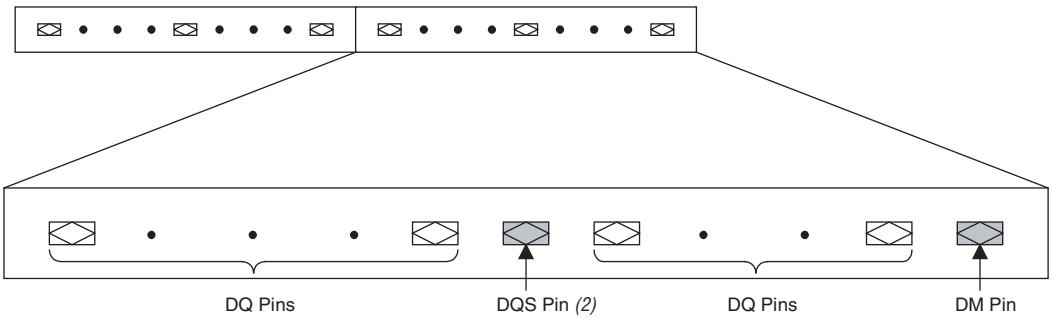
Power-Up Conditions & Memory Initialization

The Cyclone II memory block outputs always power-up to zero, regardless of whether the output registers are used or bypassed. Even if an MIF pre-loads the contents of the memory block, the outputs still power up cleared. For example, if address 0 is pre-initialized to `FF`, M4K blocks power up with the output at `00`. A subsequent read after power up from address 0 outputs the pre-initialized value of `FF`.

DDR Memory Interface Pins

Cyclone II devices use data (DQ), data strobe (DQS), and clock pins to interface with external memory. Figure 9–6 shows the DQ and DQS pins in the ×8/×9 mode.

Figure 9–6. Cyclone II Device DQ & DQS Groups in ×8/×9 Mode *Notes (1), (3)*



Notes to Figure 9–6:

(1) Each DQ group consists of a DQS pin, a DM pin, and up to nine DQ pins.

(2) For the QDRII memory interface, other DQS pins implement the CQn pins. These pins are denoted by DQS/CQ# in the pin table.

(3) This is an idealized pin layout. For the actual pin layout, refer to the pin tables in the *PCB Layout Guidelines* section of the *Cyclone II Device Handbook, Volume 1*.

Data & Data Strobe Pins

Cyclone II data pins for the DDR memory interfaces are called DQ pins. Cyclone II devices can use either bidirectional data strobes or unidirectional read clocks. Depending on the external memory interface, either the memory device's read data strobes or read clocks feed the DQS pins.

In Cyclone II devices, all the I/O banks support DDR and DDR2 SDRAM and QDRII SRAM memory at up to 167 MHz. All the I/O banks support DQS signals with the DQ bus modes of ×8/×9 and ×16/×18. Cyclone II devices can support either bidirectional data strobes or unidirectional read clocks.

DDR2 and QDRII interfaces with class II I/O standard can only be implemented on the top and bottom I/O banks of the Cyclone II device.

November 2005 v2.1	• Updated Tables 10–2 and 10–3. • Added PCI Express information. • Updated Table 10–6.	—
July 2005 v2.0	Updated Table 10–1.	—
November 2004 v1.1	Updated Table 10–7.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Although they both use the same compression algorithm, the decompression feature supported by Cyclone II devices is different from the decompression feature in enhanced configuration devices (EPC16, EPC8, and EPC4 devices). The data decompression feature in the enhanced configuration devices allows them to store compressed data and decompress the bitstream before transmitting it to the target devices.

In PS mode, you should use the Cyclone II decompression feature since sending compressed configuration data reduces configuration time. You should not use both the Cyclone II device and the enhanced configuration device decompression features simultaneously. The compression algorithm is not intended to be recursive and could expand the configuration file instead of compressing it further.

You should use the Cyclone II decompression feature during AS configuration if you need to save configuration memory space in the serial configuration device.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash, and decreases the time needed to transmit the bitstream to the Cyclone II device. The time required by a Cyclone II device to decompress a configuration file is less than the time needed to transmit the configuration data to the FPGA.

There are two methods to enable compression for Cyclone II bitstreams: before design compilation (in the Compiler Settings menu) and after design compilation (in the **Convert Programming Files** window).

To enable compression in the project's compiler settings, select **Device** under the Assignments menu to bring up the settings window. After selecting your Cyclone II device open the **Device & Pin Options** window, and in the **General settings** tab enable the check box for **Generate compressed bitstreams** (see Figure 13–1).

Configuration Stage

When the nSTATUS pin transitions high, the configuration device's OE pin also transitions high and the configuration device clocks data out serially to the FPGA using its internal oscillator. The Cyclone II device receives configuration data on its DATA0 pin and the clock is received on the DCLK pin. Data is latched into the FPGA on the rising edge of DCLK.

After the FPGA has received all configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by a pull-up resistor. Since the Cyclone II device's CONF_DONE pin is tied to the configuration device's nCS pin, the configuration device is disabled when CONF_DONE goes high. Enhanced configuration and EPC2 devices have an optional internal pull-up resistor on the nCS pin. You can turn this option on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you do not use this internal pull-up resistor, you need to connect an external 10-kΩ pull-up resistor to the nCS and CONF_DONE line. A low-to-high transition on CONF_DONE indicates configuration is complete, and the device can begin initialization.

Initialization Stage

In Cyclone II devices, the default initialization clock source is the Cyclone II internal oscillator (typically 10 MHz). Cyclone II devices can also use the optional CLKUSR pin. If your design uses the internal oscillator, the Cyclone II device supplies itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to use another device or source to send additional clock cycles to the CLKUSR pin during the initialization stage. Additionally, you can use of the CLKUSR pin as a user I/O pin, which means you have an additional user I/O pin.

If you want to delay the initialization of the device, you can use the CLKUSR pin. Using the CLKUSR pin allows you to control when the Cyclone II device enters user mode. You can delay the Cyclone II devices from entering user mode for an indefinite amount of time. You can turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data is accepted and CONF_DONE goes high, Cyclone II devices require 299 clock cycles to properly initialize and support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you use the INIT_DONE pin, an external 10-kΩ pull-up resistor pulls it high when

This chapter discusses how to use the IEEE Std. 1149.1 BST circuitry in Cyclone™ II devices, including:

- IEEE Std. 1149.1 BST architecture
- IEEE Std. 1149.1 boundary-scan register
- IEEE Std. 1149.1 BST operation control
- I/O voltage support in JTAG chain
- Using IEEE Std. 1149.1 BST circuitry
- Disabling IEEE Std. 1149.1 BST circuitry
- Guidelines for IEEE Std. 1149.1 boundary-scan testing
- Boundary-Scan Description Language (BSDL) support

In addition to BST, you can use the IEEE Std. 1149.1 controller for Cyclone II device in-circuit reconfiguration (ICR). However, this chapter only discusses the BST feature of the IEEE Std. 1149.1 circuitry.

For information on configuring Cyclone II devices via the IEEE Std. 1149.1 circuitry, see the *Configuring Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

IEEE Std. 1149.1 BST Architecture

A Cyclone II device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS and TCK. The optional TRST pin is not available in Cyclone II devices. TDI and TMS pins have weak internal pull-up resistors while TCK has weak internal pull-down resistors. All user I/O pins are tri-stated during JTAG configuration. Table 14–1 summarizes the functions of each of these pins.

Table 14–1. IEEE Std. 1149.1 Pin Descriptions

Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Signal applied to TDI is expected to change state at the falling edge of TCK. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. During non-JTAG operation, TMS is recommended to be driven high.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. The clock input waveform should have a 50% duty cycle.

Section VII. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. The chapters in this section contain the required PCB layout guidelines and package specifications.

This section includes the following chapters:

- Chapter 15, Package Information for Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Figure 15–8 shows a 896-pin FineLine BGA package outline.

Figure 15–8. 896-Pin FineLine BGA Package Outline