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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	142
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5q208c7

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC Characteristics and Timing Specifications

Table 2–15. Cyclone II DQS & DQ Bus Mode Support (Part 2 of 2) *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×9 Groups *(5)*, *(6)*	Number of ×16 Groups	Number of ×18 Groups *(5)*, *(6)*
EP2C35	484-pin FineLine BGA	16 *(4)*	8	8	8
	672-pin FineLine BGA	20 *(4)*	8	8	8
EP2C50	484-pin FineLine BGA	16 *(4)*	8	8	8
	672-pin FineLine BGA	20 *(4)*	8	8	8
EP2C70	672-pin FineLine BGA	20 *(4)*	8	8	8
	896-pin FineLine BGA	20 *(4)*	8	8	8

Notes to Table 2–15:

(1) Numbers are preliminary.
(2) EP2C5 and EP2C8 devices in the 144-pin TQFP package do not have any DQ pin groups in I/O bank 1.
(3) Because of available clock resources, only a total of 6 DQ/DQS groups can be implemented.
(4) Because of available clock resources, only a total of 14 DQ/DQS groups can be implemented.
(5) The ×9 DQS/DQ groups are also used as ×8 DQS/DQ groups. The ×18 DQS/DQ groups are also used as ×16 DQS/DQ groups.
(6) For QDRI implementation, if you connect the D ports (write data) to the Cyclone II DQ pins, the total available ×9 DQS /DQ and ×18 DQS/DQ groups are half of that shown in Table 2–15.

You can use any of the DQ pins for the parity pins in Cyclone II devices. The Cyclone II device family supports parity in the ×8/×9, and ×16/×18 mode. There is one parity bit available per eight bits of data pins.

The data mask, DM, pins are required when writing to DDR SDRAM and DDR2 SDRAM devices. A low signal on the DM pin indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. In Cyclone II devices, the DM pins are assigned and are the preferred pins. Each group of DQS and DQ signals requires a DM pin.

When using the Cyclone II I/O banks to interface with the DDR memory, at least one PLL with two clock outputs is needed to generate the system and write clock. The system clock is used to clock the DQS write signals, commands, and addresses. The write clock is shifted by –90° from the system clock and is used to clock the DQ signals during writes.

Figure 2–27 illustrates DDR SDRAM interfacing from the I/O through the dedicated circuitry to the logic array.

Programmable Drive Strength

The output buffer for each Cyclone II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL-2 class I and II, SSTL-18 class I and II, HSTL-18 class I and II, and HSTL-1.5 class I and II standards have several levels of drive strength that you can control. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 2–16 shows the possible settings for the I/O standards with drive strength control.

Table 2–16. Programmable Drive Strength (Part 1 of 2) *Note (1)*

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top & Bottom I/O Pins	Side I/O Pins
LVTTL (3.3 V)	4	4
	8	8
	12	12
	16	16
	20	20
	24	24
LVCMOS (3.3 V)	4	4
	8	8
	12	12
	16	
	20	
	24	
LVTTL/LVCMOS (2.5 V)	4	4
	8	8
	12	
	16	
LVTTL/LVCMOS (1.8 V)	2	2
	4	4
	6	6
	8	8
	10	10
	12	12

The Cyclone II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Cyclone II devices.

Table 3–2. Cyclone II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2C5	498
EP2C8	597
EP2C15	969
EP2C20	969
EP2C35	1,449
EP2C50	1,374
EP2C70	1,890

Table 3–3. 32-Bit Cyclone II Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP2C5	0000	0010 0000 1011 0001	000 0110 1110	1
EP2C8	0000	0010 0000 1011 0010	000 0110 1110	1
EP2C15	0000	0010 0000 1011 0011	000 0110 1110	1
EP2C20	0000	0010 0000 1011 0011	000 0110 1110	1
EP2C35	0000	0010 0000 1011 0100	000 0110 1110	1
EP2C50	0000	0010 0000 1011 0101	000 0110 1110	1
EP2C70	0000	0010 0000 1011 0110	000 0110 1110	1

Notes to Table 3–3:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

For more information on the Cyclone II JTAG specifications, refer to the *DC Characteristics & Timing Specifications* chapter in the *Cyclone II Device Handbook, Volume 1*.

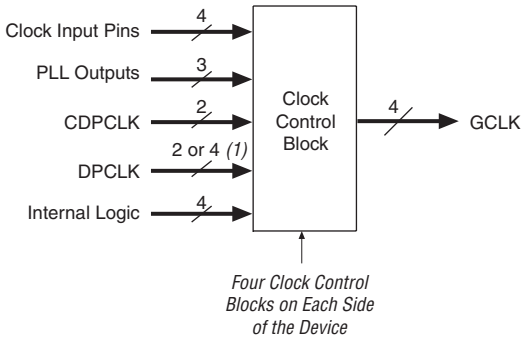
Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 1 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
LVTTL	4 mA	t_{OP}	1524	1599	2903	3125	3341	3348	ps
		t_{DIP}	1656	1738	3073	3319	3567	3567	ps
	8 mA	t_{OP}	1343	1409	2670	2866	3054	3061	ps
		t_{DIP}	1475	1548	2840	3060	3280	3280	ps
	12 mA	t_{OP}	1287	1350	2547	2735	2917	2924	ps
		t_{DIP}	1419	1489	2717	2929	3143	3143	ps
	16 mA	t_{OP}	1239	1299	2478	2665	2844	2851	ps
		t_{DIP}	1371	1438	2648	2859	3070	3070	ps
	20 mA	t_{OP}	1228	1288	2456	2641	2820	2827	ps
		t_{DIP}	1360	1427	2626	2835	3046	3046	ps
	24 mA (1)	t_{OP}	1220	1279	2452	2637	2815	2822	ps
		t_{DIP}	1352	1418	2622	2831	3041	3041	ps
LVCMOS	4 mA	t_{OP}	1346	1412	2509	2695	2873	2880	ps
		t_{DIP}	1478	1551	2679	2889	3099	3099	ps
	8 mA	t_{OP}	1240	1300	2473	2660	2840	2847	ps
		t_{DIP}	1372	1439	2643	2854	3066	3066	ps
	12 mA	t_{OP}	1221	1280	2428	2613	2790	2797	ps
		t_{DIP}	1353	1419	2598	2807	3016	3016	ps
	16 mA	t_{OP}	1203	1262	2403	2587	2765	2772	ps
		t_{DIP}	1335	1401	2573	2781	2991	2991	ps
	20 mA	t_{OP}	1194	1252	2378	2562	2738	2745	ps
		t_{DIP}	1326	1391	2548	2756	2964	2964	ps
	24 mA (1)	t_{OP}	1192	1250	2382	2566	2742	2749	ps
		t_{DIP}	1324	1389	2552	2760	2968	2968	ps

From the clock sources listed above, only two clock input pins, two PLL clock outputs, one DPCLK or CDPCLK pin, and one source from internal logic can drive into any given clock control blocks, as shown in Figure 7–11. Out of these six inputs to any clock control block, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of the DPCLK or CDPCLK pin and the signal from internal logic.

Figure 7–13 shows the simplified version of the four clock control blocks on each side of the Cyclone II device periphery. The Cyclone II devices support up to 16 of these clock control blocks and this allows for up to a maximum of 16 global clocks in Cyclone II devices.

Figure 7–13. Clock Control Blocks on Each Side of the Cyclone II Device



Note to Figure 7–13:
(1) The left and right sides of the device have two DPCLK pins, and the top and bottom of the device have four DPCLK pins.

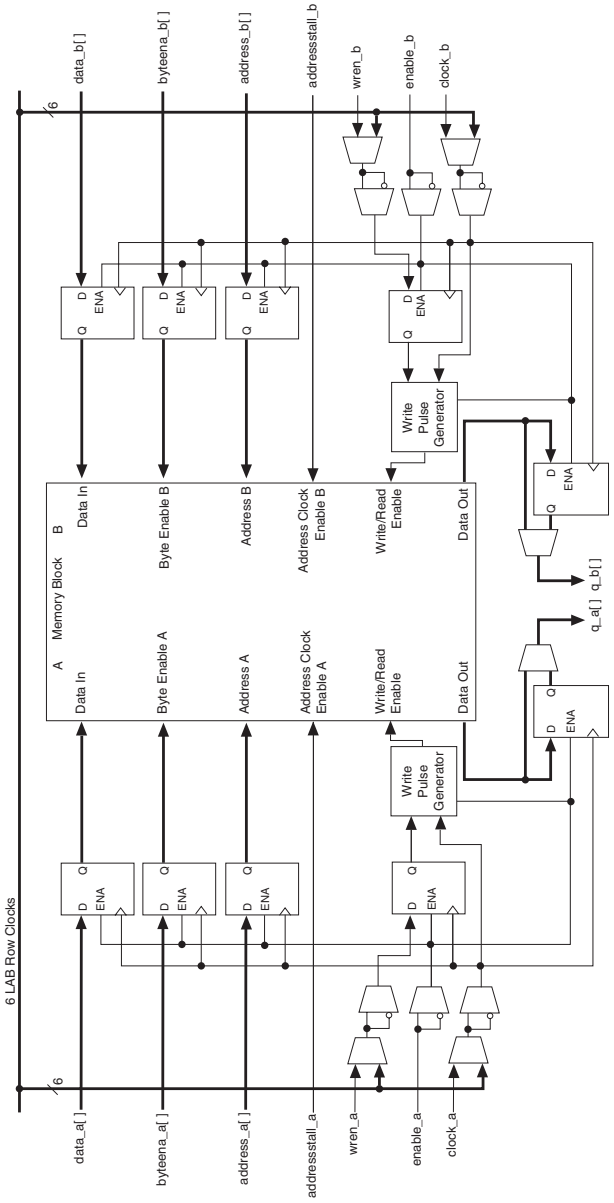
Global Clock Network Power Down

The Cyclone II global clock network can be disabled (powered down) by both static and dynamic approaches. When a clock network is powered down, all the logic fed by the clock network is in an off-state, thereby reducing the overall power consumption of the device.

The global clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable or disable feature allows internal logic to synchronously control power up or down on the global clock networks in the Cyclone II device. This function is independent of the PLL and is applied directly on the clock network, as shown in Figure 7–11. The input

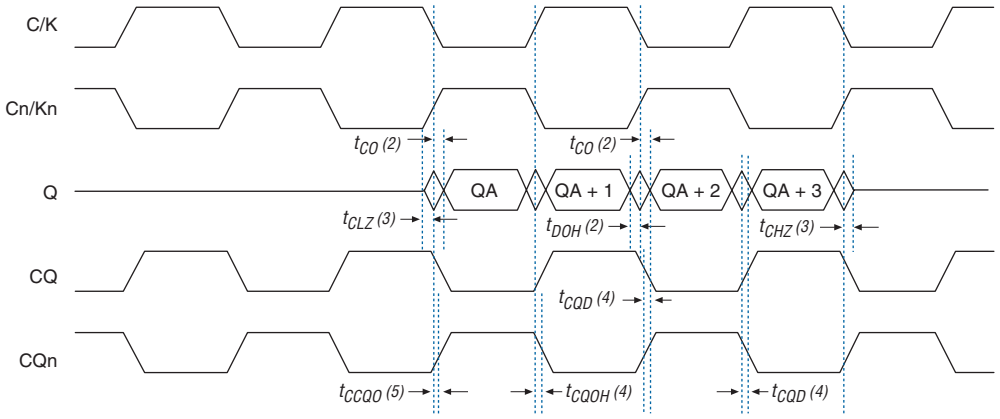
Figure 8–13. Cyclone II Memory Block in Independent Clock Mode *Note (1)*



Note to Figure 8–13:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Figure 9–5. Data & Clock Relationship During a QDRII SRAM Report



Notes to Figure 9–5:

(1) The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
(2) t_{CO} is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
(3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times, respectively.
(4) t_{CQD} is the skew between CQn and data edges.
(5) t_{CCQO} and t_{CQOH} are skew measurements between the C or C# clocks (or the K or K# clocks in single-clock mode) and the CQ or CQn clocks.

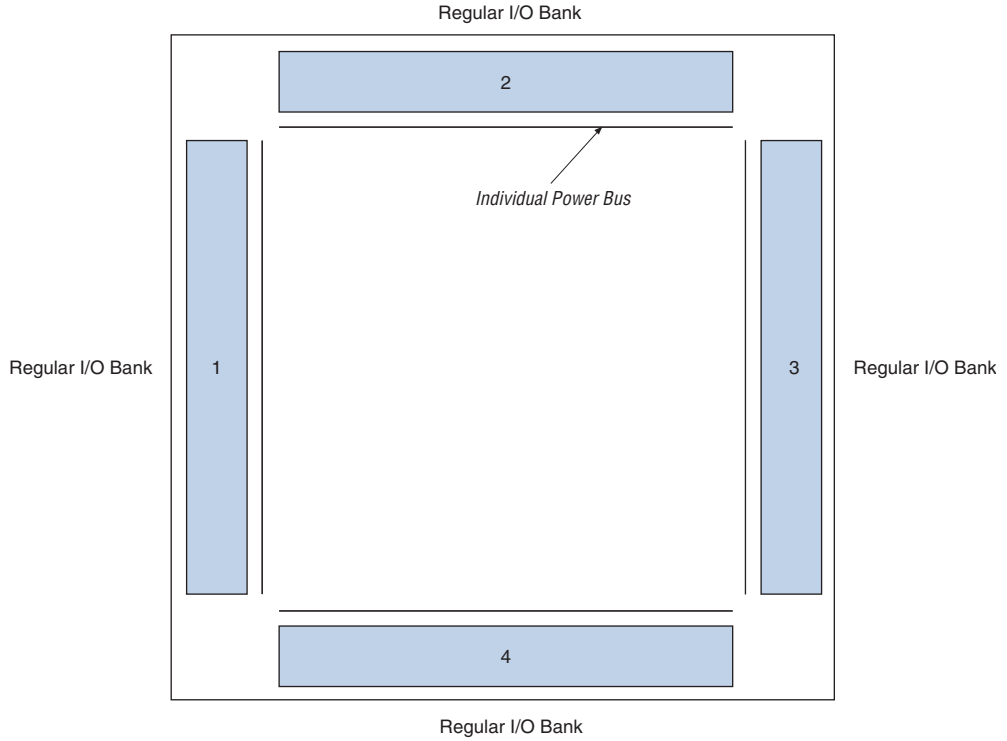
When writing to QDRII SRAM devices, the write clock generates the data while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

For information about the I/O standards supported for external memory applications, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(1)*	*(1)*	*(1)*
PCI and PCI-X *(2)*	Single ended	3.3 V	3.3 V	—	—	✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(3)*	*(4)*	2.5 V	—	—	—	✓	—
		2.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential SSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—		✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—

Figure 10–19. EP2C5 and EP2C8 Device I/O Banks *Notes (1), (2)*



Notes to Figure 10–19:

(1) This is a top view of the silicon die.

(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Additionally, each Cyclone II I/O bank has its own VCCIO pins. Any single I/O bank can only support one V_{CCIO} setting from among 1.5, 1.8, 2.5 or 3.3 V. Although there can only be one V_{CCIO} voltage per I/O bank, Cyclone II devices permit additional input signaling capabilities, as shown in Table 10–4.

Table 10–4. Acceptable Input Levels for LVTTL and LVCMOS

Bank V_{CCIO} (V)	Acceptable Input Levels (V)			
	3.3	2.5	1.8	1.5
3.3	✓	✓ (1)		
2.5	✓	✓		
1.8	✓ (2)	✓ (2)	✓	✓ (1)
1.5	✓ (2)	✓ (2)	✓	✓

Notes to Table 10–4:

(1) Because the input level does not drive to the rail, the input buffer does not completely shut off, and the I/O current is slightly higher than the default value.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on **Allow voltage overdrive for LVTTL/LVCMOS input pins** in Settings > Device > Device and Pin Options > Pin Placement tab. This setting allows input pins with LVTTL or LVCMOS I/O standards to be placed by the Quartus II software in an I/O bank with a lower V_{CCIO} voltage than the voltage specified by the pins.

Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank as long as they use compatible V_{CCIO} levels for input and output pins. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V LVTTL inputs and outputs, 2.5-V LVDS-compatible inputs and outputs, and 3.3-V LVCMOS inputs only.

Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value. For example, if you choose to implement both SSTL-2 and SSTL-18 in your Cyclone II device, I/O pins using these standards—because they require different V_{REF} values—must be in different banks from each other. However, the same I/O bank can support SSTL-2 and 2.5-V LVCMOS with the V_{CCIO} set to 2.5 V and the V_{REF} set to 1.25 V.

Refer to "Pad Placement and DC Guidelines" on page 10–27 for more information.

The number of embedded multipliers per column and the number of columns available increases with device density. Table 12–1 shows the number of embedded multipliers in each Cyclone II device and the multipliers that you can implement.

Table 12–1. Number of Embedded Multipliers in Cyclone II Devices

Device	Embedded Multipliers	9 × 9 Multipliers *(1)*	18 × 18 Multipliers *(1)*
EP2C5	13	26	13
EP2C8	18	36	18
EP2C20	26	52	26
EP2C35	35	70	35
EP2C50	86	172	86
EP2C70	150	300	150

Note to Table 12–1:
(1) Each device has either the number of 9 × 9 or 18 × 18 multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

In addition to the embedded multipliers, you can also implement soft multipliers using Cyclone II M4K memory blocks. The availability of soft multipliers increases the number of multipliers available within the device. Table 12–2 shows the total number of multipliers available in Cyclone II devices using embedded multipliers and soft multipliers.

Table 12–2. Number of Multipliers in Cyclone II Devices

Device	Embedded Multipliers (18 × 18)	Soft Multipliers (16 × 16) *(1)*	Total Multipliers *(2)*
EP2C5	13	26	39
EP2C8	18	36	54
EP2C20	26	52	78
EP2C35	35	105	140
EP2C50	86	129	215
EP2C70	150	250	400

Notes to Table 12–2:
(1) Soft multipliers are implemented in sum of multiplication mode. The M4K memory blocks are configured with 18-bit data widths to support 16-bit coefficients. The sum of the coefficients requires 18 bits of resolution to account for overflow.
(2) The total number of multipliers may vary according to the multiplier mode used.

If the configuration bitstream size exceeds the capacity of a serial configuration device, you must select a larger configuration device and/or enable the compression feature. When configuring multiple devices, the size of the bitstream is the sum of the individual devices' configuration bitstreams.

Configuring Multiple Cyclone II Devices with the Same Design

Certain designs require you to configure multiple Cyclone II devices with the same design through a configuration bitstream or SOF. You can do this through one of two methods, as described in this section. For both methods, the serial configuration devices cannot be cascaded or chained together.

Multiple SOFs

In the first method, two copies of the SOF file are stored in the serial configuration device. Use the first copy to configure the master Cyclone II device and the second copy to configure all remaining slave devices concurrently. In this setup, the master Cyclone II device is in AS mode, and the slave Cyclone II devices are in PS mode (MSEL=01). See Figure 13–5.

To configure four identical Cyclone II devices with the same SOF file, connect the three slave devices for concurrent configuration as shown in Figure 13–5. The nCEO pin from the master device drives the nCE input pins on all three slave devices. Connect the configuration device's DATA and DCLK pins to the Cyclone II device's DATA and DCLK pins in parallel. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding nCEO high. After completing its configuration cycle, the master drives nCE low and transmits the second copy of the configuration data to all three slave devices, configuring them simultaneously.

The advantage of using the setup in Figure 13–5 is that you can have a different SOF file for the Cyclone II master device. However, all the Cyclone II slave devices must be configured with the same SOF file. The SOF files in this configuration method can be either compressed or uncompressed.

You can still use this method if the master and slave Cyclone II devices use the same SOF.

You must connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. You should buffer the DCLK and DATA lines for every fourth device. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

Since all nSTATUS and CONF_DONE pins are connected, if any Cyclone II device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first Cyclone II detects an error, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single Cyclone II device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the Cyclone II devices release their nSTATUS pins after a reset time-out period (maximum of 40 µs). After all nSTATUS pins are released and pulled high, the MAX II device reconfigures the chain without pulsing nCONFIG low. If the **Auto-restart configuration after error** option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

If you want to delay the initialization of the devices in the chain, you can use the CLKUSR pin option. The CLKUSR pin allows you to control when your device enters user mode. This feature also allows you to control the order of when each device enters user mode by feeding a separate clock to each device's CLKUSR pin. By using the CLKUSR pins, you can choose any device in the multiple device chain to enter user mode first and have the other devices enter user mode at a later time.

Different device families may require a different number of initialization clock cycles. Therefore, if your multiple device chain consists of devices from different families, the devices may enter user mode at a slightly different time due to the different number of initialization clock cycles required. However, if the number of initialization clock cycles is similar across different device families or if the devices are from the same family, then the devices enter user mode at the same time. See the respective device family handbook for more information about the number of initialization clock cycles required.

it feeds the next device's nCE pin. After the first device in the chain completes configuration, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration. The nCEO pin is a dual-purpose pin in Cyclone II devices.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the device is in a chain, and the nCEO pin is connected to the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O pin after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

Connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Buffer the DCLK and DATA lines for every fourth device.

When configuring multiple devices, configuration does not begin until all devices release their OE or nSTATUS pins. Similarly, since all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

You should not pull CONF_DONE low to delay initialization. Instead, use the Quartus II software's **User-Supplied Start-Up Clock** option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain initialize together since their CONF_DONE pins are tied together.

Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if there is an error when configuring the first Cyclone II device, it resets the chain by pulling its nSTATUS pin low. This low signal drives the OE pin low on the enhanced configuration device and drives nSTATUS low on all FPGAs, which causes them to enter a reset state.

If the **Auto-restart configuration after error** option is turned on, the devices automatically initiate reconfiguration if an error occurs. The FPGAs release their nSTATUS pins after a reset time-out period (40 µs maximum). When all the nSTATUS pins are released and pulled high, the configuration device reconfigures the chain. If the **Auto-restart configuration after error** option is turned off, a microprocessor or controller must monitor the nSTATUS pin for errors and then pulse

For more information on how to use the USB-Blaster, MasterBlaster, ByteBlaster II or ByteBlasterMV cables, refer to the following documents:

- *USB-Blaster USB Port Download Cable Data Sheet*
- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlaster II Parallel Port Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*

JTAG Configuration

The Joint Test Action Group (JTAG) has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture allows you to test components on PCBs with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. The JTAG circuitry can also be used to shift configuration data into the device. The Quartus II software automatically generates SOF files that can be used for JTAG configuration with a download cable in the Quartus II programmer.

For more information on JTAG boundary-scan testing, see the following documents:

- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in Volume 2 of the *Cyclone II Device Handbook*
- Jam Programming & Testing Language Specification

Cyclone II devices are designed such that JTAG instructions have precedence over any device configuration modes. This means that JTAG configuration can take place without waiting for other configuration modes to complete. For example, if you attempt JTAG configuration of Cyclone II devices during PS configuration, PS configuration terminates and JTAG configuration begins. If the Cyclone II `MSEL` pins are set to AS or fast AS mode, the Cyclone II device does not output a `DCLK` signal when JTAG configuration takes place.

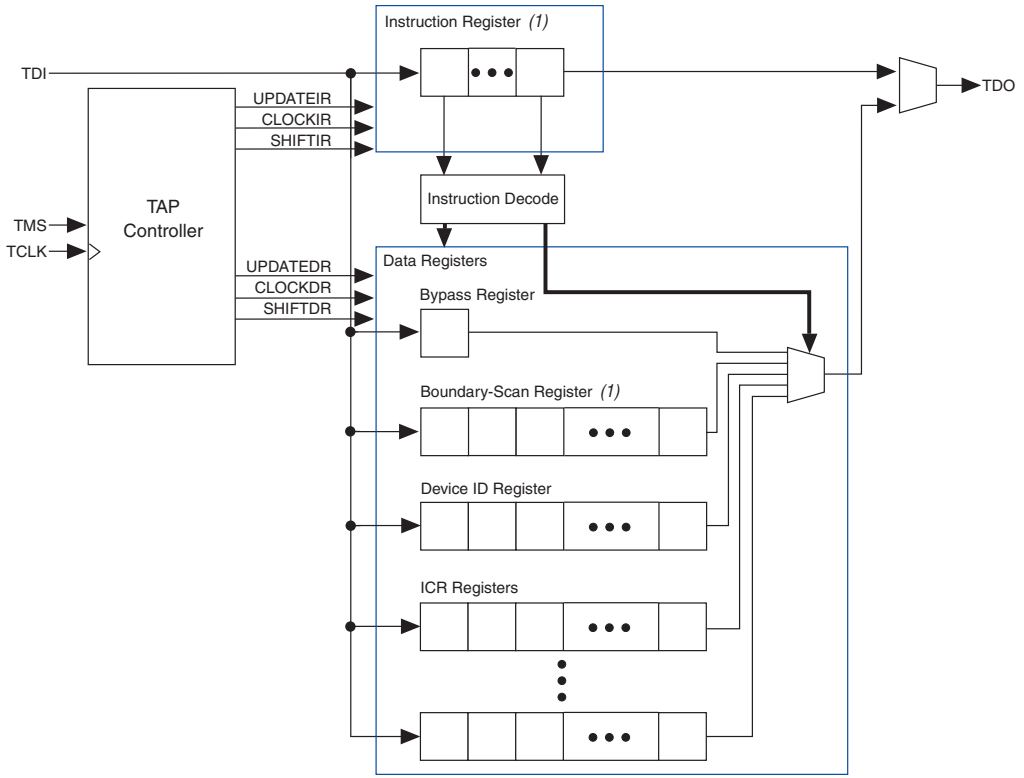
You cannot use the Cyclone II decompression feature if you are configuring your Cyclone II device when using JTAG-based configuration.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register determines the action to be performed and the data register to be accessed.
- The bypass register is a 1-bit-long data register that provides a minimum-length serial path between TDI and TDO.
- The boundary-scan register is a shift register composed of all the boundary-scan cells of the device.

Figure 14–2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 14–2. IEEE Std. 1149.1 Circuitry



Note to Figure 14–2:

(1) For register lengths, see the device data sheet in the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

IEEE Std. 1149.1 boundary-scan testing is controlled by a test access port (TAP) controller. For more information on the TAP controller, see "IEEE Std. 1149.1 BST Operation Control" on page 14–6. The TMS and TCK pins

If you are testing the device after configuring it, the programmable weak pull-up resister or the bus hold feature overrides the CLAMP value (the value stored in the update register of the boundary-scan cell) at the pin.

HIGHZ Instruction Mode

The HIGHZ instruction mode is used to set all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is loaded into the instruction register, the bypass register is connected between the TDI and TDO ports.

If you are testing the device after configuring it, the programmable weak pull-up resistor or the bus hold feature overrides the HIGHZ value at the pin.

I/O Voltage Support in JTAG Chain

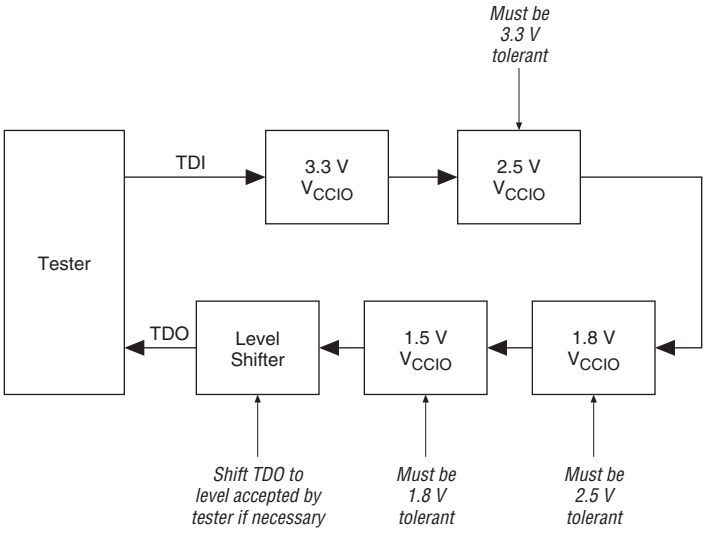
A JTAG chain can contain several different devices. However, you should be cautious if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specifications of the TDI pin it drives. For Cyclone II devices, the TDO pin is powered by the V_{CCIO} power supply. Since the V_{CCIO} supply is 3.3 V, the TDO pin drives out 3.3 V.

Devices can interface with each other although they might have different V_{CCIO} levels. For example, a device with a 3.3-V TDO pin can drive to a device with a 5.0-V TDI pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V TDI pin. JTAG pins on Cyclone II devices can support 2.5- or 3.3-V input levels.

For more information on MultiVolt I/O support, see the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook*.

You can also interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should be built such that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester. Figure 14–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 14–13. JTAG Chain of Mixed Voltages



Using IEEE Std. 1149.1 BST Circuitry

Cyclone II devices have dedicated JTAG pins, and the IEEE Std. 1149.1 BST circuitry is enabled upon device power-up. You can perform BST on Cyclone II FPGAs not only before and after configuration, but also during configuration. Cyclone II FPGAs support the BYPASS, IDCODE, and SAMPLE instructions during configuration without interrupting configuration. To send all other JTAG instructions, you must interrupt configuration using the CONFIG_IO instruction.

The CONFIG_IO instruction allows you to configure I/O buffers via the JTAG port, and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Cyclone II FPGA or waiting for a configuration device to complete configuration. Once configuration has been interrupted and JTAG BST is complete, the part must be reconfigured via JTAG (PULSE_CONFIG instruction) or by pulsing nCONFIG low.

When you perform JTAG boundary-scan testing before configuration, the nCONFIG pin must be held low.

The device-wide reset (DEV_CLRn) and device-wide output enable (DEV_OE) pins on Cyclone II devices do not affect JTAG boundary-scan or configuration operations. Toggling these pins does not disrupt BST operation any more than usual.