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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	142
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5q208i8

Dedicated Clock Pins

Larger Cyclone II devices (EP2C15 and larger devices) have 16 dedicated clock pins (CLK[15..0], four pins on each side of the device). Smaller Cyclone II devices (EP2C5 and EP2C8 devices) have eight dedicated clock pins (CLK[7..0], four pins on left and right sides of the device). These CLK pins drive the global clock network (GCLK), as shown in Figures 2–11 and 2–12.

If the dedicated clock pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the logic array using the MultiTrack interconnect. However, if they are used as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Dual-Purpose Clock Pins

Cyclone II devices have either 20 dual-purpose clock pins, DPCLK[19..0] or 8 dual-purpose clock pins, DPCLK[7..0]. In the larger Cyclone II devices (EP2C15 devices and higher), there are 20 DPCLK pins; four on the left and right sides and six on the top and bottom of the device. The corner CDPCLK pins are first multiplexed before they drive into the clock control block. Since the signals pass through a multiplexer before feeding the clock control block, these signals incur more delay to the clock control block than other DPCLK pins that directly feed the clock control block. In the smaller Cyclone II devices (EP2C5 and EP2C8 devices), there are eight DPCLK pins; two on each side of the device (see Figures 2–11 and 2–12).

A programmable delay chain is available from the DPCLK pin to its fan-out destinations. To set the propagation delay from the DPCLK pin to its fan-out destinations, use the **Input Delay from Dual-Purpose Clock Pin to Fan-Out Destinations** assignment in the Quartus II software.

These dual-purpose pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets, and clock enables, or protocol control signals such as TRDY and IRDY for PCI, or DQS signals for external memory interfaces.

Embedded multipliers can operate at up to 250 MHz (for the fastest speed grade) for 18 × 18 and 9 × 9 multiplications when using both input and output registers.

Each Cyclone II device has one to three columns of embedded multipliers that efficiently implement multiplication functions. An embedded multiplier spans the height of one LAB row. Table 2–10 shows the number of embedded multipliers in each Cyclone II device and the multipliers that can be implemented.

Table 2–10. Number of Embedded Multipliers in Cyclone II Devices *Note (1)*

Device	Embedded Multiplier Columns	Embedded Multipliers	9 × 9 Multipliers	18 × 18 Multipliers
EP2C5	1	13	26	13
EP2C8	1	18	36	18
EP2C15	1	26	52	26
EP2C20	1	26	52	26
EP2C35	1	35	70	35
EP2C50	2	86	172	86
EP2C70	3	150	300	150

Note to Table 2–10:

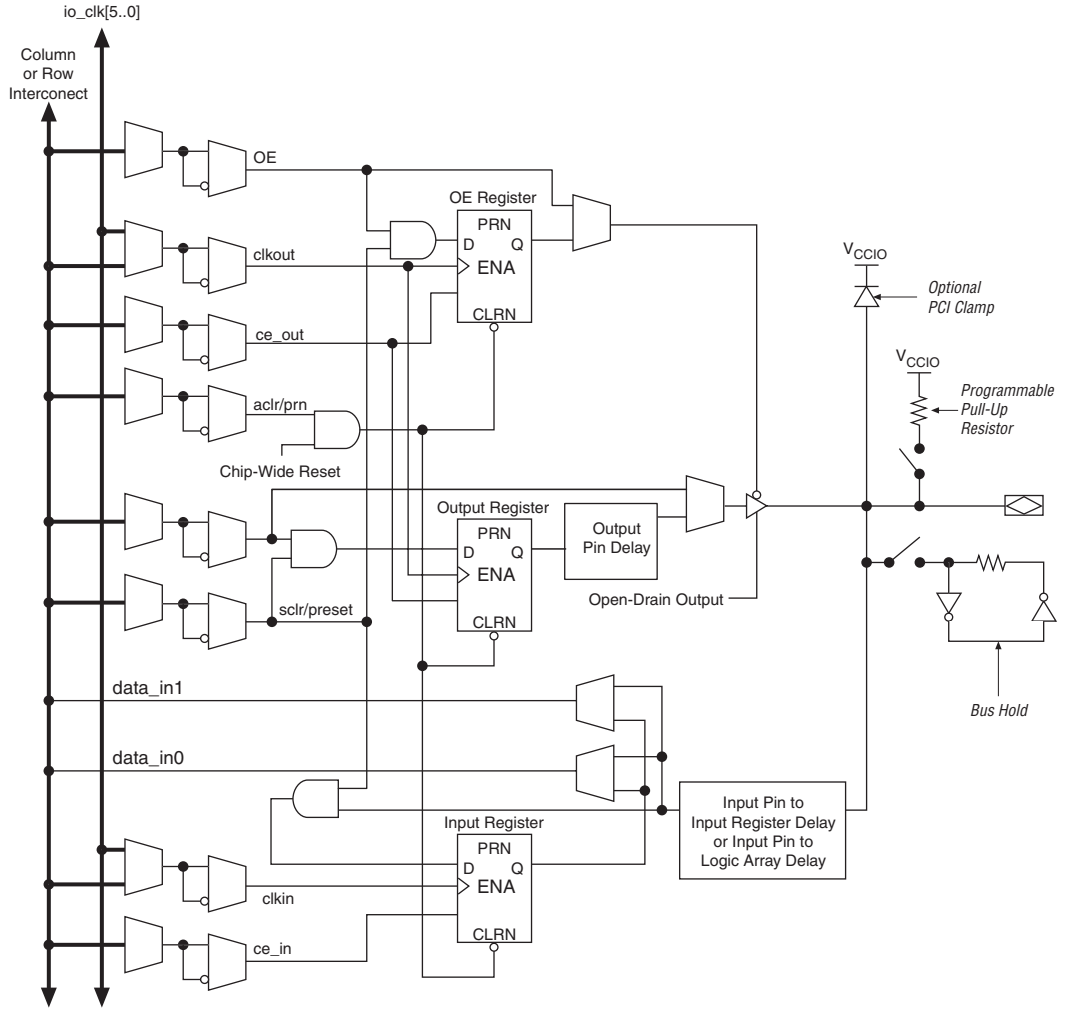
(1) Each device has either the number of 9 × 9-, or 18 × 18-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

The embedded multiplier consists of the following elements:

- Multiplier block
- Input and output registers
- Input and output interfaces

Figure 2–18 shows the multiplier block architecture.

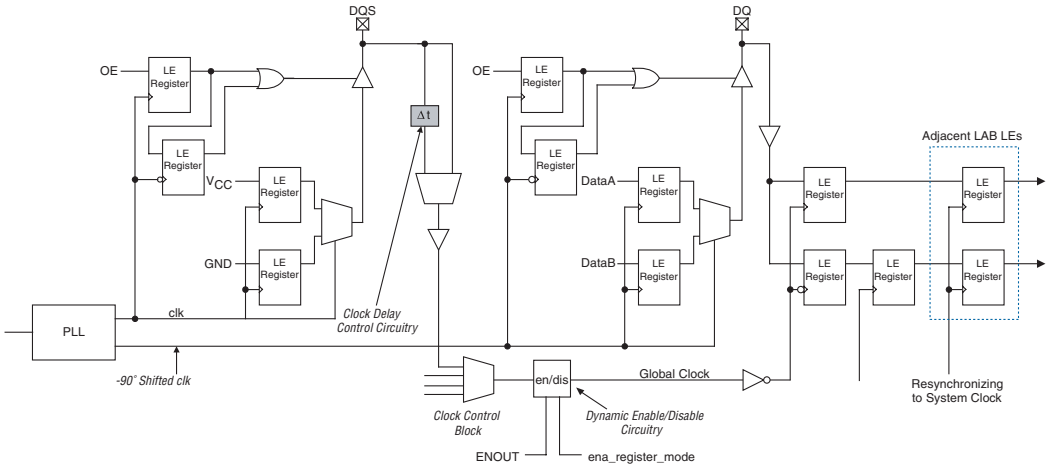
Figure 2–25. Cyclone II IOE in Bidirectional I/O Configuration



The Cyclone II device IOE includes programmable delays to ensure zero hold times, minimize setup times, or increase clock to output times.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays decrease input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time.

Figure 2–27. DDR SDRAM Interfacing



For more information on Cyclone II external memory interfaces, see the *External Memory Interfaces* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Table 5–7. DC Characteristics of User I/O Pins Using Single-Ended Standards Notes (1), (2) **(Part 2 of 2)**

I/O Standard	Test Conditions		Voltage Thresholds	
	I_{OL} (mA)	I_{OH} (mA)	Maximum V_{OL} (V)	Minimum V_{OH} (V)
1.5-V HSTL class I	8	–8	0.4	V_{CCIO} – 0.4
1.5V HSTL class II	16	–16	0.4	V_{CCIO} – 0.4

Notes to Table 5–7:

(1) The values in this table are based on the conditions listed in Tables 5–2 and 5–6.

(2) This specification is supported across all the programmable drive settings available as shown in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

Differential I/O Standards

The RSDS and mini-LVDS I/O standards are only supported on output pins. The LVDS I/O standard is supported on both receiver input pins and transmitter output pins.

For more information on how these differential I/O standards are implemented, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook*.

Figure 5–1 shows the receiver input waveforms for all differential I/O standards (LVDS, LVPECL, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Table 5–23. EP2C8/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.179	–0.189	0.089	0.047	0.045	0.055	ns

Notes to Table 5–23:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–24. EP2C8/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.256	1.314	2.270	2.416	2.596	2.606	ns
t_{COUT}	1.258	1.316	2.286	2.429	2.604	2.614	ns
t_{PLLCIN}	–0.276	–0.294	–0.08	–0.134	–0.152	–0.142	ns
$t_{PLLCOUT}$	–0.274	–0.292	–0.064	–0.121	–0.144	–0.134	ns

Notes to Table 5–24:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C15A Clock Timing Parameters

Tables 5–25 and 5–26 show the clock timing parameters for EP2C15A devices.

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

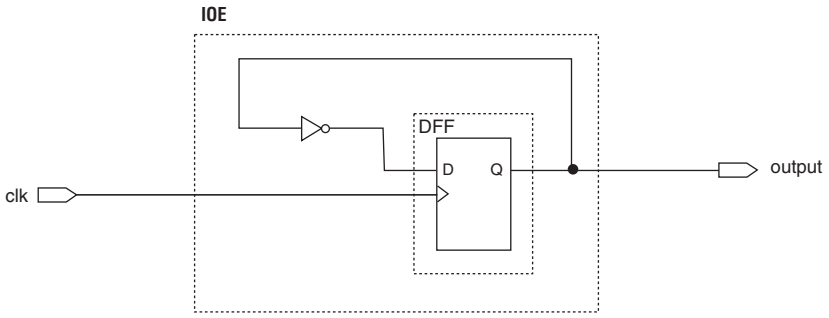
(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

DCD Measurement Techniques

DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 5–9). Therefore, any DCD present on the input clock signal, or caused by the clock input buffer, or different input I/O standard, does not transfer to the output signal.

Figure 5–9. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs



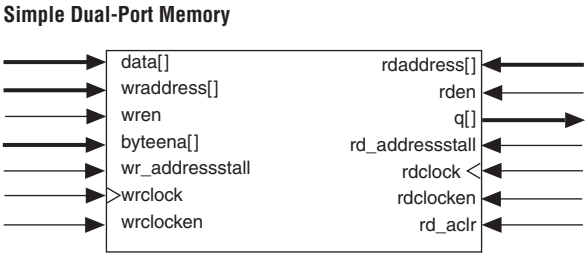
However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 5–10). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

Table 7–8 shows the clock sources connectivity to the global clock networks.

Table 7–8. Global Clock Network Connections (Part 1 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CLK0/LVDSCLK0p	✓		✓													
CLK1/LVDSCLK0n		✓	✓													
CLK2/LVDSCLK1p	✓			✓												
CLK3/LVDSCLK1n		✓		✓												
CLK4/LVDSCLK2p					✓		✓									
CLK5/LVDSCLK2n						✓	✓									
CLK6/LVDSCLK3p					✓			✓								
CLK7/LVDSCLK3n						✓		✓								
CLK8/LVDSCLK4n									✓		✓					
CLK9/LVDSCLK4p										✓	✓					
CLK10/LVDSCLK5n									✓			✓				
CLK11/LVDSCLK5p										✓		✓				
CLK12/LVDSCLK6n													✓		✓	
CLK13/LVDSCLK6p														✓	✓	
CLK14/LVDSCLK7n													✓			✓
CLK15/LVDSCLK7p														✓		✓
PLL1_c0	✓	✓		✓												
PLL1_c1	✓		✓	✓												
PLL1_c2		✓	✓													
PLL2_c0					✓	✓		✓								
PLL2_c1					✓		✓	✓								
PLL2_c2						✓	✓									
PLL3_c0									✓	✓		✓				
PLL3_c1									✓		✓	✓				
PLL3_c2										✓	✓					

Figure 8–8. Cyclone II Simple Dual-Port Mode *Note (1)*



Note to Figure 8–8:
(1) Simple dual-port RAM supports input and output clock mode in addition to the read and write clock mode shown.

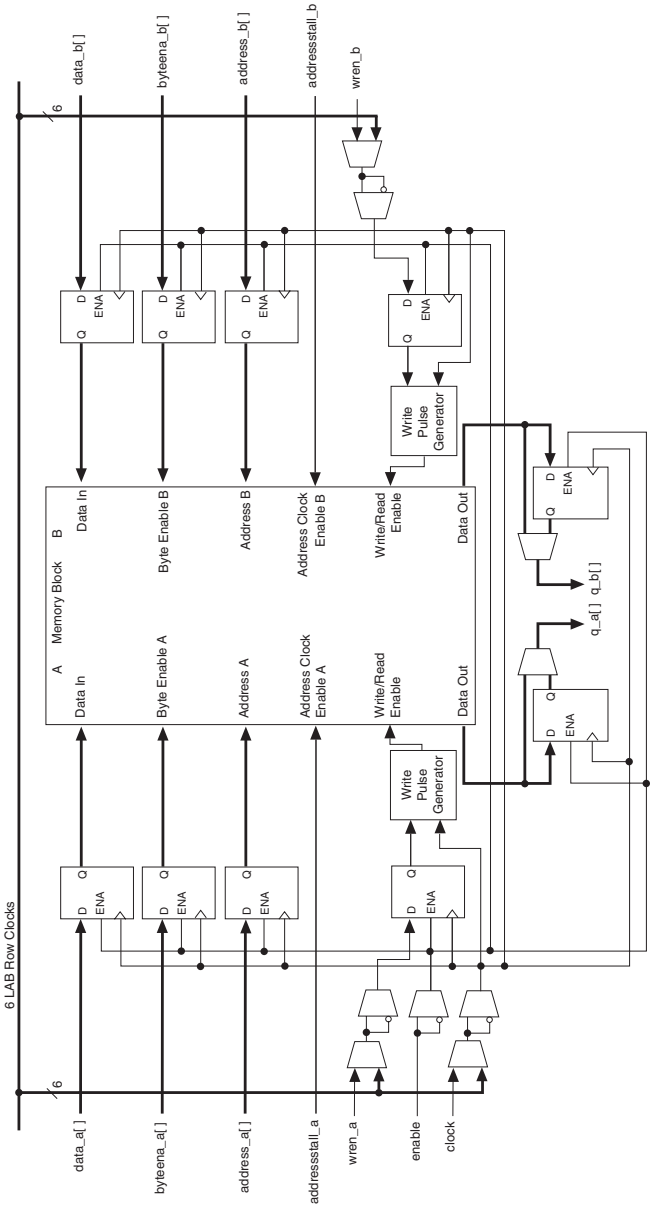
Cyclone II memory blocks support mixed-width configurations, allowing different read and write port widths. Tables 8–5 and 8–6 show the mixed-width configurations.

Table 8–5. Cyclone II Memory Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

In simple dual-port mode, the memory blocks have one write enable and one read enable signal. They do not support a clear port on the write enable and read enable registers. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is the old data stored at the memory

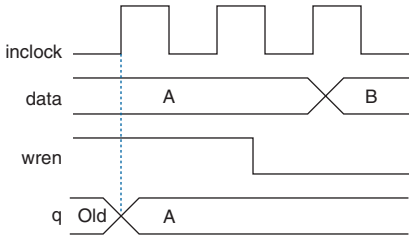
Figure 8–18. Cyclone II Single-Clock Mode in True Dual-Port Mode *Note (1)*



Note to Figure 8–18:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Figure 8–22. Cyclone II Same-Port Read-During-Write Functionality *Note (1)*



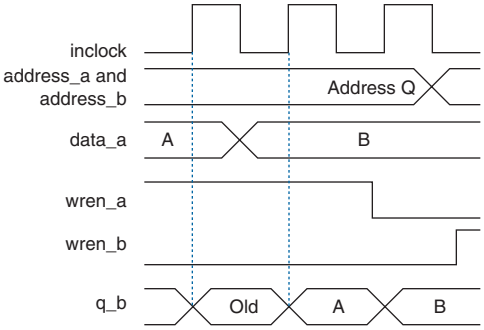
Note to Figure 8–22:
(1) Outputs are not registered.

Mixed-Port Read-During-Write Mode

This mode applies to a RAM in simple or true dual-port mode, which has one port reading and the other port writing to the same address location with the same clock.

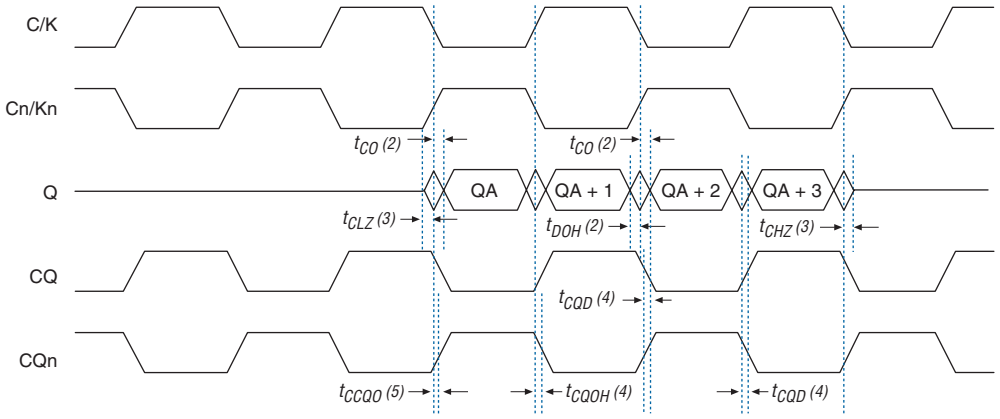
In this mode, you also have two output choices: old data or don't care. In Old Data Mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In Don't Care Mode, the same operation results in a "don't care" or unknown value on the RAM outputs.

Figure 8–23. Cyclone II Mixed-Port Read-During-Write: Old Data Mode *Note (1)*



Note to Figure 8–23:
(1) Outputs are not registered.

Figure 9–5. Data & Clock Relationship During a QDRII SRAM Report



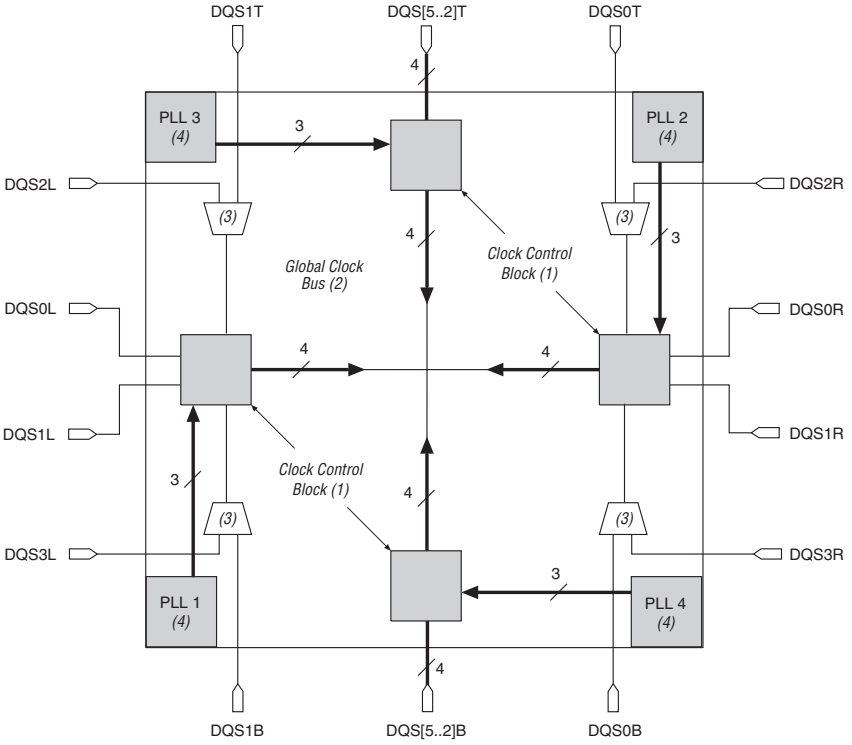
Notes to Figure 9–5:

(1) The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
(2) t_{CO} is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
(3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times, respectively.
(4) t_{CQD} is the skew between CQn and data edges.
(5) t_{CCQO} and t_{CQOH} are skew measurements between the C or C# clocks (or the K or K# clocks in single-clock mode) and the CQ or CQn clocks.

When writing to QDRII SRAM devices, the write clock generates the data while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

directly to the clock control block. For the larger Cyclone II devices, the corner DQS signals are multiplexed before they are routed to the clock control block. When you use the corner DQS pins for DDR implementation, there is a degradation in the performance of the memory interface. The clock control block is used to select from a number of input clock sources, in this case either PLL clock outputs or DQS pins, to drive onto the global clock bus. Figure 9–7 shows the corner DQS signal mappings for EP2C15 through EP2C70 devices.

Figure 9–7. Corner DQS Signal Mapping for EP2C15–EP2C70 Devices



Notes to Figure 9–7:

(1) There are four control blocks on each side.
(2) There are a total of 16 global clocks available.
(3) Only one of the corner DQS pins in each corner can feed the clock control block at a time. The other DQS pins can be used as general purpose I/O pins.
(4) PLL resource can be lost if all DQS pins from one side are used at the same time.
(5) Top/bottom and side IOE have different timing.

10. Selectable I/O Standards in Cyclone II Devices

CII51010-2.4

Introduction

The proliferation of I/O standards and the need for improved I/O performance have made it critical that low-cost devices have flexible I/O capabilities. Selectable I/O capabilities such as SSTL-18, SSTL-2, and LVDS compatibility allow Cyclone® II devices to connect to other devices on the same printed circuit board (PCB) that may require different operating and I/O voltages. With these aspects of implementation easily manipulated using the Altera® Quartus® II software, the Cyclone II device family allows you to use low cost FPGAs while keeping pace with increasing design complexity.

This chapter is a guide to understanding the input and output capabilities of the Cyclone II devices, including:

- Supported I/O standards
- Cyclone II I/O banks
- Programmable current drive strength
- I/O termination
- Pad placement and DC guidelines

For information on hot socketing, refer to the *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information on ESD specifications, refer to the *Altera Reliability Report*.

Supported I/O Standards

Cyclone II devices support the I/O standards shown in Table 10–1.

For more details on the I/O standards discussed in this section, including target data rates and voltage values for each I/O standard, refer to the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information about the I/O standards supported for external memory applications, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(1)*	*(1)*	*(1)*
PCI and PCI-X *(2)*	Single ended	3.3 V	3.3 V	—	—	✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(3)*	*(4)*	2.5 V	—	—	—	✓	—
		2.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential SSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—		✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—

Figure 10–1. SSTL-2 Class I Termination

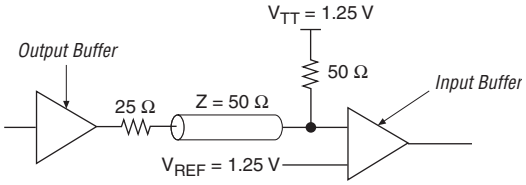
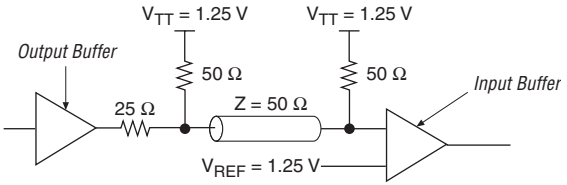


Figure 10–2. SSTL-2 Class II Termination



Cyclone II devices support both input and output SSTL-2 class I and II levels.

Pseudo-Differential SSTL-2

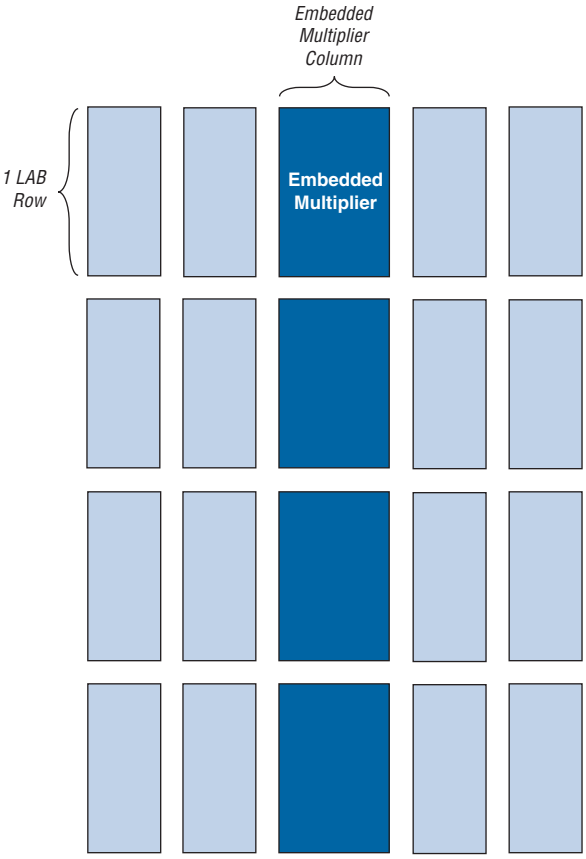
The differential SSTL-2 I/O standard (EIA/JEDEC standard JESD8-9A) is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard specifies an input voltage range of – 0.3 V ≤V_I ≤V_{CCIO} + 0.3 V. The differential SSTL-2 standard does not require an input reference voltage. Refer to Figures 10–3 and 10–4 for details on differential SSTL-2 terminations.

Cyclone II devices do not support true differential SSTL-2 standards. Cyclone II devices support pseudo-differential SSTL-2 outputs for `PLL_OUT` pins and pseudo-differential SSTL-2 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

Embedded Multiplier Block Overview

Each Cyclone II device has one to three columns of embedded multipliers that implement multiplication functions. Figure 12–1 shows one of the embedded multiplier columns with the surrounding LABs. Each embedded multiplier can be configured to support one 18 × 18 multiplier or two 9 × 9 multipliers.

Figure 12–1. Embedded Multipliers Arranged in Columns with Adjacent LABs



You must connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. You should buffer the DCLK and DATA lines for every fourth device. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

Since all nSTATUS and CONF_DONE pins are connected, if any Cyclone II device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first Cyclone II detects an error, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single Cyclone II device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the Cyclone II devices release their nSTATUS pins after a reset time-out period (maximum of 40 µs). After all nSTATUS pins are released and pulled high, the MAX II device reconfigures the chain without pulsing nCONFIG low. If the **Auto-restart configuration after error** option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

If you want to delay the initialization of the devices in the chain, you can use the CLKUSR pin option. The CLKUSR pin allows you to control when your device enters user mode. This feature also allows you to control the order of when each device enters user mode by feeding a separate clock to each device's CLKUSR pin. By using the CLKUSR pins, you can choose any device in the multiple device chain to enter user mode first and have the other devices enter user mode at a later time.

Different device families may require a different number of initialization clock cycles. Therefore, if your multiple device chain consists of devices from different families, the devices may enter user mode at a slightly different time due to the different number of initialization clock cycles required. However, if the number of initialization clock cycles is similar across different device families or if the devices are from the same family, then the devices enter user mode at the same time. See the respective device family handbook for more information about the number of initialization clock cycles required.

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 2 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nSTATUS	N/A	All	Bidirectional open-drain	The Cyclone II device drives nSTATUS low immediately after power-up and releases it after the POR time. This pin provides a status output and input for the Cyclone II device. If the Cyclone II device detects an error during configuration, it drives the nSTATUS pin low to stop configuration. If an external source (for example, another Cyclone II device) drives the nSTATUS pin low during configuration or initialization, the target device enters an error state. Driving nSTATUS low after configuration and initialization does not affect the configured device. If your design uses a configuration device, driving nSTATUS low causes the configuration device to attempt to configure the FPGA, but since the FPGA ignores transitions on nSTATUS in user mode, the FPGA does not reconfigure. To initiate a reconfiguration, pull the nCONFIG pin low. The enhanced configuration devices' and EPC2 devices' OE and nCS pins are connected to the Cyclone II device's nSTATUS and CONF_DONE pins, respectively, and have optional internal programmable pull-up resistors. If you use these internal pull-up resistors on the enhanced configuration device, do not use external 10-kΩ pull-up resistors on these pins. When using EPC2 devices, you should only use external 10-kΩ pull-up resistors. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.

to external device data via the PIN_IN signal, while the update registers connect to external data through the PIN_OUT and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 14–4 shows the Cyclone II device's user I/O boundary-scan cell.

Figure 14–4. Cyclone II Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry