Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	89
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5t144c6

Advanced I/O Standard Support

Table 2–17 shows the I/O standards supported by Cyclone II devices and which I/O pins support them.

Table 2–17. Cyclone II Supported I/O Standards & Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top & Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS *(1)*	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(2)*	*(2)*	*(2)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(2)*	*(2)*	*(2)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(2)*	*(2)*	*(2)*
PCI and PCI-X *(1) (3)*	Single ended	3.3 V	3.3 V			✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(4)*	*(5)*	2.5 V				✓	
		2.5 V	*(5)*	✓ *(6)*		✓ *(6)*		
Differential SSTL-18 class I or class II	Pseudo differential *(4)*	*(5)*	1.8 V				✓ *(7)*	
		1.8 V	*(5)*	✓ *(6)*		✓ *(6)*		

standards (e.g., SSTL-2) independently. If an I/O bank does not use voltage-referenced standards, the VREF pins are available as user I/O pins.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs. Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value.

MultiVolt I/O Interface

The Cyclone II architecture supports the MultiVolt I/O interface feature, which allows Cyclone II devices in all packages to interface with systems of different supply voltages. Cyclone II devices have one set of V_{CC} pins (VCCINT) that power the internal device logic array and input buffers that use the LVPECL, LVDS, HSTL, or SSTL I/O standards. Cyclone II devices also have four or eight sets of VCC pins (VCCIO) that power the I/O output drivers and input buffers that use the LVTTL, LVCMOS, or PCI I/O standards.

The Cyclone II VCCINT pins must always be connected to a 1.2-V power supply. If the V_{CCINT} level is 1.2 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V systems. Table 2–20 summarizes Cyclone II MultiVolt I/O support.

Table 2–20. Cyclone II MultiVolt I/O Support (Part 1 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
1.5	✓	✓	✓ *(2)*	✓ *(2)*	✓			
1.8	✓ *(4)*	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓		
2.5			✓	✓	✓ *(5)*	✓ *(5)*	✓	

Document Revision History

Table 3–5 shows the revision history for this document.

Table 3–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.2	• Added document revision history. • Added new handpara nore in "IEEE Std. 1149.1 (JTAG) Boundary Scan Support" section. • Updated "Cyclone II Automated Single Event Upset Detection" section.	• Added information about limitation of cascading multi devices in the same JTAG chain. • Corrected information on CRC calculation.
July 2005 v2.0	Updated technical content.	
February 2005 v1.2	Updated information on JTAG chain limitations.	
November 2004 v1.1	Updated Table 3–4.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

Altera has ensured by design of the I/O buffers and hot-socketing circuitry, that Cyclone II devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone II Devices

The hot-socketing feature turns off the output buffer during power up (either V_{CCINT} or V_{CCIO} supplies) or power down. The hot-socket circuit generates an internal HOTSCKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. Designs cannot use the HOTSCKT signal for other purposes. The HOTSCKT signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When V_{CC} ramps up slowly, V_{CC} is still relatively low even after the internal POR signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tristated at this low V_{CC} voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are able to operate during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 4–1.

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 1 of 2)

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Unit
V_{IN}	Input voltage	*(1)*, *(2)*		–0.5	—	4.0	V
I_i	Input pin leakage current	$V_{IN} = V_{CCIOmax}$ to 0 V *(3)*		–10	—	10	µA
V_{OUT}	Output voltage	—		0	—	V_{CCIO}	V
I_{OZ}	Tri-stated I/O pin leakage current	$V_{OUT} = V_{CCIOmax}$ to 0 V *(3)*		–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_{IN} = ground, no load, no toggling inputs T_J = 25° C Nominal V_{CCINT}	EP2C5/A	—	0.010	*(4)*	A
			EP2C8/A	—	0.017	*(4)*	A
			EP2C15A	—	0.037	*(4)*	A
			EP2C20/A	—	0.037	*(4)*	A
			EP2C35	—	0.066	*(4)*	A
			EP2C50	—	0.101	*(4)*	A
			EP2C70	—	0.141	*(4)*	A
I_{CCIO0}	V_{CCIO} supply current (standby)	V_{IN} = ground, no load, no toggling inputs T_J = 25° C V_{CCIO} = 2.5 V	EP2C5/A	—	0.7	*(4)*	mA
			EP2C8/A	—	0.8	*(4)*	mA
			EP2C15A	—	0.9	*(4)*	mA
			EP2C20/A	—	0.9	*(4)*	mA
			EP2C35	—	1.3	*(4)*	mA
			EP2C50	—	1.3	*(4)*	mA
			EP2C70	—	1.7	*(4)*	mA

Table 5–19. M4K Block Internal Timing Microparameters (Part 3 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Notes to Table 5–19:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Cyclone II Clock Timing Parameters

Refer to Tables 5–20 through 5–34 for Cyclone II clock timing parameters.

Table 5–20. Cyclone II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2C5/A Clock Timing Parameters

Tables 5–21 and 5–22 show the clock timing parameters for EP2C5/A devices.

Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.283	1.343	2.329	2.484	2.688	2.688	ns
t_{COUT}	1.297	1.358	2.363	2.516	2.717	2.717	ns
t_{PLLCIN}	–0.188	–0.201	0.076	0.038	0.042	0.052	ns

The loop filter converts these up and down signals to a voltage that is used to bias the VCO. If the charge pump receives a logic high on the up signal, current is driven into the loop filter. If the charge pump receives a logic high on the down signal, current is drawn from the loop filter. The loop filter filters out glitches from the charge pump and prevents voltage over-shoot, which minimizes the jitter on the VCO.

The voltage from the charge pump determines how fast the VCO operates. The VCO is implemented as an four-stage differential ring oscillator. A divide counter, *m*, is inserted in the feedback loop to increase the VCO frequency above the input reference frequency, making the VCO frequency $f_{VCO} = m \times f_{REF}$. Therefore, the feedback clock, f_{FB}, applied to one input of the PFD, is locked to the input reference clock, f_{REF} (f_{IN}/n), applied to the other input of the PFD.

The VCO output can feed up to three post-scale counters (c0, c1, and c2). These post-scale counters allow a number of harmonically related frequencies to be produced by the PLL.

Additionally, Cyclone II PLLs have internal delay elements to compensate for routing on the global clock networks and I/O buffers. These internal delays are fixed and not accessible to the user.

Figure 7–2 shows a simplified block diagram of the major components of a Cyclone II device PLL.

The VCO frequency is a critical parameter that must be between 300 and 1,000 MHz to ensure proper operation of the PLL. The Quartus II software automatically sets the VCO frequency within the recommended range based on the clock output and phase-shift requirements in your design.

PLL Reference Clock Generation

In Cyclone II devices, up to four clock pins can drive the PLL, as shown in Figure 7–11 on page 7–26. The multiplexer output feeds the PLL reference clock input. The PLL has internal delay elements that compensate for the clock delay from the input pin to the clock input port of the PLL.

Table 7–3 shows the clock input pin connections to the PLLs in the Cyclone II device.

Table 7–3. PLL Clock Input Pin Connections

Device	PLL 1		PLL 2		PLL 3		PLL 4	
	CLK0 CLK1	CLK2 CLK3	CLK4 CLK5	CLK6 CLK7	CLK8 CLK9	CLK10 CLK11	CLK12 CLK13	CLK14 CLK15
EP2C5	✓	✓	✓	✓				
EP2C8	✓	✓	✓	✓				
EP2C15	✓	✓	✓	✓	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓	✓	✓	✓	✓

Each PLL can be fed by one of four single-ended or two differential clock input pins. For example, PLL 1 can be fed by `CLK[3..0]` when using a single-ended I/O standard. When your design uses a differential I/O standard, these same clock pins have a secondary function as `LVDSCLK[2..1]p` and `LVDSCLK[2..1]n` pins. When using differential clocks, the `CLK0` pin's secondary function is `LVDSCLK1p`, the `CLK1` pin's secondary function is `LVDSCLK1n`, etc.

Phase-Shifting Implementation

Cyclone II devices use fine or coarse phase shifts for clock delays because they are more efficient than delay elements and are independent of process, voltage, and temperature.

Phase shift is implemented by using a combination of the VCO phase output and the counter starting time. The VCO phase taps and counter starting time are independent of process, voltage, and temperature. The VCO phase taps allow you to phase shift the Cyclone II PLL output clocks with fine resolution. The counter starting time allows you to phase shift the Cyclone II PLL output clocks with coarse resolution.

Fine-resolution phase shifting is implemented using any of the eight VCO phases for the output counters (`c[2..0]`) or the feedback counter (*m*) reference clock. This provides the finest resolution for phase shift. The minimum delay time that may be inserted using this method is defined by the equation:

$$\Delta t_{FINE} = \frac{1}{8} t_{VCO} = \frac{1}{8 \times f_{VCO}} = \frac{n}{8 \times m \times f_{IN}}$$

f_{IN} is input reference clock frequency.

For example, if f_{IN} is 100 MHz, *n* is 1 and *m* is 8, then f_{VCO} is 800 MHz and Δt is 156.25 ps. This delay time is defined by the PLL operating frequency which is governed by the reference clock and the counter settings.

The second way to implement phase shifts is by delaying the start of the *m* and post-scale counters for a predetermined number of counter clocks. This delay time may be expressed as:

$$\Delta t_{COARSE} = \frac{S - 1}{f_{VCO}} = \frac{(S - 1) \times n}{m \times f_{IN}}$$

where S is the value set for the counter starting time. The counter starting time is called the **Initial** setting in the PLL Usage section of the compilation report in the Quartus II software.

Figure 7–8 shows an example of delay insertion using these two methods. The eight phases from the VCO are shown and labeled for reference. For this example, `OUTCLK0` is based off the 0° phase from the VCO and has the S value for the counter set to 1. It is divided by 4 (two VCO clocks for high time and two VCO clocks for low time). `OUTCLK1` is based off the 135° phase tap from the VCO and also has the S value for the counter set to 1. It is also divided by 4. In this case, the two clocks are offset by three

Table 7–8. Global Clock Network Connections (Part 3 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DPCLK3 *(1)*																✓

Notes to Table 7–8:
(1) See the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook* for more information on DPCLK pins.
(2) This pin only applies to EP2C5 and EP2C8 devices.
(3) These pins only apply to EP2C15 devices and larger. Only one of the two CDPCLK pins can feed the clock control block. The other pin can be used as a regular I/O pin.

If the dedicated clock pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the logic array using the MultiTrack interconnect. However, if they are used as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Clock Control Block

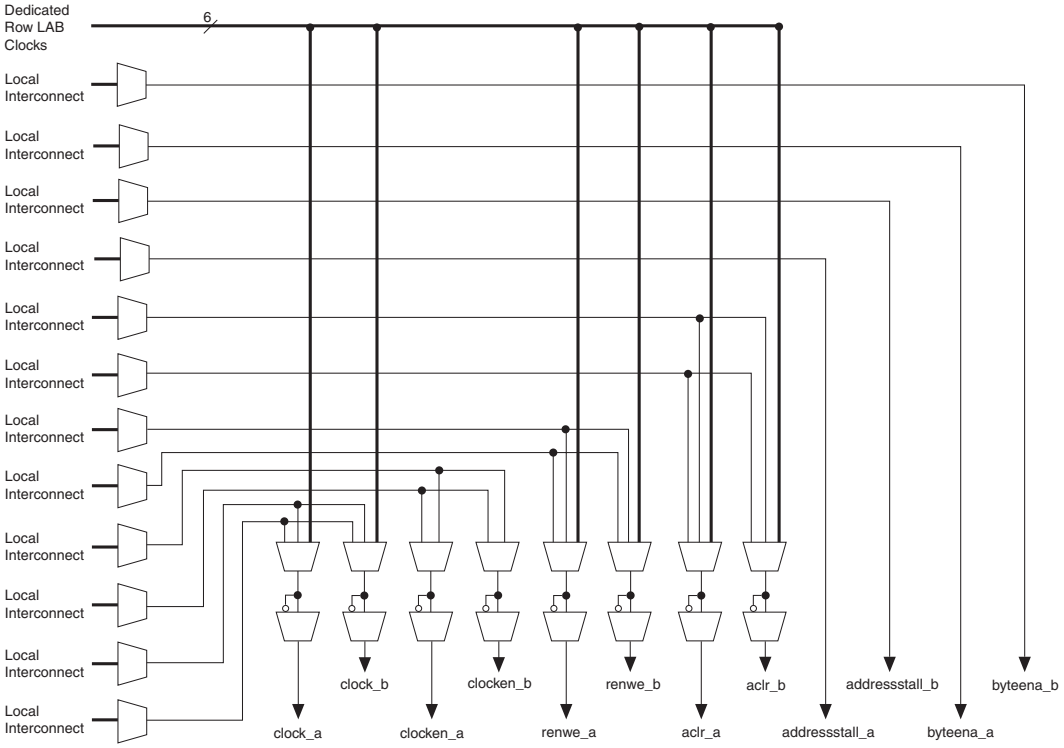
Every global clock network is driven by a clock control block residing either on the top, bottom, left, or right side of the Cyclone II device. The global clock network has been optimized for minimum clock skew and delay.

Table 7–9 lists the sources that can feed the clock control block, which in turn feeds the global clock networks.

Table 7–9. Clock Control Block Inputs (Part 1 of 2)

Input	Description
Dedicated clock inputs	Dedicated clock input pins can drive clocks or global signals, such as asynchronous clears, presets, or clock enables onto a given global clock network.
Dual-purpose clock (DPCLK and CDPCLK) I/O inputs	DPCLK and CDPCLK I/O pins are bidirectional dual function pins that can be used for high fan-out control signals, such as protocol signals, TRDY and IRDY signals for PCI, or DQS for DDR, via the global clock network.

Figure 8–1. M4K Control Signal Selection



Parity Bit Support

Error detection using parity check is possible using the parity bit, with additional logic implemented in LEs to ensure data integrity. Parity-size data words can also be used for other purposes such as storing user-specified control bits.

Refer to the *Using Parity to Detect Errors White Paper* for more information.

Byte Enable Support

All M4K memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable (`wren`) signals, along with the byte enable (`byteena`) signals, control the RAM block's write operations. The default value for the byte enable signals is high (enabled), in which

Figure 8–4. Cyclone II Address Clock Enable During Read Cycle Waveform

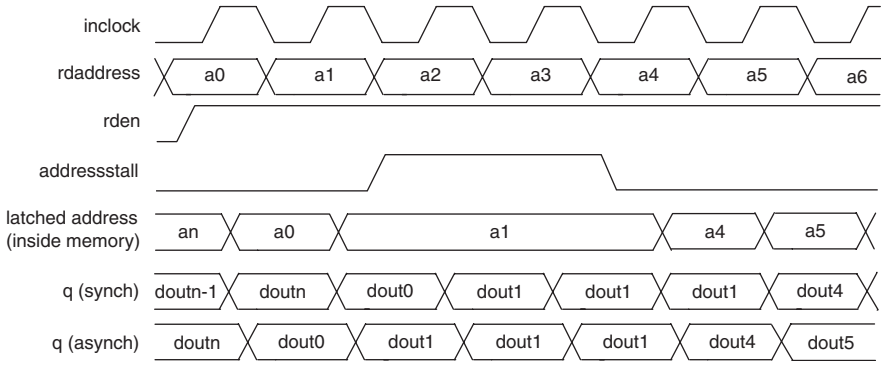
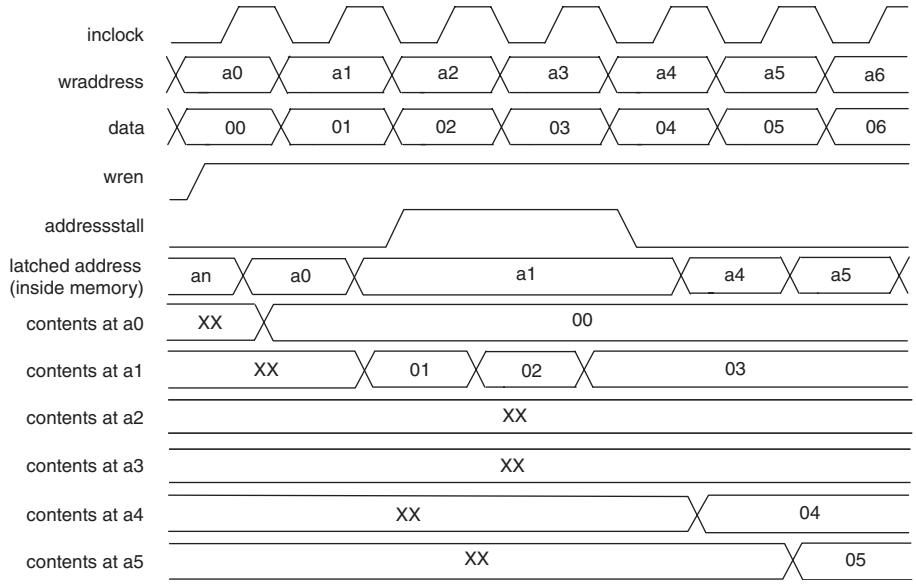


Figure 8–5. Cyclone II Address Clock Enable During Write Cycle Waveform



Memory Modes

Cyclone II M4K memory blocks include input registers that synchronize writes and output registers to pipeline data, thereby improving system performance. All M4K memory blocks are fully synchronous, meaning that you must send all inputs through a register, but you can either send outputs through a register (pipelined) or bypass the register (flow-through).

Input/Output Clock Mode

Cyclone II memory blocks can implement the input/output clock mode for true and simple dual-port memory. On each of the two ports, A and B, one clock controls all registers for the data, write enable, and address inputs into the memory block. The other clock controls the blocks' data output registers. Each memory block port also supports independent clock enables for input and output registers. Asynchronous clear signals for the registers are not supported.

Figures 8–14 through 8–16 show the memory block in input/output clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

Figure 10–1. SSTL-2 Class I Termination

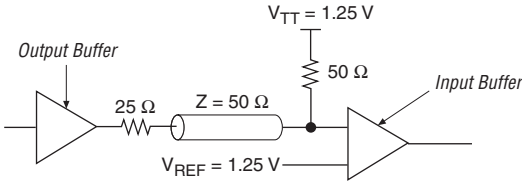
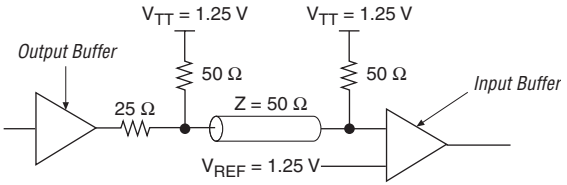


Figure 10–2. SSTL-2 Class II Termination



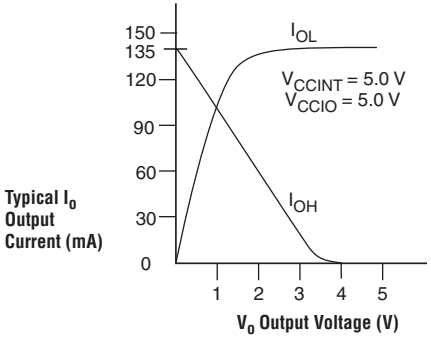
Cyclone II devices support both input and output SSTL-2 class I and II levels.

Pseudo-Differential SSTL-2

The differential SSTL-2 I/O standard (EIA/JEDEC standard JESD8-9A) is a 2.5-V standard used for applications such as high-speed DDR SDRAM clock interfaces. This standard supports differential signals in systems using the SSTL-2 standard and supplements the SSTL-2 standard for differential clocks. The differential SSTL-2 standard specifies an input voltage range of – 0.3 V ≤V_I ≤V_{CCIO} + 0.3 V. The differential SSTL-2 standard does not require an input reference voltage. Refer to Figures 10–3 and 10–4 for details on differential SSTL-2 terminations.

Cyclone II devices do not support true differential SSTL-2 standards. Cyclone II devices support pseudo-differential SSTL-2 outputs for `PLL_OUT` pins and pseudo-differential SSTL-2 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

Figure 10–22. Output Drive Characteristics of a 5.0-V Device



As shown above, R_1 = 5.0-V/135 mA.

The values shown in data sheets usually reflect typical operating conditions. Subtract 20% from the data sheet value for guard band. This subtraction when applied in the example in Figure 10–22 gives R_1 a value of 30 Ω

R_2 should be selected so that it does not violate the driving device's I_{OH} specification. For example, if the device has a maximum I_{OH} of 8 mA, given that the PCI clamping diode, $V_{IN} = V_{CCIO} + 0.7\text{-V} = 3.7\text{-V}$, and the maximum supply load of a 5.0-V device (V_{CC}) is 5.25-V, the value of R_2 can be calculated as follows:

$$R_2 = \frac{(5.25\ V - 3.7\ V) - (8\ mA \times 30\ \Omega)}{8\ mA} = 164\ \Omega$$

This analysis assumes worst case conditions. If your system does not have a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because 5.0-V device tolerance in Cyclone II devices requires use of the PCI clamp, and this clamp is activated during configuration, 5.0-V signals may not be driven into the device until it is configured.

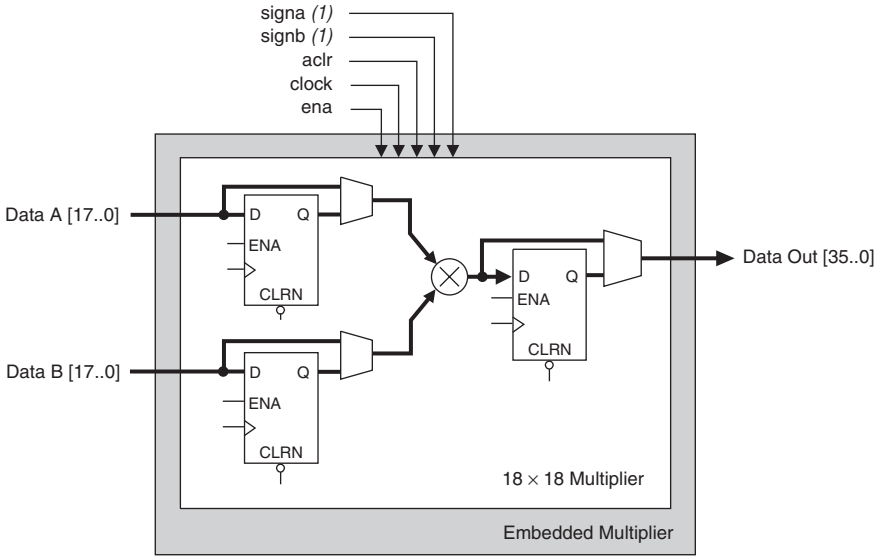
Conclusion

Cyclone II device I/O capabilities enable you to keep pace with increasing design complexity utilizing a low-cost FPGA device family. Support for I/O standards including SSTL and LVDS compatibility allow Cyclone II devices to fit into a wide variety of applications. The Quartus II

18-Bit Multipliers

Each embedded multiplier can be configured to support a single 18 × 18 multiplier for input widths from 10- to 18-bits. Figure 12–3 shows the embedded multiplier configured to support an 18-bit multiplier.

Figure 12–3. 18-Bit Multiplier Mode



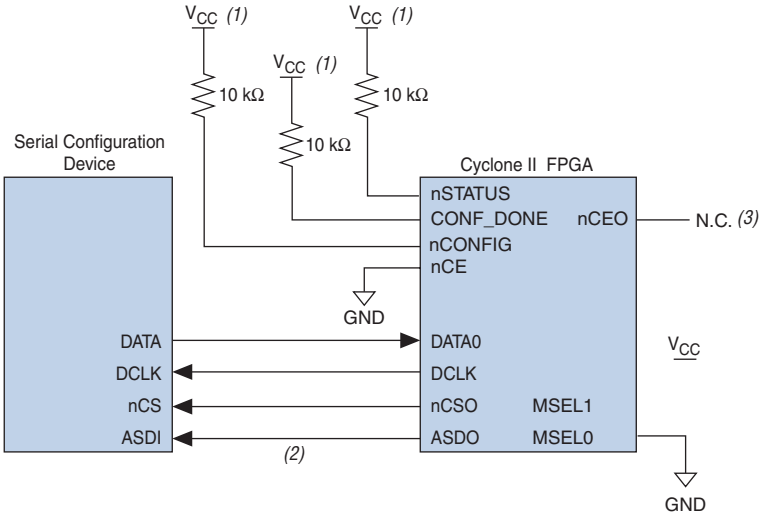
Note to Figure 12–3:
(1) If necessary, you can send these signals through one register to match the data signal path.

All 18-bit multiplier inputs and results can be independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers or a combination of both. Additionally, you can change the `signa` and `signb` signals dynamically and can send these signals through dedicated input registers.

9-Bit Multipliers

Each embedded multiplier can also be configured to support two 9 × 9 independent multipliers for input widths up to 9-bits. Figure 12–4 shows the embedded multiplier configured to support two 9-bit multipliers.

Figure 13–3. Single Device AS Configuration



Notes to Figure 13–3:

(1) Connect the pull-up resistors to a 3.3-V supply.

(2) Cyclone II devices use the ASDO to ASDI path to control the configuration device.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

Upon power-up, the Cyclone II device goes through a POR. During POR, the device resets, holds nSTATUS and CONF_DONE low, and tri-states all user I/O pins. After POR, which typically lasts 100 ms, the Cyclone II device releases nSTATUS and enters configuration mode when the external 10-kΩ resistor pulls the nSTATUS pin high. Once the FPGA successfully exits POR, all user I/O pins continue to be tri-stated. Cyclone II devices have weak pull-up resistors on the user I/O pins which are on before and during configuration.

The value of the weak pull-up resistors on the I/O pins that are on before and during configuration are available in the *DC Characteristics & Timing Specifications* chapter of the *Cyclone II Device Handbook*.

The configuration cycle consists of the reset, configuration, and initialization stages.

it feeds the next device's nCE pin. After the first device in the chain completes configuration, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration. The nCEO pin is a dual-purpose pin in Cyclone II devices.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the device is in a chain, and the nCEO pin is connected to the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O pin after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

Connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Buffer the DCLK and DATA lines for every fourth device.

When configuring multiple devices, configuration does not begin until all devices release their OE or nSTATUS pins. Similarly, since all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

You should not pull CONF_DONE low to delay initialization. Instead, use the Quartus II software's **User-Supplied Start-Up Clock** option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain initialize together since their CONF_DONE pins are tied together.

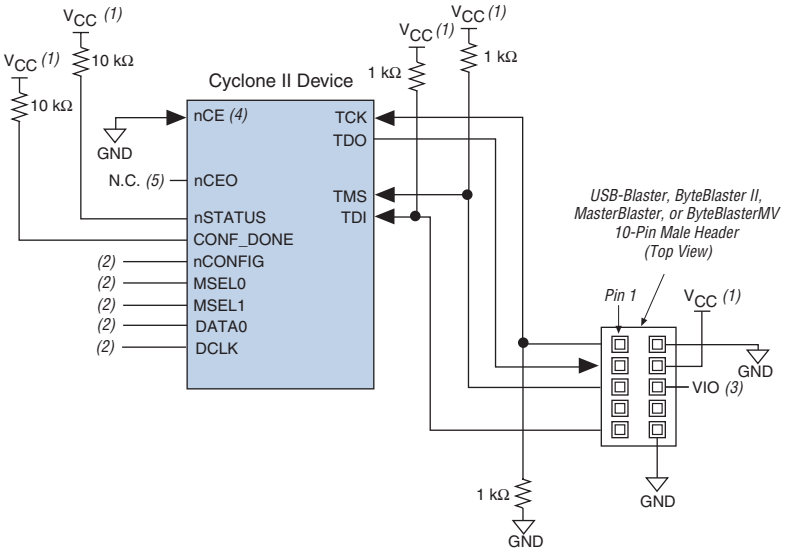
Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if there is an error when configuring the first Cyclone II device, it resets the chain by pulling its nSTATUS pin low. This low signal drives the OE pin low on the enhanced configuration device and drives nSTATUS low on all FPGAs, which causes them to enter a reset state.

If the **Auto-restart configuration after error** option is turned on, the devices automatically initiate reconfiguration if an error occurs. The FPGAs release their nSTATUS pins after a reset time-out period (40 µs maximum). When all the nSTATUS pins are released and pulled high, the configuration device reconfigures the chain. If the **Auto-restart configuration after error** option is turned off, a microprocessor or controller must monitor the nSTATUS pin for errors and then pulse

Single Device JTAG Configuration

During JTAG configuration, you can use the USB-Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV download cable to download data to the device. Configuring Cyclone II devices through a cable is similar to programming devices in system. Figure 13–22 shows JTAG configuration of a single Cyclone II device using a download cable.

Figure 13–22. JTAG Configuration of a Single Device Using a Download Cable



Notes to Figure 13–22:

(1) The pull-up resistor should be connected to the same supply voltage as the USB-Blaster, MasterBlaster (VIO pin), ByteBlaster II, or ByteBlasterMV cable.

(2) Connect the nCONFIG and MSEL[1..0] pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the nCONFIG pin to V_{CC}, and the MSEL[1..0] pins to ground. In addition, pull DCLK and DATA0 to either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) nCE must be connected to GND or driven low for successful JTAG configuration.

(5) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

To configure a single device in a JTAG chain, the programming software places all other devices in BYPASS mode. In BYPASS mode, Cyclone II devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally. This scheme

frequency (up to 40 MHz), which reduces your configuration time. In addition, Cyclone II devices can receive a compressed configuration bitstream and decompress this data on-the-fly in the AS or PS configuration scheme, which further reduces storage requirements and configuration time.