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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

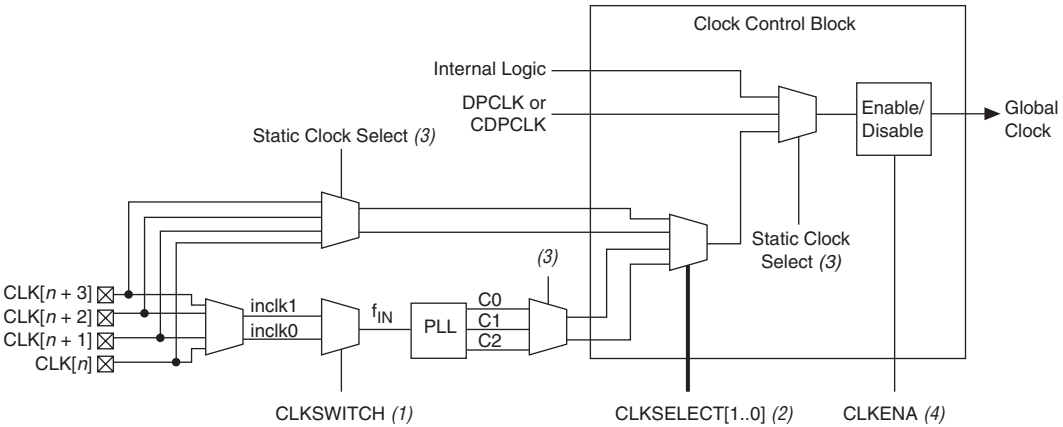
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	89
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5t144c7

Of the sources listed, only two clock pins, two PLL clock outputs, one DPCLK pin, and one internally-generated signal are chosen to drive into a clock control block. Figure 2–13 shows a more detailed diagram of the clock control block. Out of these six inputs, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of DPCLK and the signal from internal logic.

Figure 2–13. Clock Control Block



Notes to Figure 2–13:

(1) The CLKSWITCH signal can either be set through the configuration file or it can be dynamically set when using the manual PLL switchover feature. The output of the multiplexer is the input reference clock (f_{IN}) for the PLL.

(2) The CLKSELECT[1..0] signals are fed by internal logic and can be used to dynamically select the clock source for the global clock network when the device is in user mode.

(3) The static clock select signals are set in the configuration file and cannot be dynamically controlled when the device is in user mode.

(4) Internal logic can be used to enabled or disabled the global clock network in user mode.

Embedded Multiplier Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the embedded multiplier row interface interconnect. The embedded multipliers can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the embedded multiplier are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. Embedded multiplier outputs can also connect to left and right LABs through 18 direct link interconnects each. Figure 2–19 shows the embedded multiplier to logic array interface.

Figure 2–19. Embedded Multiplier LAB Row Interface

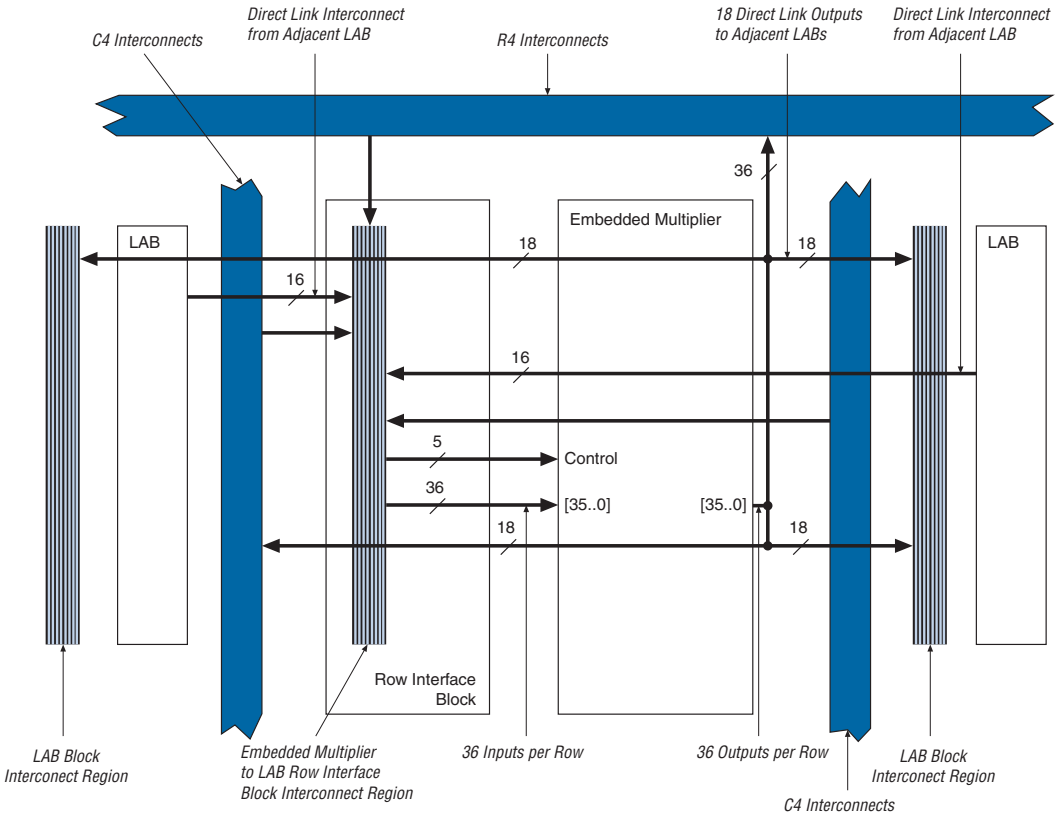


Table 5–15. Cyclone II Performance (Part 2 of 4)

Applications		Resources Used			Performance (MHz)			
		LEs	M4K Memory Blocks	DSP Blocks	–6 Speed Grade	–7 Speed Grade *(6)*	–7 Speed Grade *(7)*	–8 Speed Grade
Memory M4K block	Simple dual-port RAM 128 × 36 bit *(3)*, *(5)*	0	1	0	235.29	194.93	163.13	163.13
	True dual-port RAM 128 × 18 bit *(3)*, *(5)*	0	1	0	235.29	194.93	163.13	163.13
	FIFO 128 × 16 bit *(5)*	32	1	0	235.29	194.93	163.13	163.13
	Simple dual-port RAM 128 × 36 bit *(4)*,*(5)*	0	1	0	210.08	195.0	163.02	163.02
	True dual-port RAM 128x18 bit *(4)*,*(5)*	0	1	0	163.02	163.02	163.02	163.02
DSP block	9 × 9-bit multiplier *(2)*	0	0	1	260.01	216.73	180.57	180.57
	18 × 18-bit multiplier *(2)*	0	0	1	260.01	216.73	180.57	180.57
	18-bit, 4 tap FIR filter	113	0	8	182.74	147.47	127.74	122.98
Larger Designs	8-bit, 16 tap parallel FIR filter	52	0	4	153.56	131.25	110.44	110.57
	8-bit, 1024 pt, Streaming, 3 Mults/5 Adders FFT function	3191	22	9	235.07	195.0	147.51	163.02
	8-bit, 1024 pt, Streaming, 4 Mults/2 Adders FFT function	3041	22	12	235.07	195.0	146.3	163.02
	8-bit, 1024 pt, Single Output, 1 Parallel FFT Engine, Burst, 3 Mults/5 Adders FFT function	1056	5	3	235.07	195.0	147.84	163.02
	8-bit, 1024 pt, Single Output, 1 Parallel FFT Engine, Burst, 4 Mults/2 Adders FFT function	1006	5	4	235.07	195.0	149.99	163.02
	8-bit, 1024 pt, Single Output, 2 Parallel FFT Engines, Burst, 3 Mults/5 Adders FFT function	1857	10	6	200.0	195.0	149.61	163.02
	8-bit, 1024 pt, Single Output, 2 Parallel FFT Engines, Burst, 4 Mults/2 Adders FFT function	1757	10	8	200.0	195.0	149.34	163.02
	8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Burst, 3 Mults/5 Adders FFT function	2550	10	9	235.07	195.0	148.21	163.02

Table 5–44. Maximum Input Clock Toggle Rate on Cyclone II Devices (Part 2 of 2)

I/O Standard	Maximum Input Clock Toggle Rate on Cyclone II Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
DIFFERENTIAL_SSTL_18_CLASS_I	500	500	500	500	500	500	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_II	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
LVPECL	—	—	—	—	—	—	402	402	402
LVDS	402	402	402	402	402	402	402	402	402
1.2V_HSTL	110	90	80	—	—	—	110	90	80
1.2V_DIFFERENTIAL_HSTL	110	90	80	—	—	—	110	90	80

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 1 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVTTL	4 mA	120	100	80	120	100	80	120	100	80
	8 mA	200	170	140	200	170	140	200	170	140
	12 mA	280	230	190	280	230	190	280	230	190
	16 mA	290	240	200	290	240	200	290	240	200
	20 mA	330	280	230	330	280	230	330	280	230
	24 mA	360	300	250	360	300	250	360	300	250

Table 7–9. Clock Control Block Inputs (Part 2 of 2)

Input	Description
PLL outputs	The PLL counter outputs can drive the global clock network.
Internal logic	The global clock network can also be driven through the logic array routing to enable internal logic (LEs) to drive a high fan-out, low skew signal path.

In Cyclone II devices, the dedicated clock input pins, PLL counter outputs, dual-purpose clock I/O inputs, and internal logic can all feed the clock control block for each global clock network. The output from the clock control block in turn feeds the corresponding global clock network. The clock control blocks are arranged on the device periphery and there are a maximum of 16 clock control blocks available per Cyclone II device.

The control block has two functions:

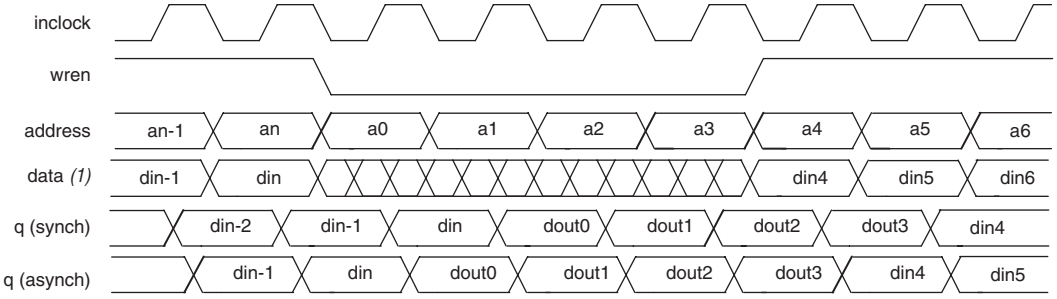
- Dynamic global clock network clock source selection
- Global clock network power-down (dynamic enable and disable)

Figure 7–11 shows the clock control block.

- 4K × 1
- 2K × 2
- 1K × 4
- 512 × 8
- 512 × 9
- 256 × 16
- 256 × 18
- 128 × 32
- 128 × 36

Figure 8–7 shows timing waveforms for read and write operations in single-port mode.

Figure 8–7. Cyclone II Single-Port Timing Waveforms

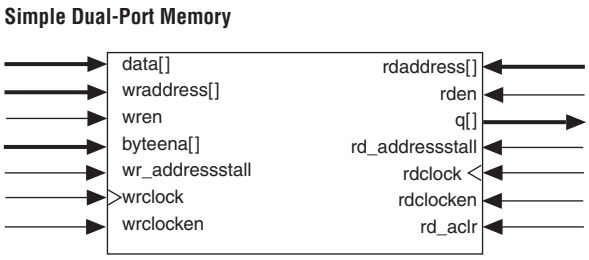


Note to Figure 8–7:
(1) The crosses in the `data` waveform during read mean "don't care."

Simple Dual-Port Mode

Simple dual-port mode supports simultaneous read and write operation. Figure 8–8 shows the simple dual-port memory configuration.

Figure 8–8. Cyclone II Simple Dual-Port Mode *Note (1)*



Note to Figure 8–8:
(1) Simple dual-port RAM supports input and output clock mode in addition to the read and write clock mode shown.

Cyclone II memory blocks support mixed-width configurations, allowing different read and write port widths. Tables 8–5 and 8–6 show the mixed-width configurations.

Table 8–5. Cyclone II Memory Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

In simple dual-port mode, the memory blocks have one write enable and one read enable signal. They do not support a clear port on the write enable and read enable registers. When the read enable is deactivated, the current data is retained at the output ports. If the read enable is activated during a write operation with the same address location selected, the simple dual-port RAM output is the old data stored at the memory

DQS pin to the DQ LE register does not necessarily match the delay from the DQ pin to the DQ LE register. Therefore, you must adjust the clock delay control circuitry to compensate for this difference in delays.

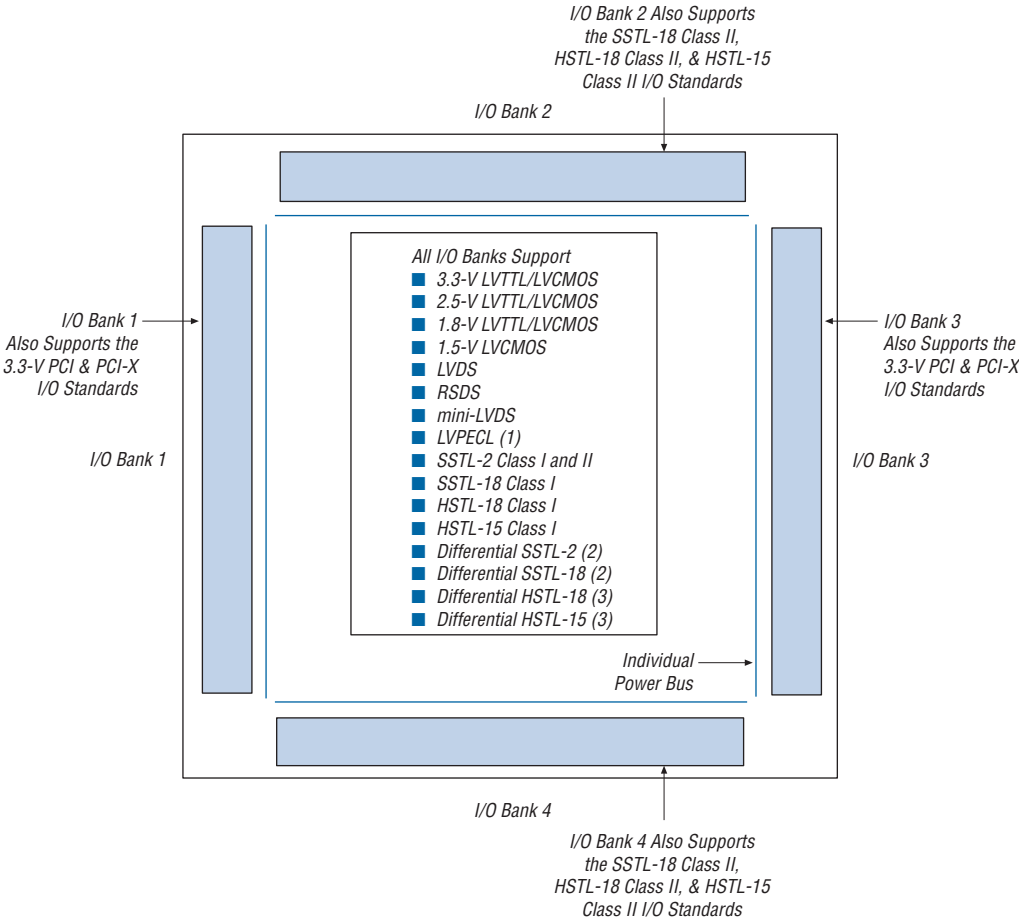
DQS Postamble

For external memory interfaces that use a bidirectional read strobe, such as DDR and DDR2 SDRAM, the DQS signal is low before going to or coming from the high-impedance state (see Figure 9–1). The state where DQS is low just after high-impedance is called the preamble and the state where DQS is low just before it goes to high-impedance is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR and DDR2 SDRAM. If the Cyclone II device or the DDR/DDR2 SDRAM device does not drive the DQ and DQS pins, the signals go to a high-impedance state. Because a pull-up resistor terminates both DQ and DQS to V_{TT} (1.25 V for SSTL-2 and 0.9 V for SSTL-18), the effective voltage on the high-impedance line is either 1.25 V or 0.9 V. According to the JEDEC JESD8-9 specification for SSTL-2 I/O standard and the JESD8-15A specification for SSTL-18 I/O standard, this is an indeterminate logic level, and the input buffer can interpret this as either a logic high or logic low. If there is any noise on the DQS line, the input buffer may interpret that noise as actual strobe edges.

Cyclone II devices have non-dedicated logic that can be configured to prevent a false edge trigger at the end of the DQS postamble. Each Cyclone II DQS signal is connected to postamble logic that consists of a D flip flop (see Figure 9–9). This register is clocked by the shifted DQS signal. Its input is connected to ground. The controller needs to include extra logic to tell the reset signal to release the preset signal on the falling DQS edge at the start of the postamble. This disables any glitches that happen right after the postamble. This postamble logic is automatically implemented by the Altera MegaCore DDR/DDR2 SDRAM Controller in the LE register as part of the open-source datapath.

pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. Cyclone II pin tables list the pins that support the high-speed I/O interface.

Figure 11–1. I/O Banks in EP2C5 & EP2C8 Devices



Notes to Figure 11–1:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(2) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(3) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

The number of embedded multipliers per column and the number of columns available increases with device density. Table 12–1 shows the number of embedded multipliers in each Cyclone II device and the multipliers that you can implement.

Table 12–1. Number of Embedded Multipliers in Cyclone II Devices

Device	Embedded Multipliers	9 × 9 Multipliers *(1)*	18 × 18 Multipliers *(1)*
EP2C5	13	26	13
EP2C8	18	36	18
EP2C20	26	52	26
EP2C35	35	70	35
EP2C50	86	172	86
EP2C70	150	300	150

Note to Table 12–1:
(1) Each device has either the number of 9 × 9 or 18 × 18 multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

In addition to the embedded multipliers, you can also implement soft multipliers using Cyclone II M4K memory blocks. The availability of soft multipliers increases the number of multipliers available within the device. Table 12–2 shows the total number of multipliers available in Cyclone II devices using embedded multipliers and soft multipliers.

Table 12–2. Number of Multipliers in Cyclone II Devices

Device	Embedded Multipliers (18 × 18)	Soft Multipliers (16 × 16) *(1)*	Total Multipliers *(2)*
EP2C5	13	26	39
EP2C8	18	36	54
EP2C20	26	52	78
EP2C35	35	105	140
EP2C50	86	129	215
EP2C70	150	250	400

Notes to Table 12–2:
(1) Soft multipliers are implemented in sum of multiplication mode. The M4K memory blocks are configured with 18-bit data widths to support 16-bit coefficients. The sum of the coefficients requires 18 bits of resolution to account for overflow.
(2) The total number of multipliers may vary according to the multiplier mode used.

13. Configuring Cyclone II Devices

CII51013-3.1

Introduction

Cyclone® II devices use SRAM cells to store configuration data. Since SRAM memory is volatile, configuration data must be downloaded to Cyclone II devices each time the device powers up. You can use the active serial (AS) configuration scheme, which can operate at a DCLK frequency up to 40 MHz, to configure Cyclone II devices. You can also use the passive serial (PS) and Joint Test Action Group (JTAG)-based configuration schemes to configure Cyclone II devices. Additionally, Cyclone II devices can receive a compressed configuration bitstream and decompress this data on-the-fly, reducing storage requirements and configuration time.

This chapter explains the Cyclone II configuration features and describes how to configure Cyclone II devices using the supported configuration schemes. This chapter also includes configuration pin descriptions and the Cyclone II configuration file format.

For more information on setting device configuration options or creating configuration files, see the *Software Settings* chapter in the *Configuration Handbook*.

Cyclone II Configuration Overview

You can use the AS, PS, and JTAG configuration schemes to configure Cyclone II devices. You can select which configuration scheme to use by driving the Cyclone II device MSEL pins either high or low as shown in Table 13–1. The MSEL pins are powered by the V_{CCIO} power supply of the bank they reside in. The MSEL[1..0] pins have 9-kΩ internal pull-down resistors that are always active. During power-on reset (POR) and reconfiguration, the MSEL pins have to be at LVTTL V_{IL} or V_{IH} levels to be considered a logic low or logic high, respectively. Therefore, to avoid any problems with detecting an incorrect configuration scheme, you should connect the MSEL[] pins to the V_{CCIO} of the I/O bank they reside in and GND without any pull-up or pull-down resistors. The MSEL[] pins should not be driven by a microprocessor or another device.

PS Configuration

You can use an Altera configuration device, a download cable, or an intelligent host, such as a MAX® II device or microprocessor to configure a Cyclone II device with the PS scheme. In the PS scheme, an external host (configuration device, MAX II device, embedded processor, or host PC) controls configuration. Configuration data is input to the target Cyclone II devices via the DATA0 pin at each rising edge of DCLK.

The Cyclone II decompression feature is fully available when configuring your Cyclone II device using PS mode.

Table 13–6 shows the MSEL pin settings when using the PS configuration scheme.

Table 13–6. Cyclone II MSEL Pin Settings for PS Configuration Schemes

Configuration Scheme	MSEL1	MSEL0
PS	0	1

Single Device PS Configuration Using a MAX II Device as an External Host

In the PS configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone II device. Configuration data can be stored in RBF, HEX, or TTF format. Figure 13–9 shows the configuration interface connections between the Cyclone II device and a MAX II device for single device configuration.

PS Configuration Using a Download Cable

In PS configuration, an intelligent host (e.g., a PC) can use a download cable to transfer data from a storage device to the Cyclone II device. You can use the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster™ serial/USB communications cable, ByteBlaster II parallel port download cable, or the ByteBlasterMV™ parallel port as a download cable.

Upon power up, the Cyclone II device goes through POR, which lasts approximately 100 ms for non "A" devices. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. Once the FPGA successfully exits POR, the nSTATUS pin is released and all user I/O pins continue to be tri-stated.

The value of the weak pull-up resistors on the I/O pins that are on before and during configuration can be found in the *Cyclone II Device Handbook*.

The configuration cycle consists of three stages: reset, configuration, and initialization. While the nCONFIG or nSTATUS pins are low, the device is in reset. To initiate configuration in this scheme, the download cable generates a low-to-high transition on the nCONFIG pin.

Make sure V_{CCINT} and V_{CCIO} for the banks where the configuration and JTAG pins reside are powered to the appropriate voltage levels in order to begin the configuration process.

When nCONFIG transitions high, the Cyclone II device comes out of reset and begins configuration. The Cyclone II device releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. Once nSTATUS transitions high, the Cyclone II device is ready to receive configuration data. The programming hardware or download cable then transmits the configuration data one bit at a time to the device's DATA0 pin. The configuration data is clocked into the target device until CONF_DONE goes high. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

When using a download cable, you cannot use the **Auto-restart configuration after error** option. You must manually restart configuration in the Quartus II software when an error occurs. Additionally, you cannot use the **Enable user-supplied start-up clock (CLKUSR)** option when programming the FPGA using the Quartus II programmer and download cable. This option is disabled in the SOF. Therefore, if you turn on the CLKUSR option, you do not need to provide a clock on CLKUSR when you are configuring the FPGA with the

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nCEO	N/A if option is on. I/O if option is off.	All	Output	This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration. If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. Use the Quartus II software to make this pin a user I/O pin.
ASDO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data. In AS mode, ASDO has an internal pull-up that is always active.
nCSO	N/A in AS mode I/O in PS and JTAG mode	AS	Output	This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.

Section VII. PCB Layout Guidelines

This section provides information for board layout designers to successfully layout their boards for Cyclone® II devices. The chapters in this section contain the required PCB layout guidelines and package specifications.

This section includes the following chapters:

- Chapter 15, Package Information for Cyclone II Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Tables 15–5 and 15–6 show the package information and package outline figure references, respectively, for the 144-pin TQFP package.

Table 15–5. 144-Pin TQFP Package Information

Description	Specification
Ordering code reference	T
Package acronym	TQFP
Lead frame material	Copper
Lead finish (plating)	Regular: 85Sn:15Pb (Typ.) Pb-free: Matte Sn
JEDEC Outline Reference	MS-026 Variation: BFB
Maximum lead coplanarity	0.003 inches (0.08mm)
Weight	1.3 g
Moisture sensitivity level	Printed on moisture barrier bag

Table 15–6. 144-Pin TQFP Package Outline Dimensions

Symbol	Millimeter		
	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
D	22.00 BSC		
D1	20.00 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	–	–
b	0.17	0.22	0.27
c	0.09	–	0.20
e	0.50 BSC		
θ	0°	3.5°	7°