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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	89
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5t144c7n

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between non-adjacent LABs, M4K memory blocks, dedicated multipliers, and row IOEs. R24 row interconnects drive to other row or column interconnects at every fourth LAB. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects and do not drive directly to LAB local interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

Column Interconnects

The column interconnect operates similar to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, M4K memory blocks, embedded multipliers, and row and column IOEs. These column resources include:

- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction
- C16 interconnects for high-speed vertical routing through the device

Cyclone II devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using register chain connections. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–9 shows the register chain interconnects.

Table 2–4 describes the PLL features in Cyclone II devices.

Table 2–4. Cyclone II PLL Features

Feature	Description
Clock multiplication and division	*m* / (*n* × post-scale counter) *m* and post-scale counter values (C0 to C2) range from 1 to 32. *n* ranges from 1 to 4.
Phase shift	Cyclone II PLLs have an advanced clock shift capability that enables programmable phase shifts in increments of at least 45°. The finest resolution of phase shifting is determined by the voltage control oscillator (VCO) period divided by 8 (for example, 1/1000 MHz/8 = down to 125-ps increments).
Programmable duty cycle	The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (C0-C2).
Number of internal clock outputs	The Cyclone II PLL has three outputs which can drive the global clock network. One of these outputs (C2) can also drive a dedicated PLL<#>_OUT pin (single ended or differential).
Number of external clock outputs	The C2 output drives a dedicated PLL<#>_OUT pin. If the C2 output is not used to drive an external clock output, it can be used to drive the internal global clock network. The C2 output can concurrently drive the external clock output and internal global clock network.
Manual clock switchover	The Cyclone II PLLs support manual switchover of the reference clock through internal logic. This enables you to switch between two reference input clocks during user mode for applications that may require clock redundancy or support for clocks with two different frequencies.
Gated lock signal	The lock output indicates that there is a stable clock output signal in phase with the reference clock. Cyclone II PLLs include a programmable counter that holds the lock signal low for a user-selected number of input clock transitions, allowing the PLL to lock before enabling the locked signal. Either a gated locked signal or an ungated locked signal from the locked port can drive internal logic or an output pin.
Clock feedback modes	In zero delay buffer mode, the external clock output pin is phase-aligned with the clock input pin for zero delay. In normal mode, the PLL compensates for the internal global clock network delay from the input clock pin to the clock port of the IOE output registers or registers in the logic array. In no compensation mode, the PLL does not compensate for any clock networks.
Control signals	The pllenable signal enables and disables the PLLs. The areset signal resets/resynchronizes the inputs for each PLL. The pfdena signal controls the phase frequency detector (PFD) output with a programmable gate.

Programmable delays can increase the register-to-pin delays for output registers. Table 2–13 shows the programmable delays for Cyclone II devices.

Table 2–13. Cyclone II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to internal LE registers that reside in two different areas of the device. You set the two combinational input delays by selecting different delays for two different paths under the **Input delay from pin to internal cells logic** option in the Quartus II software. However, if the pin uses the input register, one of delays is disregarded because the IOE only has two paths to internal logic. If the input register is used, the IOE uses one input path. The other input path is then available for the combinational path, and only one input delay assignment is applied.

The IOE registers in each I/O block share the same source for clear or preset. You can program preset or clear for each individual IOE, but both features cannot be used simultaneously. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available for the IOE registers.

External Memory Interfacing

Cyclone II devices support a broad range of external memory interfaces such as SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature dedicated high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The programmable DQS delay chain allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Table 2–17. Cyclone II Supported I/O Standards & Constraints (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level		Top & Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
Differential HSTL-15 class I or class II	Pseudo differential *(4)*	*(5)*	1.5 V				✓ *(7)*	
		1.5 V	*(5)*	✓ *(6)*		✓ *(6)*		
Differential HSTL-18 class I or class II	Pseudo differential *(4)*	*(5)*	1.8 V				✓ *(7)*	
		1.8 V	*(5)*	✓ *(6)*		✓ *(6)*		
LVDS	Differential	2.5 V	2.5 V	✓	✓	✓	✓	✓
RSDS and mini-LVDS *(8)*	Differential	*(5)*	2.5 V		✓		✓	✓
LVPECL *(9)*	Differential	3.3 V/ 2.5 V/ 1.8 V/ 1.5 V	*(5)*	✓		✓		

Notes to Table 2–17:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.
(2) These pins support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.
(3) PCI-X does not meet the IV curve requirement at the linear region. PCI-clamp diode is not available on top and bottom I/O pins.
(4) Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Pseudo-differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them.
(5) This I/O standard is not supported on these I/O pins.
(6) This I/O standard is only supported on the dedicated clock pins.
(7) `PLL_OUT` does not support differential SSTL-18 class II and differential 1.8 and 1.5-V HSTL class II.
(8) mini-LVDS and RSDS are only supported on output pins.
(9) LVPECL is only supported on clock inputs.

For more information on Cyclone II supported I/O standards, see the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

High-Speed Differential Interfaces

Cyclone II devices can transmit and receive data through LVDS signals at a data rate of up to 640 Mbps and 805 Mbps, respectively. For the LVDS transmitter and receiver, the Cyclone II device's input and output pins support serialization and deserialization through internal logic.

I/O Banks

The I/O pins on Cyclone II devices are grouped together into I/O banks and each bank has a separate power bus. EP2C5 and EP2C8 devices have four I/O banks (see Figure 2–28), while EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices have eight I/O banks (see Figure 2–29). Each device I/O pin is associated with one I/O bank. To accommodate voltage-referenced I/O standards, each Cyclone II I/O bank has a VREF bus. Each bank in EP2C5, EP2C8, EP2C15, EP2C20, EP2C35, and EP2C50 devices supports two VREF pins and each bank of EP2C70 supports four VREF pins. When using the VREF pins, each VREF pin must be properly connected to the appropriate voltage level. In the event these pins are not used as VREF pins, they may be used as regular I/O pins.

The top and bottom I/O banks (banks 2 and 4 in EP2C5 and EP2C8 devices and banks 3, 4, 7, and 8 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support all I/O standards listed in Table 2–17, except the PCI/PCI-X I/O standards. The left and right side I/O banks (banks 1 and 3 in EP2C5 and EP2C8 devices and banks 1, 2, 5, and 6 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support I/O standards listed in Table 2–17, except SSTL-18 class II, HSTL-18 class II, and HSTL-15 class II I/O standards. See Table 2–17 for a complete list of supported I/O standards.

The top and bottom I/O banks (banks 2 and 4 in EP2C5 and EP2C8 devices and banks 3, 4, 7, and 8 in EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) support DDR2 memory up to 167 MHz/333 Mbps and QDR memory up to 167 MHz/668 Mbps. The left and right side I/O banks (1 and 3 of EP2C5 and EP2C8 devices and 1, 2, 5, and 6 of EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices) only support SDR and DDR SDRAM interfaces. All the I/O banks of the Cyclone II devices support SDR memory up to 167 MHz/167 Mbps and DDR memory up to 167 MHz/333 Mbps.

DDR2 and QDRII interfaces may be implemented in Cyclone II side banks if the use of class I I/O standard is acceptable.

standards (e.g., SSTL-2) independently. If an I/O bank does not use voltage-referenced standards, the VREF pins are available as user I/O pins.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3-V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs. Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards as long as they use the same V_{REF} and a compatible V_{CCIO} value.

MultiVolt I/O Interface

The Cyclone II architecture supports the MultiVolt I/O interface feature, which allows Cyclone II devices in all packages to interface with systems of different supply voltages. Cyclone II devices have one set of V_{CC} pins (VCCINT) that power the internal device logic array and input buffers that use the LVPECL, LVDS, HSTL, or SSTL I/O standards. Cyclone II devices also have four or eight sets of VCC pins (VCCIO) that power the I/O output drivers and input buffers that use the LVTTL, LVCMOS, or PCI I/O standards.

The Cyclone II VCCINT pins must always be connected to a 1.2-V power supply. If the V_{CCINT} level is 1.2 V, then input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3-V and is compatible with 3.3-V systems. Table 2–20 summarizes Cyclone II MultiVolt I/O support.

Table 2–20. Cyclone II MultiVolt I/O Support (Part 1 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
1.5	✓	✓	✓ *(2)*	✓ *(2)*	✓			
1.8	✓ *(4)*	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓		
2.5			✓	✓	✓ *(5)*	✓ *(5)*	✓	

Table 2–20. Cyclone II MultiVolt I/O Support (Part 2 of 2) *Note (1)*

V_{CCIO} (V)	Input Signal				Output Signal			
	1.5 V	1.8 V	2.5 V	3.3 V	1.5 V	1.8 V	2.5 V	3.3 V
3.3			✓ *(4)*	✓	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓

Notes to Table 2–20:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value. To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on **Allow voltage overdrive for LVTTL/LVCMOS input pins** option in Device setting option in the Quartus II software.

(3) When V_{CCIO} = 1.8-V, a Cyclone II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(4) When V_{CCIO} = 3.3-V and a 2.5-V input signal feeds an input pin or when V_{CCIO} = 1.8-V and a 1.5-V input signal feeds an input pin, the V_{CCIO} supply current will be slightly larger than expected. The reason for this increase is that the input signal level does not drive to the V_{CCIO} rail, which causes the input buffer to not completely shut off.

(5) When V_{CCIO} = 2.5-V, a Cyclone II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(6) When V_{CCIO} = 3.3-V, a Cyclone II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

5. DC Characteristics and Timing Specifications

CII51005-4.0

Operating Conditions

Cyclone® II devices are offered in commercial, industrial, automotive, and extended temperature grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the parameter values in this chapter apply to all Cyclone II devices. AC and DC characteristics are specified using the same numbers for commercial, industrial, and automotive grades. All parameters representing voltages are measured with respect to ground.

Tables 5–1 through 5–4 provide information on absolute maximum ratings.

Table 5–1. Cyclone II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Output supply voltage		–0.5	4.6	V
V_{CCA_PLL} [1..4]	PLL supply voltage		–0.5	1.8	V
V_{IN}	DC input voltage *(3)*	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	—	125	°C

Notes to Table 5–1:

(1) Conditions beyond those listed in this table cause permanent damage to a device. These are stress ratings only. Functional operation at these levels or any other conditions beyond those specified in this chapter is not implied. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effect on the device reliability.

(2) Refer to the *Operating Requirements for Altera Devices Data Sheet* for more information.

(3) During transitions, the inputs may overshoot to the voltage shown in Table 5–4 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transition, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5–7. DC Characteristics of User I/O Pins Using Single-Ended Standards Notes (1), (2) **(Part 2 of 2)**

I/O Standard	Test Conditions		Voltage Thresholds	
	I_{OL} (mA)	I_{OH} (mA)	Maximum V_{OL} (V)	Minimum V_{OH} (V)
1.5-V HSTL class I	8	–8	0.4	V_{CCIO} – 0.4
1.5V HSTL class II	16	–16	0.4	V_{CCIO} – 0.4

Notes to Table 5–7:

(1) The values in this table are based on the conditions listed in Tables 5–2 and 5–6.

(2) This specification is supported across all the programmable drive settings available as shown in the *Cyclone II Architecture* chapter of the *Cyclone II Device Handbook*.

Differential I/O Standards

The RSDS and mini-LVDS I/O standards are only supported on output pins. The LVDS I/O standard is supported on both receiver input pins and transmitter output pins.

For more information on how these differential I/O standards are implemented, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the *Cyclone II Device Handbook*.

Figure 5–1 shows the receiver input waveforms for all differential I/O standards (LVDS, LVPECL, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 3 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
SSTL_2_ CLASS_I	8 mA	t_{OP}	1196	1254	2388	2516	2638	2645	ps
		t_{DIP}	1328	1393	2558	2710	2864	2864	ps
	12 mA (1)	t_{OP}	1174	1231	2277	2401	2518	2525	ps
		t_{DIP}	1306	1370	2447	2595	2744	2744	ps
SSTL_2_ CLASS_II	16 mA	t_{OP}	1158	1214	2245	2365	2479	2486	ps
		t_{DIP}	1290	1353	2415	2559	2705	2705	ps
	20 mA	t_{OP}	1152	1208	2231	2351	2464	2471	ps
		t_{DIP}	1284	1347	2401	2545	2690	2690	ps
	24 mA (1)	t_{OP}	1152	1208	2225	2345	2458	2465	ps
		t_{DIP}	1284	1347	2395	2539	2684	2684	ps
SSTL_18_ CLASS_I	6 mA	t_{OP}	1472	1544	3140	3345	3542	3549	ps
		t_{DIP}	1604	1683	3310	3539	3768	3768	ps
	8 mA	t_{OP}	1469	1541	3086	3287	3482	3489	ps
		t_{DIP}	1601	1680	3256	3481	3708	3708	ps
	10 mA	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
	12 mA (1)	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
SSTL_18_ CLASS_II	16 mA	t_{OP}	1454	1525	2905	3088	3263	3270	ps
		t_{DIP}	1586	1664	3075	3282	3489	3489	ps
	18 mA (1)	t_{OP}	1453	1524	2900	3082	3257	3264	ps
		t_{DIP}	1585	1663	3070	3276	3483	3483	ps
1.8V_HSTL_ CLASS_I	8 mA	t_{OP}	1460	1531	3222	3424	3618	3625	ps
		t_{DIP}	1592	1670	3392	3618	3844	3844	ps
	10 mA	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
	12 mA (1)	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps

clock sources and the clkena signals for the global clock network multiplexers can be set through the Quartus II software using the altclkctrl megafunction.

clkena signals

In Cyclone II devices, the clkena signals are supported at the clock network level. Figure 7–14 shows how the clkena is implemented. This allows you to gate off the clock even when a PLL is not being used. Upon re-enabling the output clock, the PLL does not need a resynchronization or relock period because the clock is gated off at the clock network level. Also, the PLL can remain locked independent of the clkena signals since the loop-related counters are not affected.

Figure 7–14. clkena Implementation

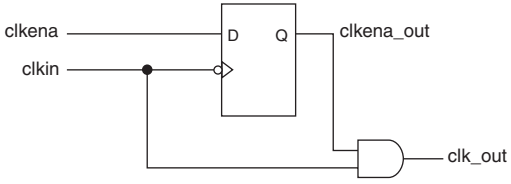


Figure 7–15 shows the waveform example for a clock output enable. clkena is synchronous to the falling edge of the clock (clkin).

This feature is useful for applications that require a low power or sleep mode. The exact amount of power saved when using this feature is pending device characterization.

Section III. Memory

This section provides information on embedded memory blocks in Cyclone® II devices and the supported external memory interfaces.

This section includes the following chapters:

- Chapter 8, Cyclone II Memory Blocks
- Chapter 9, External Memory Interfaces

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

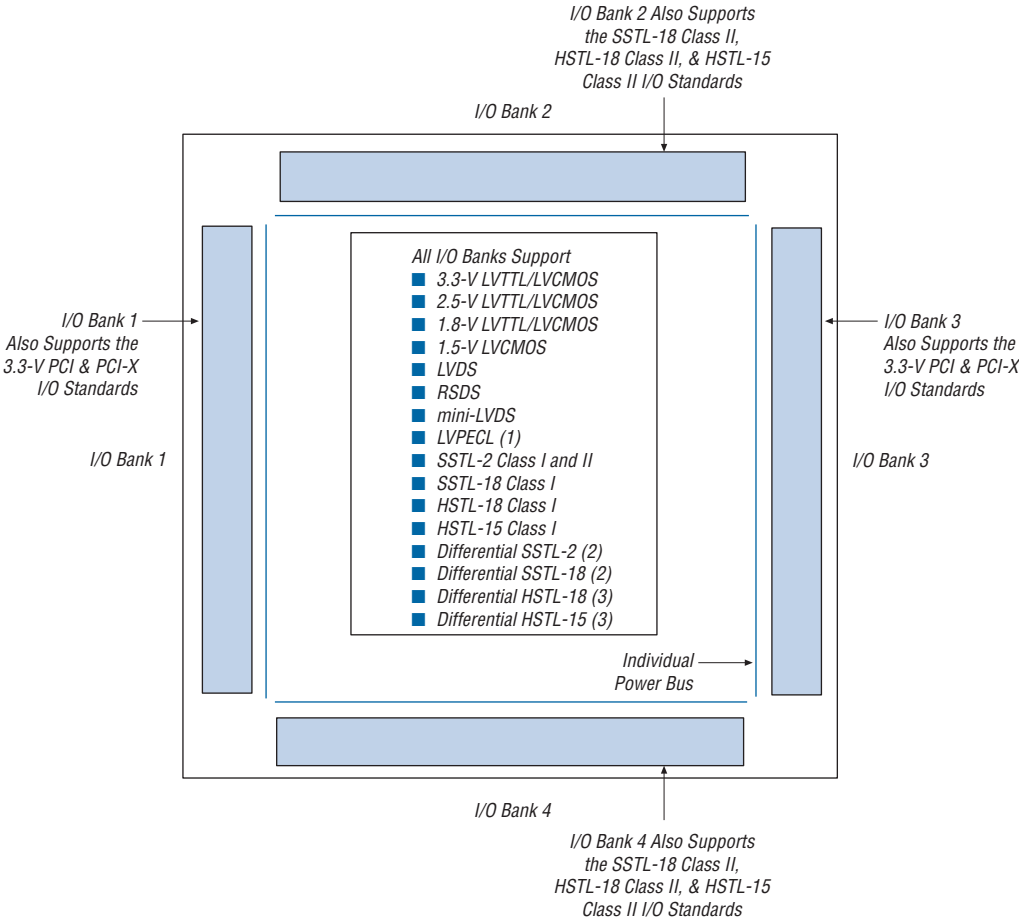
For information about the I/O standards supported for external memory applications, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(1)*	*(1)*	*(1)*
PCI and PCI-X *(2)*	Single ended	3.3 V	3.3 V	—	—	✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(3)*	*(4)*	2.5 V	—	—	—	✓	—
		2.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential SSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—		✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—

pins in each I/O bank (on both rows and columns) support the high-speed I/O interface. Cyclone II pin tables list the pins that support the high-speed I/O interface.

Figure 11–1. I/O Banks in EP2C5 & EP2C8 Devices



Notes to Figure 11–1:

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(2) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(3) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

You must connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. You should buffer the DCLK and DATA lines for every fourth device. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

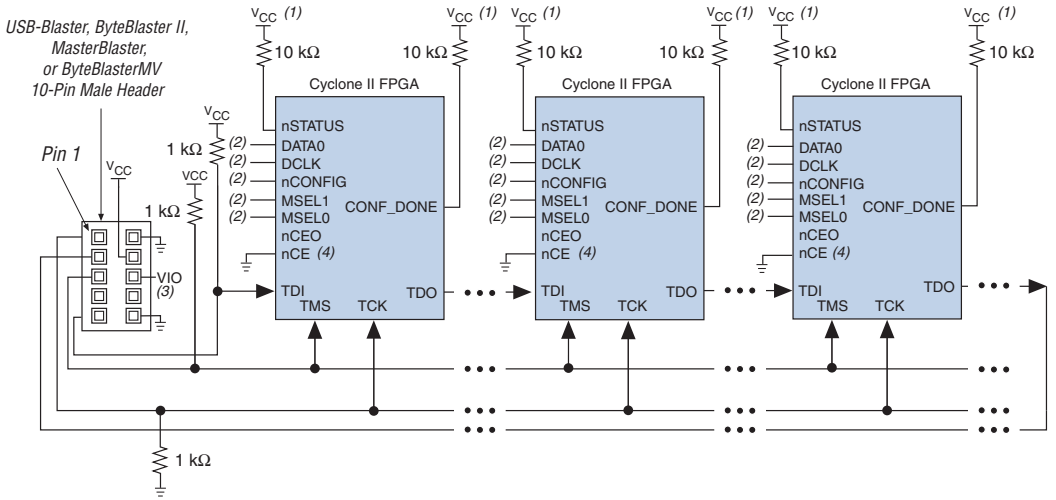
Since all nSTATUS and CONF_DONE pins are connected, if any Cyclone II device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first Cyclone II detects an error, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single Cyclone II device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the Cyclone II devices release their nSTATUS pins after a reset time-out period (maximum of 40 µs). After all nSTATUS pins are released and pulled high, the MAX II device reconfigures the chain without pulsing nCONFIG low. If the **Auto-restart configuration after error** option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

If you want to delay the initialization of the devices in the chain, you can use the CLKUSR pin option. The CLKUSR pin allows you to control when your device enters user mode. This feature also allows you to control the order of when each device enters user mode by feeding a separate clock to each device's CLKUSR pin. By using the CLKUSR pins, you can choose any device in the multiple device chain to enter user mode first and have the other devices enter user mode at a later time.

Different device families may require a different number of initialization clock cycles. Therefore, if your multiple device chain consists of devices from different families, the devices may enter user mode at a slightly different time due to the different number of initialization clock cycles required. However, if the number of initialization clock cycles is similar across different device families or if the devices are from the same family, then the devices enter user mode at the same time. See the respective device family handbook for more information about the number of initialization clock cycles required.

Figure 13–24. JTAG Configuration of Multiple Devices Using a Download Cable



Notes to Figure 13–24:

(1) The pull-up resistor should be connected to the same supply voltage as the USB-Blaster, MasterBlaster (VIO pin), ByteBlaster II or ByteBlasterMV cable.

(2) Connect the nCONFIG and MSEL[1..0] pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the nCONFIG pin to V_{CC}, and the MSEL[1..0] pins to ground. In addition, pull DCLK and DATA0 to either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cable, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.

(4) nCE must be connected to ground or driven low for successful JTAG configuration.

Connect the nCE pin to GND or pull it low during JTAG configuration. In multiple device AS and PS configuration chains, connect the first device's nCE pin to GND and connect its nCEO pin to the nCE pin of the next device in the chain or you can use it as a user I/O pin after configuration.

After the first device completes configuration in a multiple device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, you should make sure the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multiple device configuration chain, the nCEO pin of the previous device drives the nCE pin of the next device low when it has successfully been JTAG configured.

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Document Revision History

Table 14–4 shows the revision history for this document.

Table 14–4. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.1	• Added document revision history. • Added new section "BST for Configured Devices".	• Added infomation about 'Always Enable Input Buffer' option.
July 2005 v2.0	Moved the "JTAG Timing Specifications" section to the *DC Characteristics & Timing Specifications* chapter.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

15. Package Information for Cyclone II Devices

CII51015-2.3

Introduction

This chapter provides package information for Altera® Cyclone® II devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Table 15–1 shows Cyclone II device package options.

Table 15–1. Cyclone II Device Package Options

Device	Package	Pins
EP2C5	Plastic Thin Quad Flat Pack (TQFP) – Wirebond	144
	Plastic Quad Flat Pack (PQFP) – Wirebond	208
	Low profile FineLine BGA® – Wirebond	256
EP2C8	TQFP – Wirebond	144
	PQFP – Wirebond	208
	Low profile FineLine BGA – Wirebond	256
EP2C15	Low profile FineLine BGA, Option 2 – Wirebond	256
	FineLine BGA, Option 3– Wirebond	484
EP2C20	PQFP – Wirebond	240
	Low profile FineLine BGA, Option 2 – Wirebond	256
	FineLine BGA, Option 3– Wirebond	484
EP2C35	FineLine BGA, Option 3 – Wirebond	484
	Ultra FineLine BGA – Wirebond	484
	FineLine BGA, Option 3 – Wirebond	672
EP2C50	FineLine BGA, Option 3 – Wirebond	484
	Ultra FineLine BGA – Wirebond	484
	FineLine BGA, Option 3 – Wirebond	672
EP2C70	FineLine BGA, Option 3 – Wirebond	672
	FineLine BGA – Wirebond	896

Document Revision History

Table 15–21 shows the revision history for this document.

Table 15–21. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.3	Added document revision history.	
November 2005 v2.1	Updated information throughout.	
July 2005 v2.0	Updated packaging information.	
November 2004 v1.0	Added document to the Cyclone II Device Handbook.	