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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

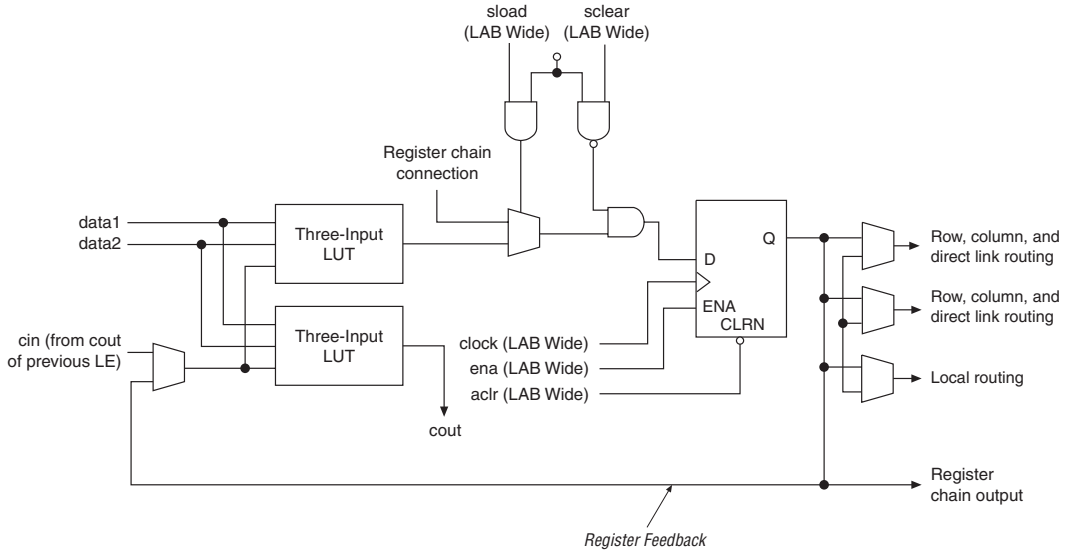
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	288
Number of Logic Elements/Cells	4608
Total RAM Bits	119808
Number of I/O	89
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c5t144i8

Contents

Figure 2–4. LE in Arithmetic Mode

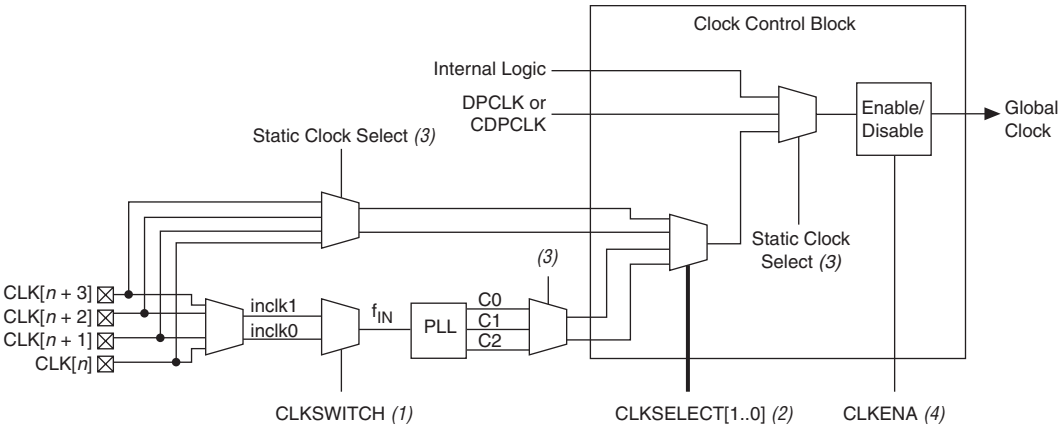


The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 LEs by automatically linking LABs in the same column. For enhanced fitting, a long carry chain runs vertically, which allows fast horizontal connections to M4K memory blocks or embedded multipliers through direct link interconnects. For example, if a design has a long carry chain in a LAB column next to a column of M4K memory blocks, any LE output can feed an adjacent M4K memory block through the direct link interconnect. Whereas if the carry chains ran horizontally, any LAB not next to the column of M4K memory blocks would use other row or column interconnects to drive a M4K memory block. A carry chain continues as far as a full column.

Of the sources listed, only two clock pins, two PLL clock outputs, one DPCLK pin, and one internally-generated signal are chosen to drive into a clock control block. Figure 2–13 shows a more detailed diagram of the clock control block. Out of these six inputs, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of DPCLK and the signal from internal logic.

Figure 2–13. Clock Control Block



Notes to Figure 2–13:

(1) The CLKSWITCH signal can either be set through the configuration file or it can be dynamically set when using the manual PLL switchover feature. The output of the multiplexer is the input reference clock (f_{IN}) for the PLL.

(2) The CLKSELECT[1..0] signals are fed by internal logic and can be used to dynamically select the clock source for the global clock network when the device is in user mode.

(3) The static clock select signals are set in the configuration file and cannot be dynamically controlled when the device is in user mode.

(4) Internal logic can be used to enabled or disabled the global clock network in user mode.

Table 2–18. Cyclone II Device LVDS Channels (Part 2 of 2)		
Device	**Pin Count**	**Number of LVDS Channels** *(1)*
EP2C70	672	160 (168)
	896	257 (265)

Note to Table 2–18:
(1) The first number represents the number of bidirectional I/O pins which can be used as inputs or outputs. The number in parenthesis includes dedicated clock input pin pairs which can only be used as inputs.

You can use I/O pins and internal logic to implement a high-speed I/O receiver and transmitter in Cyclone II devices. Cyclone II devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal PLLs, and IOEs are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

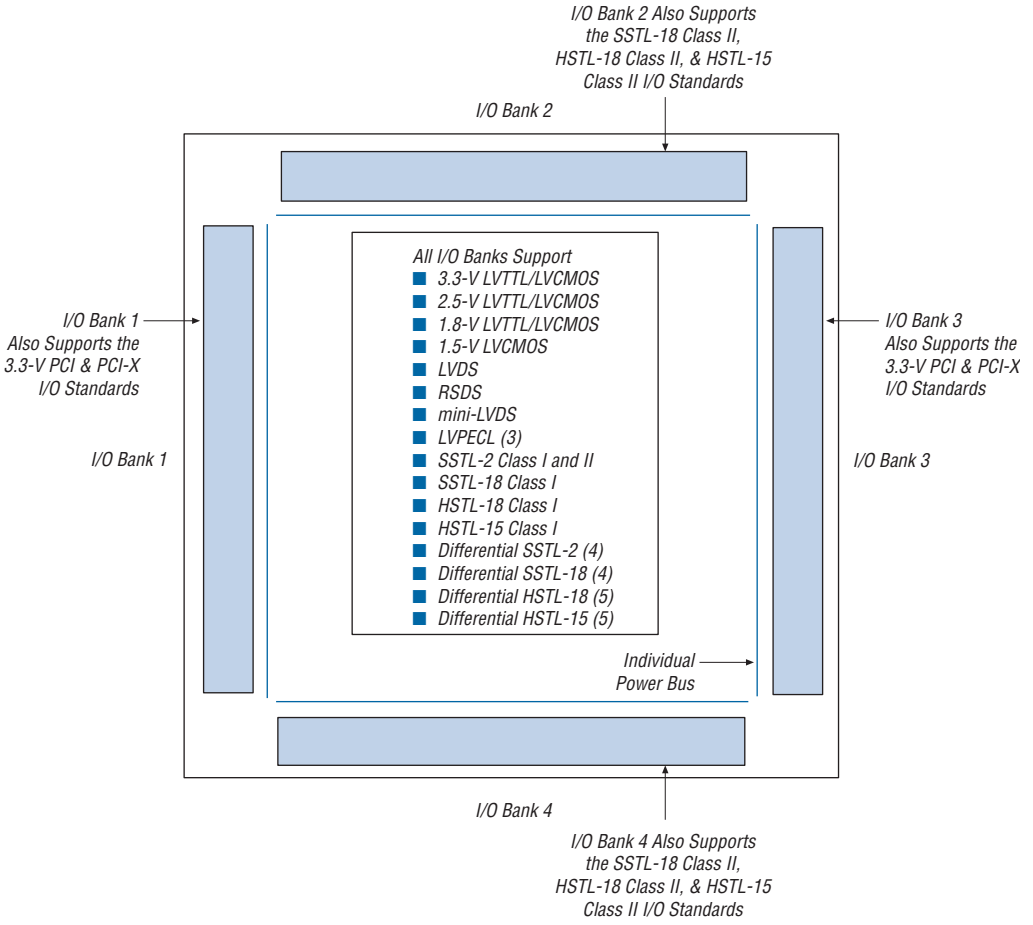
The maximum internal clock frequency for a receiver and for a transmitter is 402.5 MHz. The maximum input data rate of 805 Mbps and the maximum output data rate of 640 Mbps is only achieved when DDIO registers are used. The LVDS standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side.

For more information on Cyclone II differential I/O interfaces, see the *High-Speed Differential Interfaces in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Series On-Chip Termination

On-chip termination helps to prevent reflections and maintain signal integrity. This also minimizes the need for external resistors in high pin count ball grid array (BGA) packages. Cyclone II devices provide I/O driver on-chip impedance matching and on-chip series termination for single-ended outputs and bidirectional pins.

Figure 2–28. EP2C5 & EP2C8 I/O Banks *Notes (1), (2)*



Notes to Figure 2–28:

(1) This is a top view of the silicon die.
(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.
(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
(4) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.
(5) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

Altera has ensured by design of the I/O buffers and hot-socketing circuitry, that Cyclone II devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone II Devices

The hot-socketing feature turns off the output buffer during power up (either V_{CCINT} or V_{CCIO} supplies) or power down. The hot-socket circuit generates an internal HOTSCKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. Designs cannot use the HOTSCKT signal for other purposes. The HOTSCKT signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When V_{CC} ramps up slowly, V_{CC} is still relatively low even after the internal POR signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tristated at this low V_{CC} voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are able to operate during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 4–1.

Table 5–23. EP2C8/A Column Pins Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
$t_{PLLCOUT}$	–0.179	–0.189	0.089	0.047	0.045	0.055	ns

Notes to Table 5–23:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–24. EP2C8/A Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.256	1.314	2.270	2.416	2.596	2.606	ns
t_{COUT}	1.258	1.316	2.286	2.429	2.604	2.614	ns
t_{PLLCIN}	–0.276	–0.294	–0.08	–0.134	–0.152	–0.142	ns
$t_{PLLCOUT}$	–0.274	–0.292	–0.064	–0.121	–0.144	–0.134	ns

Notes to Table 5–24:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

EP2C15A Clock Timing Parameters

Tables 5–25 and 5–26 show the clock timing parameters for EP2C15A devices.

Table 5–25. EP2C15A Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.621	1.698	2.590	2.766	3.009	2.989	ns
t_{COUT}	1.635	1.713	2.624	2.798	3.038	3.018	ns
t_{PLLCIN}	–0.351	–0.372	0.045	0.008	0.046	0.016	ns

Table 5–38. Default Loading of Different I/O Standards for Cyclone II Device (Part 2 of 2)

I/O Standard	Capacitive Load	Unit
SSTL_18_CLASS_II	0	pF
1.5V_HSTL_CLASS_I	0	pF
1.5V_HSTL_CLASS_II	0	pF
1.8V_HSTL_CLASS_I	0	pF
1.8V_HSTL_CLASS_II	0	pF
DIFFERENTIAL_SSTL_2_CLASS_I	0	pF
DIFFERENTIAL_SSTL_2_CLASS_II	0	pF
DIFFERENTIAL_SSTL_18_CLASS_I	0	pF
DIFFERENTIAL_SSTL_18_CLASS_II	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.5V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_I	0	pF
1.8V_DIFFERENTIAL_HSTL_CLASS_II	0	pF
LVDS	0	pF
1.2V_HSTL	0	pF
1.2V_DIFFERENTIAL_HSTL	0	pF

Table 5–48. RSDS Transmitter Timing Specification (Part 2 of 2)

Symbol	Conditions	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max *(1)*	Min	Typ	Max *(1)*	Min	Typ	Max *(1)*	
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	500	ps
t_{RISE}	20–80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	80–20%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	—	—		100	—		100	—	—	100	µs

Note to Table 5–48:

(1) These specifications are for a three-resistor RSDS implementation. For single-resistor RSDS in ×10 through ×2 modes, the maximum data rate is 170 Mbps and the corresponding maximum input clock frequency is 85 MHz. For single-resistor RSDS in ×1 mode, the maximum data rate is 170 Mbps, and the maximum input clock frequency is 170 MHz. For more information about the different RSDS implementations, refer to the *High-Speed Differential Interfaces in Cyclone II Devices* chapter of the Cyclone II Device Handbook.

In order to determine the transmitter timing requirements, RSDS receiver timing requirements on the other end of the link must be taken into consideration. RSDS receiver timing parameters are typically defined as t_{SU} and t_H requirements. Therefore, the transmitter timing parameter specifications are t_{CO} (minimum) and t_{CO} (maximum). Refer to Figure 5–4 for the timing budget.

The AC timing requirements for RSDS are shown in Figure 5–5.

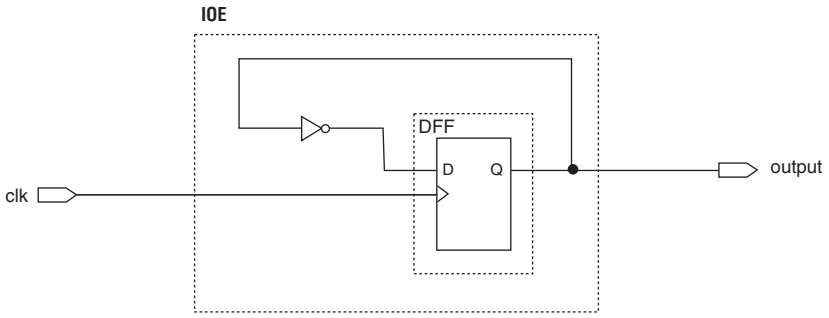
(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

DCD Measurement Techniques

DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 5–9). Therefore, any DCD present on the input clock signal, or caused by the clock input buffer, or different input I/O standard, does not transfer to the output signal.

Figure 5–9. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs

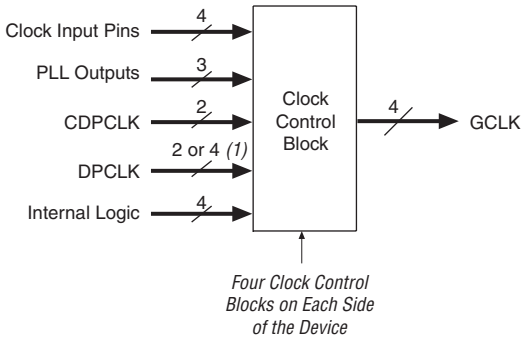


However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 5–10). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

From the clock sources listed above, only two clock input pins, two PLL clock outputs, one DPCLK or CDPCLK pin, and one source from internal logic can drive into any given clock control blocks, as shown in Figure 7–11. Out of these six inputs to any clock control block, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of the DPCLK or CDPCLK pin and the signal from internal logic.

Figure 7–13 shows the simplified version of the four clock control blocks on each side of the Cyclone II device periphery. The Cyclone II devices support up to 16 of these clock control blocks and this allows for up to a maximum of 16 global clocks in Cyclone II devices.

Figure 7–13. Clock Control Blocks on Each Side of the Cyclone II Device



Note to Figure 7–13:
(1) The left and right sides of the device have two DPCLK pins, and the top and bottom of the device have four DPCLK pins.

Global Clock Network Power Down

The Cyclone II global clock network can be disabled (powered down) by both static and dynamic approaches. When a clock network is powered down, all the logic fed by the clock network is in an off-state, thereby reducing the overall power consumption of the device.

The global clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable or disable feature allows internal logic to synchronously control power up or down on the global clock networks in the Cyclone II device. This function is independent of the PLL and is applied directly on the clock network, as shown in Figure 7–11. The input

VCCA & GNDA

Each Cyclone II PLL uses separate VCC and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called VCCA_PLL<*PLL number*> and GNDA_ PLL<*PLL number*>. Connect the VCCA power pin to a 1.2-V power supply, even if you do not use the PLL. Isolate the power connected to VCCA from the power to the rest of the Cyclone II device or any other digital device on the board. You can use one of three different methods of isolating the VCCA pin:

- Use separate VCCA power planes
- Use a partitioned VCCA island within the VCCINT plane
- Use thick VCCA traces

Separate VCCA Power Plane

A mixed signal system is already partitioned into analog and digital sections, each with its own power planes on the board. To isolate the VCCA pin using a separate VCCA power plane, connect the VCCA pin to the analog 1.2-V power plane.

Partitioned VCCA Island Within the VCCINT Plane

Fully digital systems do not have a separate analog power plane on the board. Since it is expensive to add new planes to the board, you can create islands for VCCA_PLL. Figure 7–16 shows an example board layout with an analog power island. The dielectric boundary that creates the island should be 25 mils thick. Figure 7–16 shows a partitioned plane within V_{CCINT} for VCCA.

case writing is controlled only by the write enable signals. There is no clear port to the byte enable registers. M4K blocks support byte enables when the write port has a data width of 1, 2, 4, 8, 9, 16, 18, 32, or 36 bits. When using data widths of 1, 2, 4, 8, and 9 bits, the byte enable behaves as a redundant write enable because the data width is less than or equal to a single byte. Table 8–3 summarizes the byte selection.

Table 8–3. Byte Enable for Cyclone II M4K Blocks *Note (1)*

byteena[3..0]	Affected Bytes								
	datain ×1	datain ×2	datain ×4	datain ×8	datain ×9	datain ×16	datain ×18	datain ×32	datain ×36
[0] = 1	[0]	[1..0]	[3..0]	[7..0]	[8..0]	[7..0]	[8..0]	[7..0]	[8..0]
[1] = 1	-	-	-	-	-	[15..8]	[17..9]	[15..8]	[17..9]
[2] = 1	-	-	-	-	-	-	-	[23..16]	[26..18]
[3] = 1	-	-	-	-	-	-	-	[31..24]	[35..27]

Note to Table 8–3:
(1) Any combination of byte enables is possible.

Table 8–4 shows the byte enable port control for true dual-port mode.

Table 8–4. Byte Enable Port Control for True Dual-Port Mode

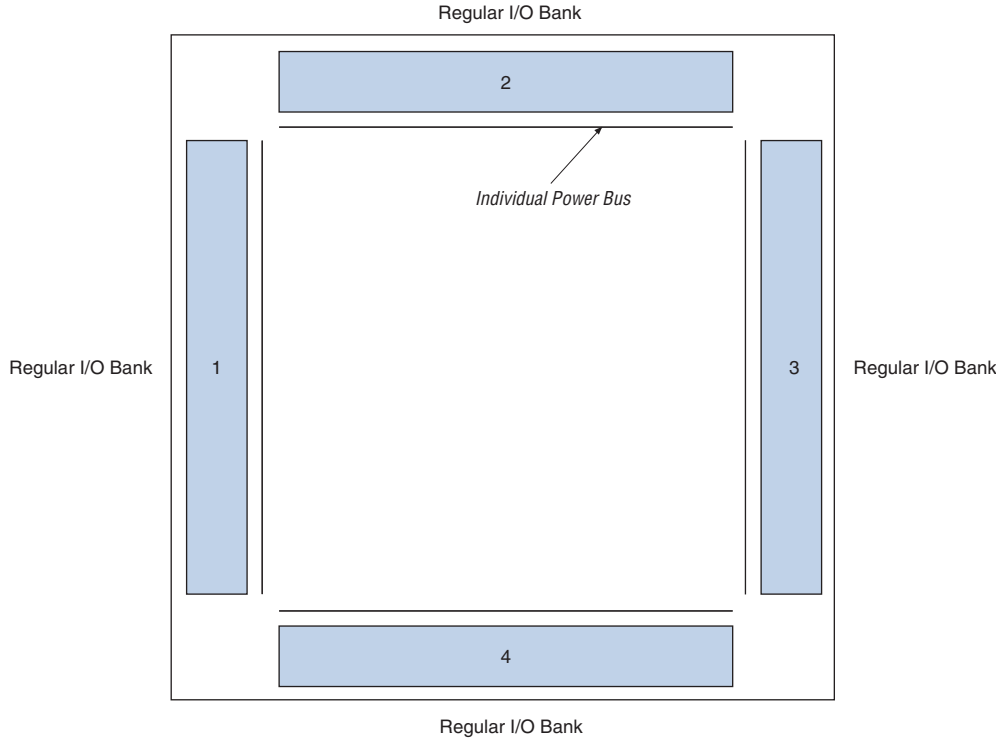
byteena [3:0]	Affected Port
[1:0]	Port A *(1)*
[3:2]	Port B *(1)*

Note to Table 8–4:
(1) For any data width up to ×18 for each port.

Figure 8–2 shows how the `wren` and `byteena` signals control the operations of the RAM.

When a byte enable bit is de-asserted during a write cycle, the corresponding data byte output appears as a "don't care" or unknown value. When a byte enable bit is asserted during a write cycle, the corresponding data byte output is the newly written data.

Figure 10–19. EP2C5 and EP2C8 Device I/O Banks *Notes (1), (2)*

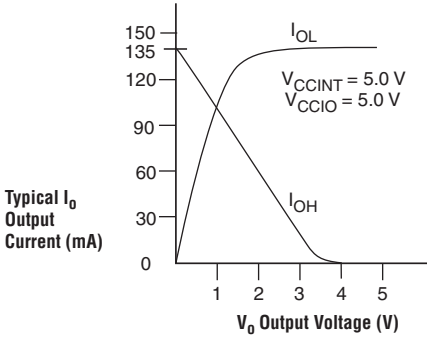


Notes to Figure 10–19:

(1) This is a top view of the silicon die.

(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Figure 10–22. Output Drive Characteristics of a 5.0-V Device



As shown above, R_1 = 5.0-V/135 mA.

The values shown in data sheets usually reflect typical operating conditions. Subtract 20% from the data sheet value for guard band. This subtraction when applied in the example in Figure 10–22 gives R_1 a value of 30 Ω

R_2 should be selected so that it does not violate the driving device's I_{OH} specification. For example, if the device has a maximum I_{OH} of 8 mA, given that the PCI clamping diode, $V_{IN} = V_{CCIO} + 0.7\text{-V} = 3.7\text{-V}$, and the maximum supply load of a 5.0-V device (V_{CC}) is 5.25-V, the value of R_2 can be calculated as follows:

$$R_2 = \frac{(5.25\ V - 3.7\ V) - (8\ mA \times 30\ \Omega)}{8\ mA} = 164\ \Omega$$

This analysis assumes worst case conditions. If your system does not have a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because 5.0-V device tolerance in Cyclone II devices requires use of the PCI clamp, and this clamp is activated during configuration, 5.0-V signals may not be driven into the device until it is configured.

Conclusion

Cyclone II device I/O capabilities enable you to keep pace with increasing design complexity utilizing a low-cost FPGA device family. Support for I/O standards including SSTL and LVDS compatibility allow Cyclone II devices to fit into a wide variety of applications. The Quartus II

Figure 11–12. Differential SSTL Class I Interface

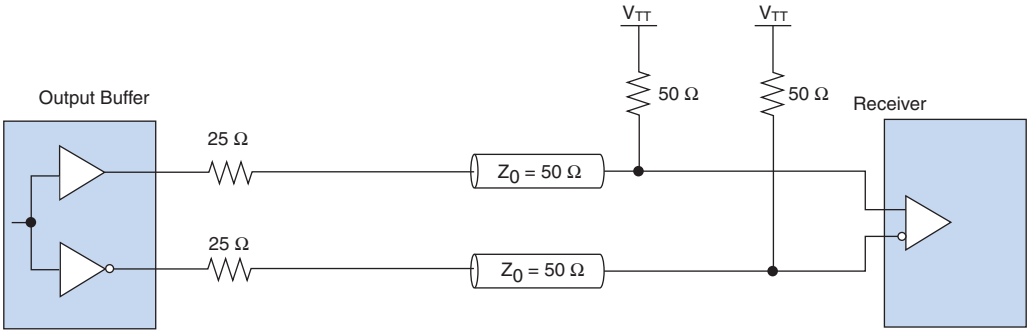
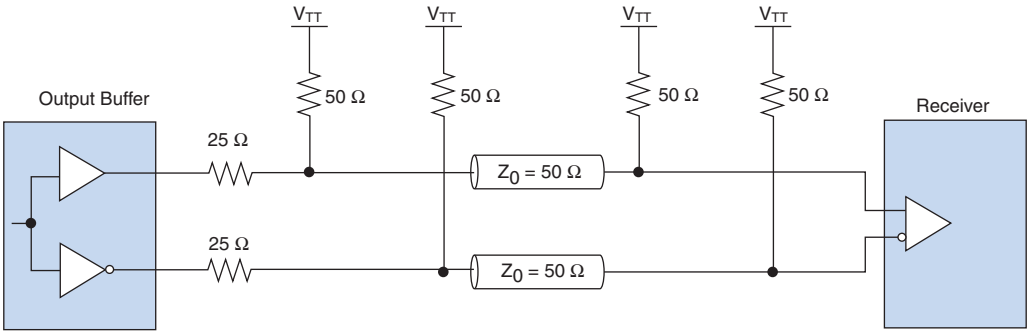


Figure 11–13. Differential SSTL Class II Interface



Differential HSTL Support in Cyclone II Devices

The differential HSTL AC and DC specifications are the same as the HSTL single-ended specifications. The differential HSTL I/O standard is available on the GCLK pins only, treating differential inputs as two single-ended HSTL, and only decoding one of them. The differential HSTL output I/O standard is only supported at the PLLCLKOUT pins using two single-ended HSTL output buffers with the second output programmed as inverted. The standard requires two differential inputs with an external termination voltage (V_{TT}) of 0.5 × V_{CCIO} to which termination resistors are connected.

For the HSTL signaling characteristics, see the *DC Characteristics & Timing Specifications* chapter and the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook.*

PS Configuration

You can use an Altera configuration device, a download cable, or an intelligent host, such as a MAX® II device or microprocessor to configure a Cyclone II device with the PS scheme. In the PS scheme, an external host (configuration device, MAX II device, embedded processor, or host PC) controls configuration. Configuration data is input to the target Cyclone II devices via the DATA0 pin at each rising edge of DCLK.

The Cyclone II decompression feature is fully available when configuring your Cyclone II device using PS mode.

Table 13–6 shows the MSEL pin settings when using the PS configuration scheme.

Table 13–6. Cyclone II MSEL Pin Settings for PS Configuration Schemes

Configuration Scheme	MSEL1	MSEL0
PS	0	1

Single Device PS Configuration Using a MAX II Device as an External Host

In the PS configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone II device. Configuration data can be stored in RBF, HEX, or TTF format. Figure 13–9 shows the configuration interface connections between the Cyclone II device and a MAX II device for single device configuration.

In addition, because the nSTATUS pins are connected, all the Cyclone II devices in the chain stop configuration if any device detects an error. If this happens, you must manually restart configuration in the Quartus II software.

Figure 13–20 shows how to configure multiple Cyclone II devices with a download cable.

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 3 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bidirectional open-drain	This pin is a status output and input. The target Cyclone II device drives the CONF_DONE pin low before and during configuration. Once the Cyclone II device receives all the configuration data without error and the initialization cycle starts, it releases CONF_DONE. Driving CONF_DONE low during user mode does not affect the configured device. Do not drive CONF_DONE low before the device enters user mode. After the Cyclone II device receives all the data, the CONF_DONE pin transitions high, and the device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device. The enhanced configuration devices' and EPC2 devices' OE and nCS pins are connected to the Cyclone II device's nSTATUS and CONF_DONE pins, respectively, and have optional internal programmable pull-up resistors. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on these pins. When using EPC2 devices, you should only use external 10-kΩ pull-up resistors. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.
nCE	N/A	All	Input	This pin is an active-low chip enable. The nCE pin activates the device with a low signal to allow configuration. The nCE pin must be held low during configuration, initialization, and user mode. In single device configuration, it should be tied low. In multiple device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. The nCE pin must also be held low for successful JTAG programming of the FPGA. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.