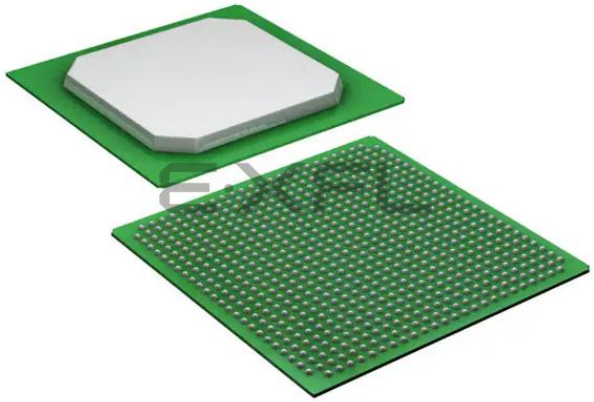

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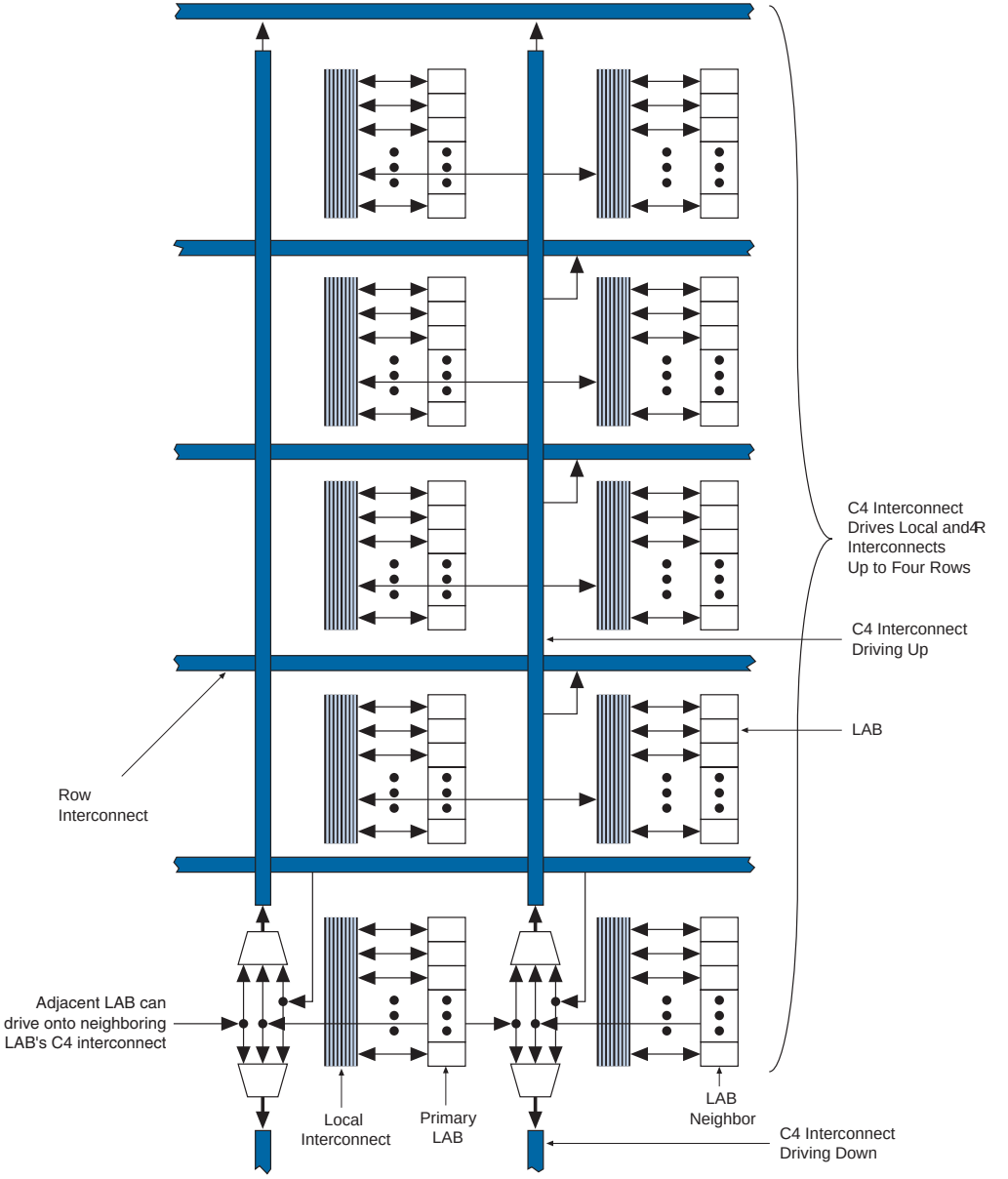
Details	
Product Status	Active
Number of LABs/CLBs	4276
Number of Logic Elements/Cells	68416
Total RAM Bits	1152000
Number of I/O	422
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c70f672c6n

Figure 2–10. C4 Interconnect Connections Note (1)



Note to Figure 2–10

(1) Each C4 interconnect can drive either up or down four rows.

Slew Rate Control

Slew rate control is performed by using programmable output drive strength.

Bus Hold

Each Cyclone II device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals.

1 If the bus-hold feature is enabled, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus hold circuitry is not available on the dedicated clock pins.

The bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 k to pull the signal level to the last-driven state. Refer to the DC Characteristics & Timing Specifications chapter in Volume 1 of the Cyclone II Device Handbook for the specific sustaining current for each V_{CCIO} voltage level driven through the resistor and overdrive current used to identify the next driven input level.

Programmable Pull-Up Resistor

Each Cyclone II device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 k) holds the output to the V_{CCIO} level of the output pin's bank.

1 If the programmable pull-up is enabled, the device cannot use the bus-hold feature. The programmable pull-up resistors are not supported on the dedicated configuration, JTAG, and dedicated clock pins.

5. DC Characteristics and Timing Specifications

CII51005-4.0

Operating Conditions

Cyclone® II devices are offered in commercial, industrial, automotive, and extended temperature grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the parameter values in this chapter apply to all Cyclone II devices. AC and DC characteristics are specified using the same numbers for commercial, industrial, and automotive grades. All parameters representing voltages are measured with respect to ground.

Tables 5–1 through 5–4 provide information on absolute maximum ratings.

Table 5–1. Cyclone II Device Absolute Maximum Ratings Notes (1), (2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Output supply voltage		–0.5	4.6	V
V_{CCA_PLL} [1..4]	PLL supply voltage		–0.5	1.8	V
V_{IN}	DC input voltage (3)	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	—	125	°C

Notes to Table 5–1:

(1) Conditions beyond those listed in this table cause permanent damage to a device. These are stress ratings only. Functional operation at these levels or any other conditions beyond those specified in this chapter is not implied. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effect on the device reliability.

(2) Refer to the Operating Requirements for Altera Devices Data Sheet for more information.

(3) During transitions, the inputs may overshoot to the voltage shown in Table 5–4 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transition, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Single-Ended I/O Standards

Tables 5–6 and 5–7 provide operating condition information when using single-ended I/O standards with Cyclone II devices. Table 5–5 provides descriptions for the voltage and current symbols used in Tables 5–6 and 5–7.

Table 5–5. Voltage and Current Symbol Definitions

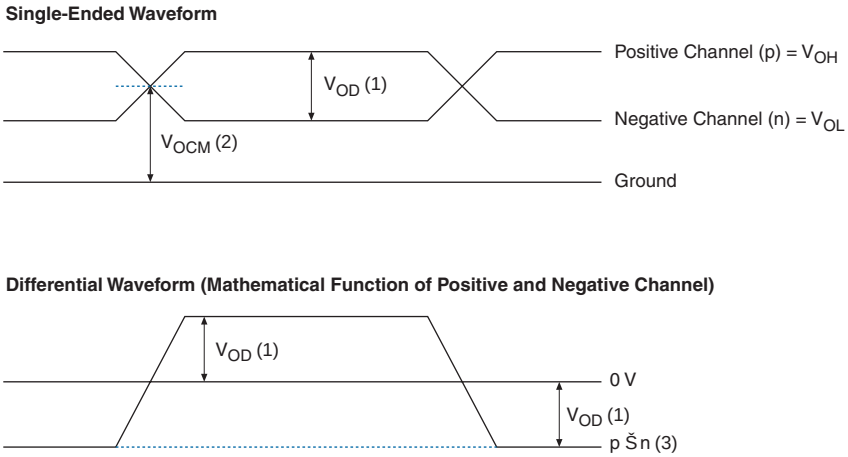
Symbol	Definition
V_{CCIO}	Supply voltage for single-ended inputs and for output drivers
V_{REF}	Reference voltage for setting the input switching threshold
V_{IL}	Input voltage that indicates a low logic level
V_{IH}	Input voltage that indicates a high logic level
V_{OL}	Output voltage that indicates a low logic level
V_{OH}	Output voltage that indicates a high logic level
I_{OL}	Output current condition under which V_{OL} is tested
I_{OH}	Output current condition under which V_{OH} is tested
V_{TT}	Voltage applied to a resistor termination as specified by HSTL and SSTL standards

Table 5–6. Recommended Operating Conditions for User I/O Pins Using Single-Ended I/O Standards Note (1) *(Part 1 of 2)*

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{IL} (V)	V_{IH} (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
3.3-V LVTTL and LVCMOS	3.135	3.3	3.465	—	—	—	0.8	1.7
2.5-V LVTTL and LVCMOS	2.375	2.5	2.625	—	—	—	0.7	1.7
1.8-V LVTTL and LVCMOS	1.710	1.8	1.890	—	—	—	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
1.5-V LVCMOS	1.425	1.5	1.575	—	—	—	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$
PCI and PCI-X	3.000	3.3	3.600	—	—	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$
SSTL-2 class I	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF} - 0.18$ (DC) $V_{REF} - 0.35$ (AC)	$V_{REF} + 0.18$ (DC) $V_{REF} + 0.35$ (AC)
SSTL-2 class II	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF} - 0.18$ (DC) $V_{REF} - 0.35$ (AC)	$V_{REF} + 0.18$ (DC) $V_{REF} + 0.35$ (AC)
SSTL-18 class I	1.7	1.8	1.9	0.833	0.9	0.969	$V_{REF} - 0.125$ (DC) $V_{REF} - 0.25$ (AC)	$V_{REF} + 0.125$ (DC) $V_{REF} + 0.25$ (AC)

Figure 5–2 shows the transmitter output waveforms for all supported differential output standards (LVDS, mini-LVDS, RSDS, differential 1.5-V HSTL class I and II, differential 1.8-V HSTL class I and II, differential SSTL-2 class I and II, and differential SSTL-18 class I and II).

Figure 5–2. Transmitter Output Waveforms for Differential I/O Standards



Notes to Figure 5–2
(1) V_{OD} is the output differential voltage. $V_{OD} = |p - n|$.
(2) V_{OCM} is the output common mode voltage. $V_{OCM} = (p + n)/2$.
(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–9 shows the DC characteristics for user I/O pins with differential I/O standards.

Table 5–9. DC Characteristics for User I/O Pins Using Differential I/O Standards Note (1) *(Part 1 of 2)*

I/O Standard	V_{OD} (mV)			V_{OD} (mV)		V_{OCM} (V)			V_{OH} (V)		V_{OL} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS	250	—	600	—	50	1.125	1.25	1.375	—	—	—	—
mini-LVDS (2)	300	—	600	—	50	1.125	1.25	1.375	—	—	—	—
RSDS (2)	100	—	600	—	—	1.125	1.25	1.375	—	—	—	—
Differential 1.5-V HSTL class I and II (3)	—	—	—	—	—	—	—	—	V_{CCIO} – 0.4	—	—	0.4

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.2V_DIFFERENTIAL_HSTL	t_{PI}	570	597	1263	1324	1385	1385	ps
	t_{PCOUT}	356	373	801	879	957	957	ps

Notes to Table 5–40:
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–41. Cyclone II I/O Input Delay for Row Pins (Part 1 of 2)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
LVTTL	t_{PI}	583	611	1129	1160	1240	1240	ps
	t_{PCOUT}	366	384	762	784	855	855	ps
2.5V	t_{PI}	629	659	1099	1171	1244	1244	ps
	t_{PCOUT}	412	432	732	795	859	859	ps
1.8V	t_{PI}	729	764	1278	1360	1443	1443	ps
	t_{PCOUT}	512	537	911	984	1058	1058	ps
1.5V	t_{PI}	794	832	1345	1429	1513	1513	ps
	t_{PCOUT}	577	605	978	1053	1128	1128	ps
LVCMOS	t_{PI}	583	611	1129	1160	1240	1240	ps
	t_{PCOUT}	366	384	762	784	855	855	ps
SSTL_2_CLASS_I	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
SSTL_2_CLASS_II	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
SSTL_18_CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
SSTL_18_CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.5V_HSTL_CLASS_I	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps

The VCO frequency is a critical parameter that must be between 300 and 1,000 MHz to ensure proper operation of the PLL. The Quartus II software automatically sets the VCO frequency within the recommended range based on the clock output and phase-shift requirements in your design.

PLL Reference Clock Generation

In Cyclone II devices, up to four clock pins can drive the PLL, as shown in Figure 7–11 on page 7–26. The multiplexer output feeds the PLL reference clock input. The PLL has internal delay elements that compensate for the clock delay from the input pin to the clock input port of the PLL.

Table 7–3 shows the clock input pin connections to the PLLs in the Cyclone II device.

Table 7–3. PLL Clock Input Pin Connections

Device	PLL 1		PLL 2		PLL 3		PLL 4	
	CLK0 CLK1	CLK2 CLK3	CLK4 CLK5	CLK6 CLK7	CLK8 CLK9	CLK10 CLK11	CLK12 CLK13	CLK14 CLK15
EP2C5	v	v	v v					
EP2C8	v	v	v v					
EP2C15	v	v	v v	v	v	v	v	
EP2C20	v	v	v v	v	v	v	v	
EP2C35	v	v	v v	v	v	v	v	
EP2C50	v	v	v v	v	v	v	v	
EP2C70	v	v	v v	v	v	v	v	

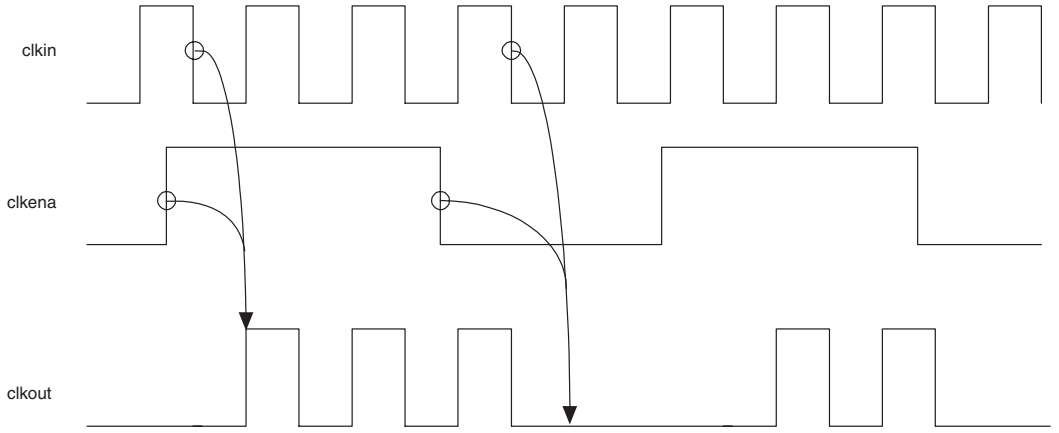
Each PLL can be fed by one of four single-ended or two differential clock input pins. For example, PLL 1 can be fed by CLK[3..0] when using a single-ended I/O standard. When your design uses a differential I/O standard, these same clock pins have a secondary function as LVDSCLK[2..1]p and LVDSCLK[2..1]n pins. When using differential clocks, the CLK0 pin's secondary function is LVDSCLK1p, the CLK1 pin's secondary function is LVDSCLK1n, etc.

Table 7–5. PLL Output signals			
Port	**Description**	**Source**	**Destination**
c[2..0]	PLL clock outputs driving the internal global clock network or external clock output pin (PLL<#>_OUT)	PLL post-scale counter	Global clock network or external I/O pin
Locked	Gives the status of the PLL lock. When the PLL is locked, this port drives V_{CC}. When the PLL is out of lock, this port drives GND. The locked port may pulse high and low during the PLL lock process.	PLL lock detect circuit	Logic array or output pin

Table 7–6 shows a list of I/O standards supported in Cyclone II device PLLs.

Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 1 of 2)			
I/O Standard	**Input**	**Output**	
	inclk	**lock**	**pll_out**
LVTTL (3.3, 2.5, and 1.8 V)	v	v	v
LVCMOS (3.3, 2.5, 1.8, and 1.5 V)	v	v	v
3.3-V PCI	v	v	v
3.3-V PCI-X (1)	v	v	v
LVPECL	v		
LVDS	v	v	v
1.5 and 1.8 V differential HSTL class I and class II	v		v (2)
1.8 and 2.5 V differential SSTL class I and class II	v		v (2)
1.5-V HSTL class I	v	v	v
1.5-V HSTL class II (3)	v	v	v
1.8-V HSTL class I	v	v	v
1.8-V HSTL class II (3)	v	v	v
SSTL-18 class I	v	v	v
SSTL-18 class II (3)	v	v	v
SSTL-25 class I	v	v	v

Figure 7–15. clkena Implementation



The clkena signal can also disable clock outputs if the system is not tolerant to frequency overshoot during PLL resynchronization.

Altera recommends using the clkena signals when switching the clock source to the PLLs or the global clock network. The recommended sequence to be followed is:

1. Disable the primary output clock by de-asserting the clkena signal.
2. Switch to the secondary clock using the dynamic select signals of the clock control block.
3. Allow some clock cycles of the secondary clock to pass before re-asserting the clkena signal. The exact number of clock cycles you need to wait before enabling the secondary clock is design dependent. You can build custom logic to ensure glitch-free transition when switching between different clock sources.

Board Layout

The PLL circuits in Cyclone II devices contain analog components embedded in a digital device. These analog components have separate power and ground pins to minimize noise generated by the digital components.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
Differential HSTL-15 class I or class II	Pseudo differential (3)	(4)	1.5 V	—	—	—	v (6)	—
		1.5 V	(4)	v (5)	—	v (5)	—	—
Differential HSTL-18 class I or class II	Pseudo differential (3)	(4)	1.8 V	—	—	—	v (6)	—
		1.8 V	(4)	v (5)	—	v (5)	—	—
LVDS	Differential	2.5 V	2.5 V	v	v v		v v	
RSDS and mini-LVDS (7)	Differential	(4)	2.5 V	—	v	—	v	v
LVPECL (8)	Differential	3.3 V/ 2.5 V/ 1.8 V/ 1.5 V	(4)	v	—	v	—	—

Notes to Table 10–1:

(1) These pins support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.
(2) PCI-X does not meet the IV curve requirement at the linear region. PCI-clamp diode is not available on top and bottom I/O pins.
(3) Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Pseudo-differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them.
(4) This I/O standard is not supported on these I/O pins.
(5) This I/O standard is only supported on the dedicated clock pins.
(6) PLL_OUTdoes not support differential SSTL-18 class II and differential 1.8 and 1.5-V HSTL class II.
(7) mini-LVDS and RSDS are only supported on output pins.
(8) LVPECL is only supported on clock inputs, not DQS and dual-purpose clock pins.

3.3-V LVTTL (EIA/JEDEC Standard JESD8-B)

The 3.3-V LVTTL I/O standard is a general-purpose, single-ended standard used for 3.3-V applications. The LVTTL standard defines the DC interface parameters for digital circuits operating from a 3.0-/3.3-V power supply and driving or being driven by LVTTL-compatible devices.

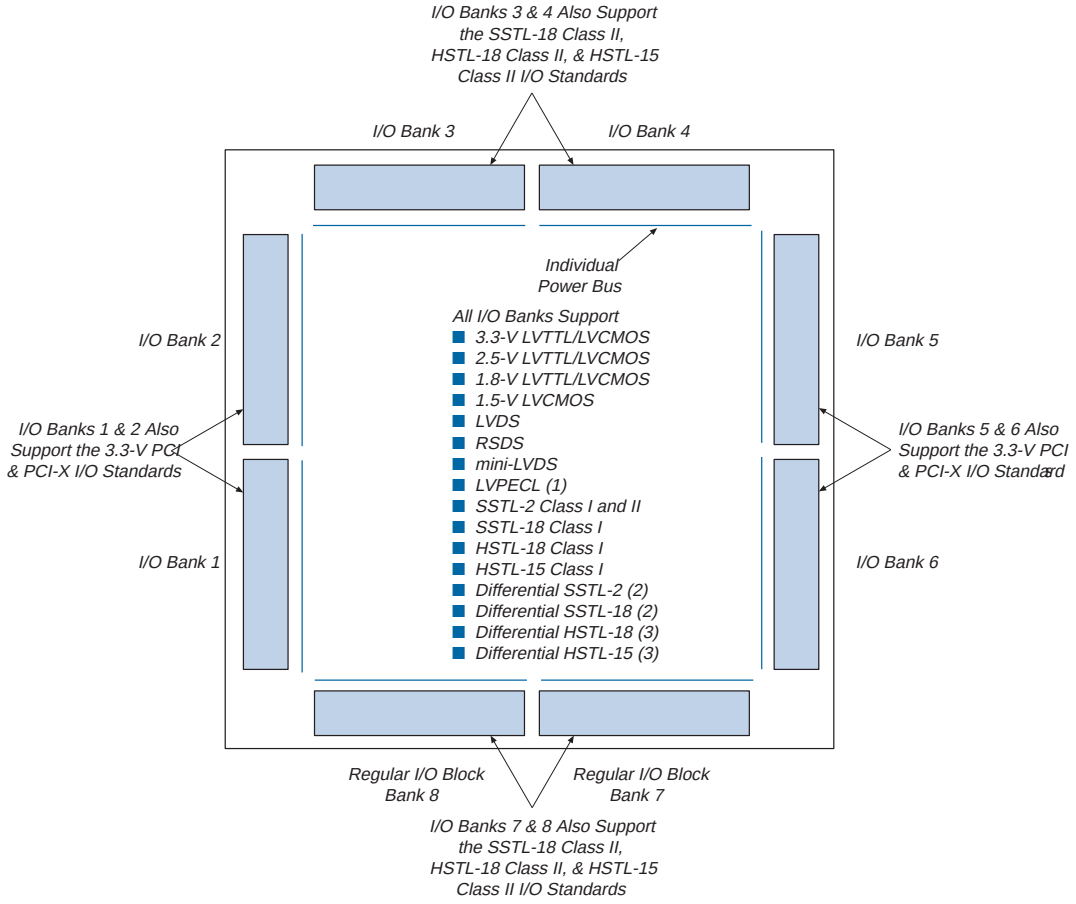
The LVTTL input standard specifies a wider input voltage range of – 0.3 V V_I 3.9 V. Altera recommends an input voltage range of – 0.5 V V_I 4.1 V.

Table 10–6. Programmable Drive Strength (Part 2 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Side I/O Pins
SSTL-2 class I	8	8
	12	12
SSTL-2 class II	16	16
	20	—
	24	—
SSTL-18 class I	6	6
	8	8
	10	10
	12	—
SSTL-18 class II	16	—
	18	—
HSTL-18 class I	8	8
	10	10
	12	12
HSTL-18 class II	16	N/A
	18	—
	20	—
HSTL-15 class I	8	8
	10	—
	12	—
HSTL-15 class II	16	N/A

These drive-strength settings are programmable on a per-pin basis using the Quartus II software.

Figure 11–2. I/O Banks in EP2C15, EP2C20, EP2C35, EP2C50 & EP2C70 Devices



Notes to Figure 11–2

(1) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(2) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.

(3) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

Cyclone II High-Speed I/O Interface

Cyclone II devices provide a multi-protocol interface that allows communication between a variety of I/O standards, including LVDS, LVPECL, RSDS, mini-LVDS, differential HSTL, and differential SSTL. This feature makes the Cyclone II device family ideal for applications that require multiple I/O standards, such as protocol translation.

Upon power-up, the Cyclone II device goes through a POR. During POR, the device reset, holds nSTATUSand CONF_DONEow, and tri-states all user I/O pins. After POR, which typically lasts 100 ms, the Cyclone II FPGA releases nSTATUSand enters configuration mode when this signal is pulled high by the external 10-k resistor. Once the FPGA successfully exits POR, all user I/O pins continue to be tri-stated. Cyclone II devices have weak pull-up resistors on the user I/O pins which are on before and during configuration.

The configuration device also goes through a POR delay to allow the power supply to stabilize. The maximum POR time for EPC2 or EPC1 devices is 200 ms. The POR time for enhanced configuration devices can be set to 100 ms or 2 ms, depending on the enhanced configuration device's PORSELpin setting. If the PORSELpin is connected to ground, the POR delay is 100 ms. If the PORSELpin is connected to V_{CC}, the POR delay is 2 ms. You must power the Cyclone II device before or during the enhanced configuration device POR time. During POR, the configuration device transitions its OEpin low. This low signal delays configuration because the OEpin is connected to the target device's nSTATUSpin. When the target and configuration devices complete POR, they both release the nSTATUSto OEline, which is then pulled high by a pull-up resistor.

When the power supplies have reached the appropriate operating voltages, the target FPGA senses the low-to-high transition on nCONFIG and initiates the configuration cycle. The configuration cycle consists of three stages: reset, configuration, and initialization.

1 The Cyclone II device does not have a PORSELpin.

Reset Stage

While nCONFIGor nSTATUSis low, the device is in reset. You can delay configuration by holding the nCONFIGor nSTATUSpin low.

1 V_{CCINT} and V_{CCIO} of the banks where the configuration and JTAG pins reside need to be fully powered to the appropriate voltage levels in order to begin the configuration process.

When the nCONFIGsignal goes high, the device comes out of reset and releases the nSTATUSpin, which is pulled high by a pull-up resistor. Enhanced configuration and EPC2 devices have an optional internal pull-up resistor on the OEpin. You can turn on this option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If this internal pull-up resistor is not used, you need to connect an external 10-k pull-up resistor to the OEand nSTATUSline. Once nSTATUSis released, the FPGA is ready to receive configuration data and the configuration stage begins.

it feeds the next device's nCE pin. After the first device in the chain completes configuration, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration. The nCEO pin is a dual-purpose pin in Cyclone II devices.

1 The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the device is in a chain, and the nCEO pin is connected to the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O pin after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

Connect all other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) to every Cyclone II device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Buffer the DCLK and DATA lines for every fourth device.

When configuring multiple devices, configuration does not begin until all devices release their OE or nSTATUS pins. Similarly, since all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

You should not pull CONF_DONE low to delay initialization. Instead, use the Quartus II software's **User-Supplied Start-Up Clock** option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain initialize together since their CONF_DONE pins are tied together.

Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if there is an error when configuring the first Cyclone II device, it resets the chain by pulling its nSTATUS pin low. This low signal drives the OE pin low on the enhanced configuration device and drives nSTATUS low on all FPGAs, which causes them to enter a reset state.

If the **Auto-restart configuration after error** option is turned on, the devices automatically initiate reconfiguration if an error occurs. The FPGAs release their nSTATUS pins after a reset time-out period (40 µs maximum). When all the nSTATUS pins are released and pulled high, the configuration device reconfigures the chain. If the **Auto-restart configuration after error** option is turned off, a microprocessor or controller must monitor the nSTATUS pin for errors and then pulse