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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	4276
Number of Logic Elements/Cells	68416
Total RAM Bits	1152000
Number of I/O	422
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c70f672i8

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

| Table 2–8. M4K Clock Modes	
Clock Mode	**Description**
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, wren, and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, wraddress, and wren. The read clock controls the data output, rdaddress, and rden.
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

Table 2–9. Cyclone II M4K Memory Clock Modes			
Clocking Modes	**True Dual-Port Mode**	**Simple Dual-Port Mode**	**Single-Port Mode**
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Figure 2–18. Multiplier Block Architecture
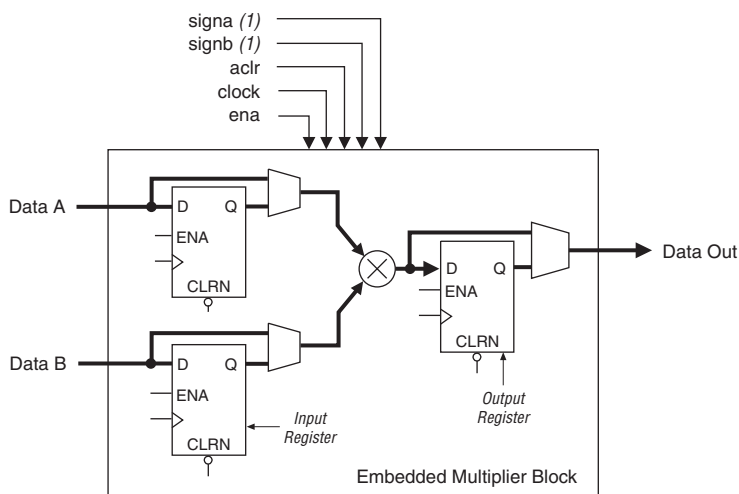
Note to Figure 2–18:
(1)   If necessary, these signals can be registered once to match the data signal path.

Each multiplier operand can be a unique signed or unsigned number. Two signals, signa and signb, control the representation of each operand respectively. A logic 1 value on the signa signal indicates that data A is a signed number while a logic 0 value indicates an unsigned number. Table 2–11 shows the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

Table 2–11. Multiplier Sign Representation

Data A (signa Value)	Data B (signb Value)	Result
Unsigned	Unsigned	Unsigned
Unsigned	Signed	Signed
Signed	Unsigned	Signed
Signed	Signed	Signed

Table 5–3. DC Characteristics for User I/O, Dual-Purpose, and Dedicated Pins (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{CONF} (5) (6)	Value of I/O pin pull-up resistor before and during configuration	$V_{IN} = 0$ V; $V_{CCIO} = 3.3$ V	10	25	50	kΩ
		$V_{IN} = 0$ V; $V_{CCIO} = 2.5$ V	15	35	70	kΩ
		$V_{IN} = 0$ V; $V_{CCIO} = 1.8$ V	30	50	100	kΩ
		$V_{IN} = 0$ V; $V_{CCIO} = 1.5$ V	40	75	150	kΩ
		$V_{IN} = 0$ V; $V_{CCIO} = 1.2$ V	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	(7)	—	1	2	kΩ

Notes to Table 5–3:

(1)   All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(2)   The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltages shown in Table 5–4, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(3)   This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(4)   Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (www.altera.com) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to "Power Consumption" on page 5–13 for more information.

(5) R_{CONF} values are based on characterization. $R_{CONF} = V_{CCIO}/I_{RCONF}$. R_{CONF} values may be different if V_{IN} value is not 0 V. Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

(6)   Minimum condition at –40°C and high V_{CC}, typical condition at 25°C and nominal V_{CC} and maximum condition at 125°C and low V_{CC} for R_{CONF} values.

(7)   These values apply to all V_{CCIO} settings.

Table 5–4 shows the maximum V_{IN} overshoot voltage and the dependency on the duty cycle of the input signal. Refer to Table 5–3 for more information.

Table 5–4. V_{IN} Overshoot Voltage for All Input Buffers

Maximum V_{IN} (V)	Input Signal Duty Cycle
4.0	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

IOE Programmable Delay

Refer to Table 5–36 and 5–37 for IOE programmable delay.

Table 5–36. Cyclone II IOE Programmable Delay on Column Pins Notes (1), (2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		−6 Speed Grade		−7 Speed Grade (4)		−8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad -> I/O dataout to core	7	0	2233	0	3827	0	4232	0	4349	ps
			0	2344	—	—	0	4088	—	—	ps
Input Delay from Pin to Input Register	Pad -> I/O input register	8	0	2656	0	4555	0	4914	0	4940	ps
			0	2788	—	—	0	4748	—	—	ps
Delay from Output Register to Output Pin	I/O output register -> Pad	2	0	303	0	563	0	638	0	670	ps
			0	318	—	—	0	617	—	—	ps

Notes to Table 5–36:
(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.
(3) The value in the first row for each parameter represents the fast corner timing parameter for industrial and automotive devices. The second row represents the fast corner timing parameter for commercial devices.
(4) The value in the first row is for automotive devices. The second row is for commercial devices.

Table 5–37. Cyclone II IOE Programmable Delay on Row Pins Notes (1), (2) (Part 1 of 2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		−6 Speed Grade		−7 Speed Grade (4)		−8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad -> I/O dataout to core	7	0	2240	0	3776	0	4174	0	4290	ps
			0	2352	—	—	0	4033	—	—	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 5 of 6)									
I/O Standard	Drive Strength	Parameter	Fast Corner		−6 Speed Grade	−7 Speed Grade *(2)*	−7 Speed Grade *(3)*	−8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
DIFFERENTIAL_ SSTL_18_CLASS_I	6 mA	t_{OP}	1472	1544	3140	3345	3542	3549	ps
		t_{DIP}	1604	1683	3310	3539	3768	3768	ps
	8 mA	t_{OP}	1469	1541	3086	3287	3482	3489	ps
		t_{DIP}	1601	1680	3256	3481	3708	3708	ps
	10 mA	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
	12 mA *(1)*	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
DIFFERENTIAL_ SSTL_18_CLASS_II	16 mA	t_{OP}	1454	1525	2905	3088	3263	3270	ps
		t_{DIP}	1586	1664	3075	3282	3489	3489	ps
	18 mA *(1)*	t_{OP}	1453	1524	2900	3082	3257	3264	ps
		t_{DIP}	1585	1663	3070	3276	3483	3483	ps
1.8V_DIFFERENTIAL _HSTL_CLASS_I	8 mA	t_{OP}	1460	1531	3222	3424	3618	3625	ps
		t_{DIP}	1592	1670	3392	3618	3844	3844	ps
	10 mA	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
	12 mA *(1)*	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
1.8V_DIFFERENTIAL _HSTL_CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA *(1)*	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_DIFFERENTIAL _HSTL_CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA *(1)*	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 2 of 4)										
		Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins (1)			Row I/O Pins (1)			Dedicated Clock Outputs		
I/O Standard	Drive Strength	−6 Speed Grade	−7 Speed Grade	−8 Speed Grade	−6 Speed Grade	−7 Speed Grade	−8 Speed Grade	−6 Speed Grade	−7 Speed Grade	−8 Speed Grade
LVCMOS	4 mA	250	210	170	250	210	170	250	210	170
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	310	260	210	310	260	210	310	260	210
	16 mA	320	270	220	—	—	—	—	—	—
	20 mA	350	290	240	—	—	—	—	—	—
	24 mA	370	310	250	—	—	—	—	—	—
2.5V	4 mA	180	150	120	180	150	120	180	150	120
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	440	370	300	—	—	—	—	—	—
	16 mA	450	405	350	—	—	—	—	—	—
1.8V	2 mA	120	100	80	120	100	80	120	100	80
	4 mA	180	150	120	180	150	120	180	150	120
	6 mA	220	180	150	220	180	150	220	180	150
	8 mA	240	200	160	240	200	160	240	200	160
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	350	290	240	350	290	240	350	290	240
1.5V	2 mA	80	60	50	80	60	50	80	60	50
	4 mA	130	110	90	130	110	90	130	110	90
	6 mA	180	150	120	180	150	120	180	150	120
	8 mA	230	190	160	—	—	—	—	—	—
SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
SSTL_18_ CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—

Table 5–53 shows the JTAG timing parameters and values for Cyclone II devices.

Table 5–53. Cyclone II JTAG Timing Parameters and Values					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	
t_{JCP}	TCK clock period	40	—	ns	
t_{JCH}	TCK clock high time	20	—	ns	
t_{JCL}	TCK clock low time	20	—	ns	
t_{JPSU}	JTAG port setup time *(2)*	5	—	ns	
t_{JPH}	JTAG port hold time	10	—	ns	
t_{JPCO}	JTAG port clock to output *(2)*	—	13	ns	
t_{JPZX}	JTAG port high impedance to valid output *(2)*	—	13	ns	
t_{JPXZ}	JTAG port valid output to high impedance *(2)*	—	13	ns	
t_{JSSU}	Capture register setup time *(2)*	5	—	ns	
t_{JSH}	Capture register hold time	10	—	ns	
t_{JSCO}	Update register clock to output	—	25	ns	
t_{JSZX}	Update register high impedance to valid output	—	25	ns	
t_{JSXZ}	Update register valid output to high impedance	—	25	ns	

Notes to Table 5–53:
(1) This information is preliminary.
(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the JTAG port and capture register clock setup time is 3 ns and port clock to output time is 15 ns.

Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Cyclone II devices are in the 18th position or after they will fail configuration. This does not affect the SignalTap® II logic analyzer.

For more information on JTAG, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in the *Cyclone II Handbook.*

Document Revision History

Table 9–4 shows the revision history for this document.

Table 9–4. Document Revision History		
Date & Document Version	**Changes Made**	**Summary of Changes**
February 2007 v3.1	● Added document revision history. ● Added handpara note in "Data & Data Strobe Pins" section. ● Updated "DDR Output Registers" section.	● Elaboration of DDR2 and QDRII interfaces supported by I/O bank included.
November 2005, v2.1	● Introduction ● Updated Table 9–2. ● Updated Figure 9–7.	
July 2005, v2.0	Updated Table 9–2.	
November 2004, v1.1	● Moved the "External Memory Interface Standards" section to follow the "Introduction" section. ● Updated the "Data & Data Strobe Pins" section. ● Updated Figures 9–11, 9–12, 9–15, 9–16, and 9–17.	
June 2004, v1.0	Added document to the Cyclone II Device Handbook.	

10. Selectable I/O Standards in Cyclone II Devices

Introduction

The proliferation of I/O standards and the need for improved I/O performance have made it critical that low-cost devices have flexible I/O capabilities. Selectable I/O capabilities such as SSTL-18, SSTL-2, and LVDS compatibility allow Cyclone® II devices to connect to other devices on the same printed circuit board (PCB) that may require different operating and I/O voltages. With these aspects of implementation easily manipulated using the Altera® Quartus® II software, the Cyclone II device family allows you to use low cost FPGAs while keeping pace with increasing design complexity.

This chapter is a guide to understanding the input and output capabilities of the Cyclone II devices, including:

- Supported I/O standards
- Cyclone II I/O banks
- Programmable current drive strength
- I/O termination
- Pad placement and DC guidelines

👣 For information on hot socketing, refer to the *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information on ESD specifications, refer to the *Altera Reliability Report*.

Supported I/O Standards

Cyclone II devices support the I/O standards shown in Table 10–1.

👣 For more details on the I/O standards discussed in this section, including target data rates and voltage values for each I/O standard, refer to the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*.

11. High-Speed Differential Interfaces in Cyclone II Devices

Introduction

From high-speed backplane applications to high-end switch boxes, low-voltage differential signaling (LVDS) is the technology of choice. LVDS is a low-voltage differential signaling standard, allowing higher noise immunity than single-ended I/O technologies. Its low-voltage swing allows for high-speed data transfers, low power consumption, and reduced electromagnetic interference (EMI). LVDS I/O signaling is a data interface standard defined in the TIA/EIA-644 and IEEE Std. 1596.3 specifications.

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced EMI. National Semiconductor Corporation and Texas Instruments introduced the RSDS and mini-LVDS specifications, respectively. Currently, many designers use these specifications for flat panel display links between the controller and the drivers that drive display column drivers. Cyclone® II devices support the RSDS and mini-LVDS I/O standards at speeds up to 311 megabits per second (Mbps) at the transmitter.
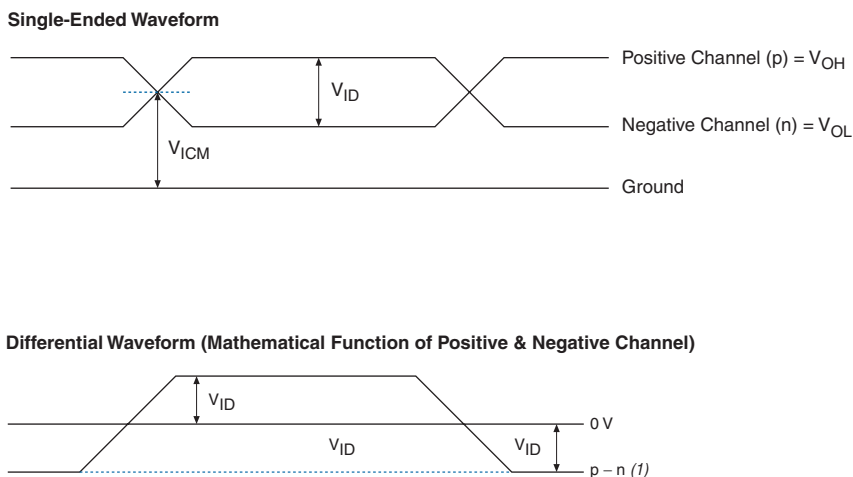
Altera® Cyclone II devices can transmit and receive data through LVDS signals at a data rate of up to 640 Mbps and 805 Mbps, respectively. For the LVDS transmitter and receiver, the Cyclone II device's input and output pins support serialization and deserialization through internal logic.

This chapter describes how to use Cyclone II I/O pins for differential signaling and contains the following topics:

- Cyclone II high-speed I/O banks
- Cyclone II high-speed I/O interface
- LVDS, RSDS, mini-LVDS, LVPECL, differential HSTL, and differential SSTL I/O standards support in Cyclone II devices
- High-speed I/O timing in Cyclone II devices
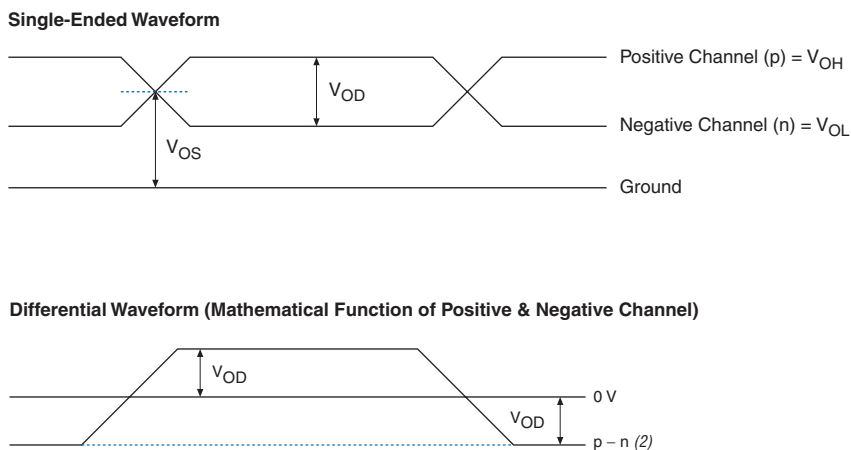- Design guidelines

Cyclone II High-Speed I/O Banks

Cyclone II device I/O banks are shown in Figures 11–1 and 11–2. The EP2C5 and EP2C8 devices offer four I/O banks and EP2C15, EP2C20, EP2C35, EP2C50, and EP2C70 devices offer eight I/O banks. A subset of

Figure 11–4. Receiver Input Waveforms for the LVDS Differential I/O Standard

Single-Ended Waveform

Positive Channel (p) = V_{OH}

Negative Channel (n) = V_{OL}

Ground

V_{ID}

V_{ICM}

Differential Waveform (Mathematical Function of Positive & Negative Channel)

V_{ID}

V_{ID}

V_{ID}

0 V

p – n *(1)*

Note to Figure 11–4:
(1)   The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figure 11–5. Transmitter Output Waveform for the LVDS Differential I/O Standard   *Note (2)*

Single-Ended Waveform

Positive Channel (p) = V_{OH}

Negative Channel (n) = V_{OL}

Ground

V_{OD}

V_{OS}

Differential Waveform (Mathematical Function of Positive & Negative Channel)

V_{OD}

V_{OD}

0 V

p – n *(2)*

Notes to Figure 11–5:
(1)   The V_{OD} specifications apply at the resistor network output.
(2)   The p – n waveform is a function of the positive channel (p) and the negative channel (n).

RSDS I/O Standard Support in Cyclone II Devices

The RSDS specification is used in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the National Semiconductor Corporation RSDS Interface Specification and support the RSDS output standard. Table 11–2 shows the RSDS electrical characteristics for Cyclone II devices.

### Table 11–2. RSDS Electrical Characteristics for Cyclone II Devices   Note (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} (2)	Differential output voltage	R_L = 100 Ω	100		600	mV
V_{OS} (3)	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
T_r/T_f	Transition time	20% to 80%		500		ps

Notes to Table 11–2:
(1)   The specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

Figure 11–6 shows the RSDS transmitter output signal waveforms.

Figure 11–6. Transmitter Output Signal Level Waveforms for RSDS   Note (1)
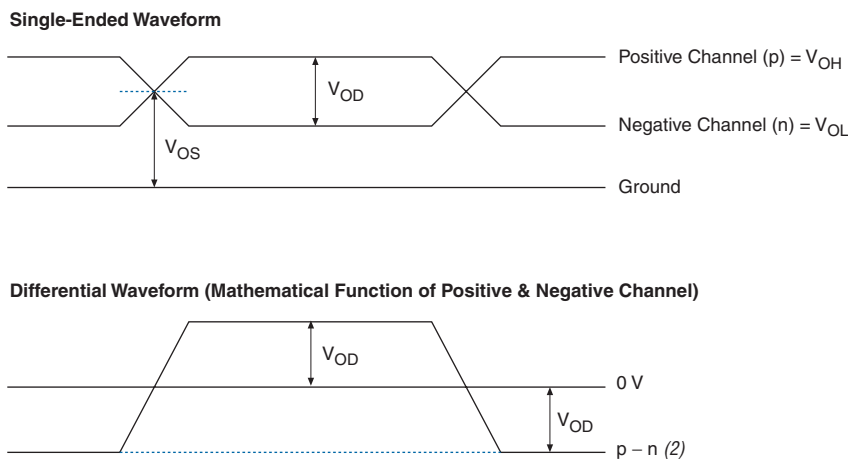
Notes to Figure 11–6:
(1)   The V_{OD} specifications apply at the resistor network output.
(2)   The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Figures 11–14 and 11–15 show differential HSTL class I and II interfaces, respectively.

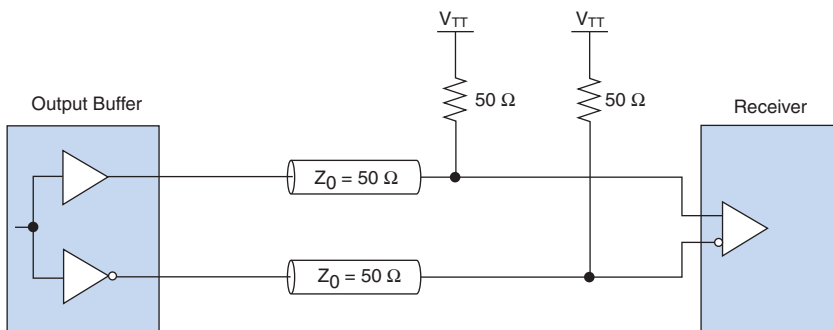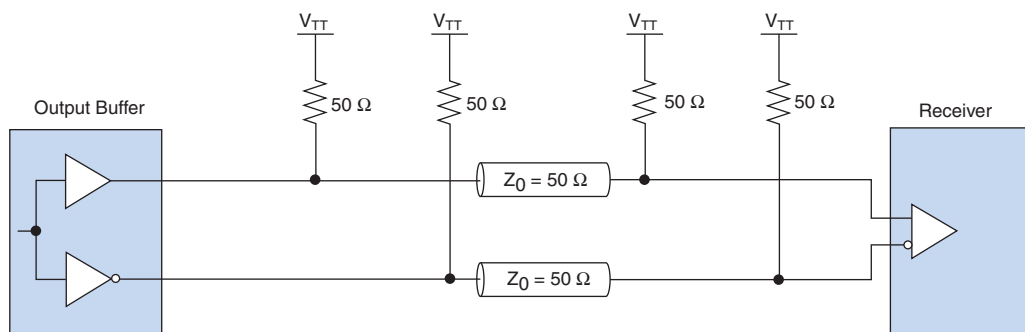*Figure 11–14. Differential HSTL Class I Interface*

Figure 11–15. Differential HSTL Class II Interface

High-Speed I/O Timing in Cyclone II Devices

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Cyclone II devices. LVDS, LVPECL, RSDS, and mini-LVDS I/O standards enable high-speed data transmission. Timing for these high-speed signals is based on skew between the data and the clock signals.

High-speed differential data transmission requires timing parameters provided by integrated circuit (IC) vendors and requires consideration of board skew, cable skew, and clock jitter. This section provides details on high-speed I/O standards timing parameters in Cyclone II devices.

Document Revision History

Table 12–4 shows the revision history for this document.

Table 12–4. Document Revision History		
Date & Document Version	**Changes Made**	**Summary of Changes**
February 2007 v1.2	● Added document revision history. ● Updated "Software Support" section.	● Removed reference to third-party synthesis tool: LeonardoSpectrum and Synplify.
November 2005 v2.1	Updated Introduction.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

During initialization, the initialization clock source is either the Cyclone II 10 MHz (typical) internal oscillator (separate from the AS internal oscillator) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If the internal oscillator is used, the Cyclone II device provides itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. You can also make use of the CLKUSR pin as a user I/O pin, which means you have an additional user I/O pin.

If you want to delay the initialization of the devices in the chain, you can use the CLKUSR pin option. The CLKUSR pin allows you to control when your device enters user mode. This feature also allows you to control the order of when each device enters user mode by feeding a separate clock to each device's CLKUSR pin. By using the CLKUSR pins, you can choose any device in the multiple device chain to enter user mode first and have the other devices enter user mode at a later time.

Different device families may require a different number of initialization clock cycles. Therefore, if your multiple device chain consists of devices from different families, the devices may enter user mode at a slightly different time due to the different number of initialization clock cycles required. However, if the number of initialization clock cycles is similar across different device families or if the devices are from the same family, then the devices enter user mode at the same time. See the respective device family handbook for more information about the number of initialization clock cycles required.

If an error occurs at any point during configuration, the FPGA with the error drives the nSTATUS signal low. If you enable the **Auto-restart configuration after error** option, the entire chain begins reconfiguration after a reset time-out period (a maximum of 40 μs). If the **Auto-restart configuration after error** option is turned off, a microprocessor or controller must monitor nSTATUS for errors and then pulse nCONFIG low to restart configuration. The microprocessor or controller can pulse nCONFIG if it is under system control rather than tied to V_{CC}.

☞ While you can cascade Cyclone II devices, serial configuration devices cannot be cascaded or chained together.

☞ If you use the optional CLKUSR pin and the nCONFIG is pulled low to restart configuration during device initialization, make sure the CLKUSR pin continues to toggle while nSTATUS is low (a maximum of 40 μs).

PS Configuration

You can use an Altera configuration device, a download cable, or an intelligent host, such as a MAX® II device or microprocessor to configure a Cyclone II device with the PS scheme. In the PS scheme, an external host (configuration device, MAX II device, embedded processor, or host PC) controls configuration. Configuration data is input to the target Cyclone II devices via the DATA0 pin at each rising edge of DCLK.

☞ The Cyclone II decompression feature is fully available when configuring your Cyclone II device using PS mode.

Table 13–6 shows the MSEL pin settings when using the PS configuration scheme.

Table 13–6. Cyclone II MSEL Pin Settings for PS Configuration Schemes

Configuration Scheme	MSEL1	MSEL0
PS	0	1

Single Device PS Configuration Using a MAX II Device as an External Host

In the PS configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone II device. Configuration data can be stored in RBF, HEX, or TTF format. Figure 13–9 shows the configuration interface connections between the Cyclone II device and a MAX II device for single device configuration.

Figure 13–14. Multiple Device PS Configuration Using an Enhanced Configuration Device
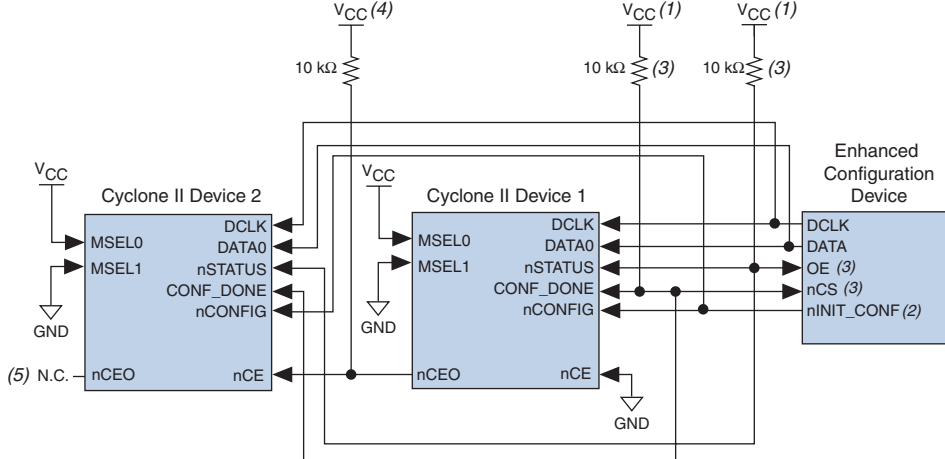
Notes to *Figure 13–14*:
(1)   The pull-up resistor should be connected to the same supply voltage as the configuration device.
(2)   The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V$_{CC}$ either directly or through a resistor (if reconfiguration is required, a resistor is necessary).
(3)   The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.
(4)   Connect the pull-up resistor to the V$_{CCIO}$ supply voltage of I/O bank that the nCEO pin resides in.
(5)   The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

☞   You cannot cascade enhanced configuration devices (EPC16, EPC8, and EPC4 devices).

When configuring multiple devices, you must generate the configuration device's POF from each project's SOF. You can combine multiple SOFs using the **Convert Programming Files** window in the Quartus II software.

👣   For more information on how to create configuration files for multiple device configuration chains, see the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

When configuring multiple devices with the PS scheme, connect the first Cyclone II device's nCE pin to GND and connect its nCEO pin to the nCE pin of the Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's nCEO pin to the V$_{CCIO}$ level when

feature. To use this feature successfully, set the MSEL[1..0] pins of the master Cyclone II device to select the AS configuration scheme or fast AS configuration scheme (see Table 13–1).

☞ The Quartus II software version 4.1 and higher supports serial configuration device ISP through an FPGA JTAG interface using a JIC file.

The serial configuration device in-system programming through the Cyclone II JTAG interface has three stages, which are described in the following sections.

Loading the Serial Flash Loader Design

The serial flash loader design is a design inside the Cyclone II device that bridges the JTAG interface and AS interface inside the Cyclone II device using glue logic.

The intelligent host uses the JTAG interface to configure the master Cyclone II device with a serial flash loader design. The serial flash loader design allows the master Cyclone II device to control the access of four serial configuration device pins, also known as the Active Serial Memory Interface (ASMI) pins, through the JTAG interface. The ASMI pins are the serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS) pins.

If you configure a master Cyclone II device with a serial flash loader design, the master Cyclone II device can enter user mode even though the slave devices in the multiple device chain are not being configured. The master Cyclone II device can enter user mode with a serial flash loader design even though the CONF_DONE signal is externally held low by the other slave devices in chain. Figure 13–25 shows the JTAG configuration of a single Cyclone II device with a serial flash loader design.

240-Pin Plastic Quad Flat Pack (PQFP)

■ All dimensions and tolerances conform to ASME Y14.5M – 1994.
■ Controlling dimension is in millimeters.
■ Pin 1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

Tables 15–9 and 15–10 show the package information and package outline figure references, respectively, for the 240-pin PQFP package.

Table 15–9. 240-Pin PQFP Package Information	
Description	**Specification**
Ordering Code Reference	Q
Package Acronym	PQFP
Leadframe Material	Copper
Lead Finish (Plating)	Regular: 85Sn:15Pb (Typ.) Pb-free: Matte Sn
JEDEC Outline Reference	MS-029 Variation: GA
Maximum Lead Coplanarity	0.003 inches (0.08mm)
Weight	7.0 g
Moisture Sensitivity Level	Printed on moisture barrier bag

Table 15–10. 240-Pin PQFP Package Outline Dimensions (Part 1 of 2)			
Symbol	**Millimeter**		
	Min.	**Nom.**	**Max.**
A	–	–	4.10
A1	0.25	–	0.50
A2	3.20	3.40	3.60
D	34.60 BSC		
D1	32.00 BSC		
E	34.60 BSC		
E1	32.00 BSC		
L	0.45	0.60	0.75
L1	1.30 REF		
S	0.20	–	–
b	0.17	–	0.27
c	0.09	–	0.20