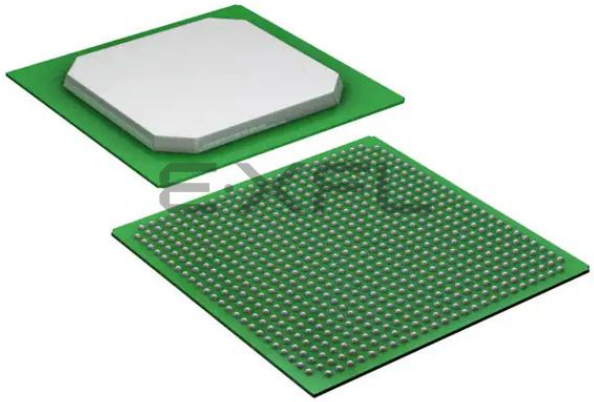


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

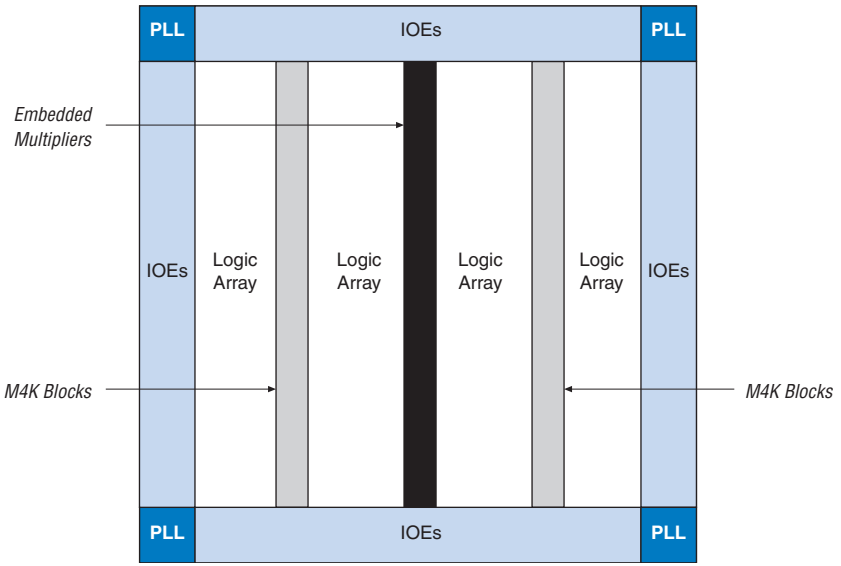
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4276
Number of Logic Elements/Cells	68416
Total RAM Bits	1152000
Number of I/O	422
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c70f672i8n

phase-align double data rate (DDR) signals) provide interface support for external memory devices such as DDR, DDR2, and single data rate (SDR) SDRAM, and QDRII SRAM devices at up to 167 MHz.

Figure 2–1 shows a diagram of the Cyclone II EP2C20 device.

Figure 2–1. Cyclone II EP2C20 Device Block Diagram



The number of M4K memory blocks, embedded multiplier blocks, PLLs, rows, and columns vary per device.

Logic Elements

The smallest unit of logic in the Cyclone II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE features:

- A four-input look-up table (LUT), which is a function generator that can implement any function of four variables
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and direct link interconnects
- Support for register packing
- Support for register feedback

There are five dynamic control input signals that feed the embedded multiplier: `signa`, `signb`, `clk`, `clkena`, and `aclr`. `signa` and `signb` can be registered to match the data signal input path. The same `clk`, `clkena`, and `aclr` signals feed all registers within a single embedded multiplier.

For more information on Cyclone II embedded multipliers, see the *Embedded Multipliers in Cyclone II Devices* chapter.

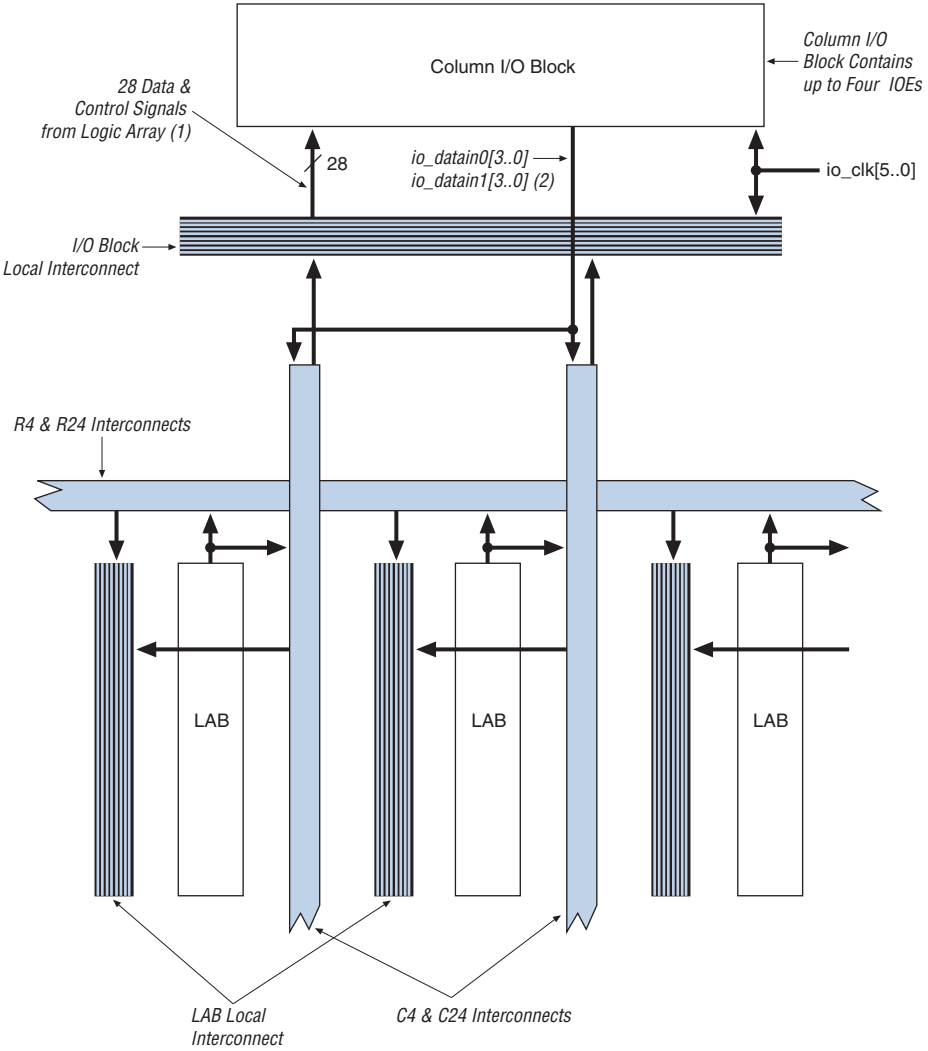
I/O Structure & Features

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- V_{REF} pins

Cyclone II device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–20 shows the Cyclone II IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. You can use IOEs as input, output, or bidirectional pins.

Figure 2–22. Column I/O Block Connection to the Interconnect



Notes to Figure 2–22:

(1) The 28 data and control signals consist of four data out lines, `io_dataout[3..0]`, four output enables, `io_coe[3..0]`, four input clock enables, `io_cce_in[3..0]`, four output clock enables, `io_cce_out[3..0]`, four clocks, `io_cclk[3..0]`, four asynchronous clear signals, `io_caclr[3..0]`, and four synchronous clear signals, `io_csclr[3..0]`.

(2) Each of the four IOEs in the column I/O block can have two `io_datain` (combinational or registered) inputs.

Programmable delays can increase the register-to-pin delays for output registers. Table 2–13 shows the programmable delays for Cyclone II devices.

Table 2–13. Cyclone II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to internal LE registers that reside in two different areas of the device. You set the two combinational input delays by selecting different delays for two different paths under the **Input delay from pin to internal cells logic** option in the Quartus II software. However, if the pin uses the input register, one of delays is disregarded because the IOE only has two paths to internal logic. If the input register is used, the IOE uses one input path. The other input path is then available for the combinational path, and only one input delay assignment is applied.

The IOE registers in each I/O block share the same source for clear or preset. You can program preset or clear for each individual IOE, but both features cannot be used simultaneously. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available for the IOE registers.

External Memory Interfacing

Cyclone II devices support a broad range of external memory interfaces such as SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM external memories. Cyclone II devices feature dedicated high-speed interfaces that transfer data between external memory devices at up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. The programmable DQS delay chain allows you to fine tune the phase shift for the input clocks or strobes to properly align clock edges as needed to capture data.

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 1 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
LVTTL	4 mA	t_{OP}	1524	1599	2903	3125	3341	3348	ps
		t_{DIP}	1656	1738	3073	3319	3567	3567	ps
	8 mA	t_{OP}	1343	1409	2670	2866	3054	3061	ps
		t_{DIP}	1475	1548	2840	3060	3280	3280	ps
	12 mA	t_{OP}	1287	1350	2547	2735	2917	2924	ps
		t_{DIP}	1419	1489	2717	2929	3143	3143	ps
	16 mA	t_{OP}	1239	1299	2478	2665	2844	2851	ps
		t_{DIP}	1371	1438	2648	2859	3070	3070	ps
	20 mA	t_{OP}	1228	1288	2456	2641	2820	2827	ps
		t_{DIP}	1360	1427	2626	2835	3046	3046	ps
	24 mA (1)	t_{OP}	1220	1279	2452	2637	2815	2822	ps
		t_{DIP}	1352	1418	2622	2831	3041	3041	ps
LVCMOS	4 mA	t_{OP}	1346	1412	2509	2695	2873	2880	ps
		t_{DIP}	1478	1551	2679	2889	3099	3099	ps
	8 mA	t_{OP}	1240	1300	2473	2660	2840	2847	ps
		t_{DIP}	1372	1439	2643	2854	3066	3066	ps
	12 mA	t_{OP}	1221	1280	2428	2613	2790	2797	ps
		t_{DIP}	1353	1419	2598	2807	3016	3016	ps
	16 mA	t_{OP}	1203	1262	2403	2587	2765	2772	ps
		t_{DIP}	1335	1401	2573	2781	2991	2991	ps
	20 mA	t_{OP}	1194	1252	2378	2562	2738	2745	ps
		t_{DIP}	1326	1391	2548	2756	2964	2964	ps
	24 mA (1)	t_{OP}	1192	1250	2382	2566	2742	2749	ps
		t_{DIP}	1324	1389	2552	2760	2968	2968	ps

Table 5–44. Maximum Input Clock Toggle Rate on Cyclone II Devices (Part 2 of 2)

I/O Standard	Maximum Input Clock Toggle Rate on Cyclone II Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
DIFFERENTIAL_SSTL_18_CLASS_I	500	500	500	500	500	500	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_II	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.8V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.5V_DIFFERENTIAL_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
LVPECL	—	—	—	—	—	—	402	402	402
LVDS	402	402	402	402	402	402	402	402	402
1.2V_HSTL	110	90	80	—	—	—	110	90	80
1.2V_DIFFERENTIAL_HSTL	110	90	80	—	—	—	110	90	80

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 1 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVTTL	4 mA	120	100	80	120	100	80	120	100	80
	8 mA	200	170	140	200	170	140	200	170	140
	12 mA	280	230	190	280	230	190	280	230	190
	16 mA	290	240	200	290	240	200	290	240	200
	20 mA	330	280	230	330	280	230	330	280	230
	24 mA	360	300	250	360	300	250	360	300	250

6. Reference & Ordering Information

CII51006-1.4

Software

Cyclone® II devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Quartus II Handbook* for more information on the Quartus II software features.

The free Quartus II Web Edition software, available at **www.Altera.com**, supports Microsoft Windows XP and Windows 2000. The full version of Quartus II software is available through the Altera subscription program. The full version of Quartus II software supports all Altera devices, is available for Windows XP, Windows 2000, Sun Solaris, and Red Hat Linux operating systems, and includes a free suite of popular IP MegaCore® functions for DSP applications and interfacing to external memory devices. Quartus II software and Quartus II Web Edition software support seamless integration with your favorite third party EDA tools.

Device Pin-Outs

Device pin-outs for Cyclone II devices are available on the Altera web site (**www.altera.com**). For more information contact Altera Applications.

Ordering Information

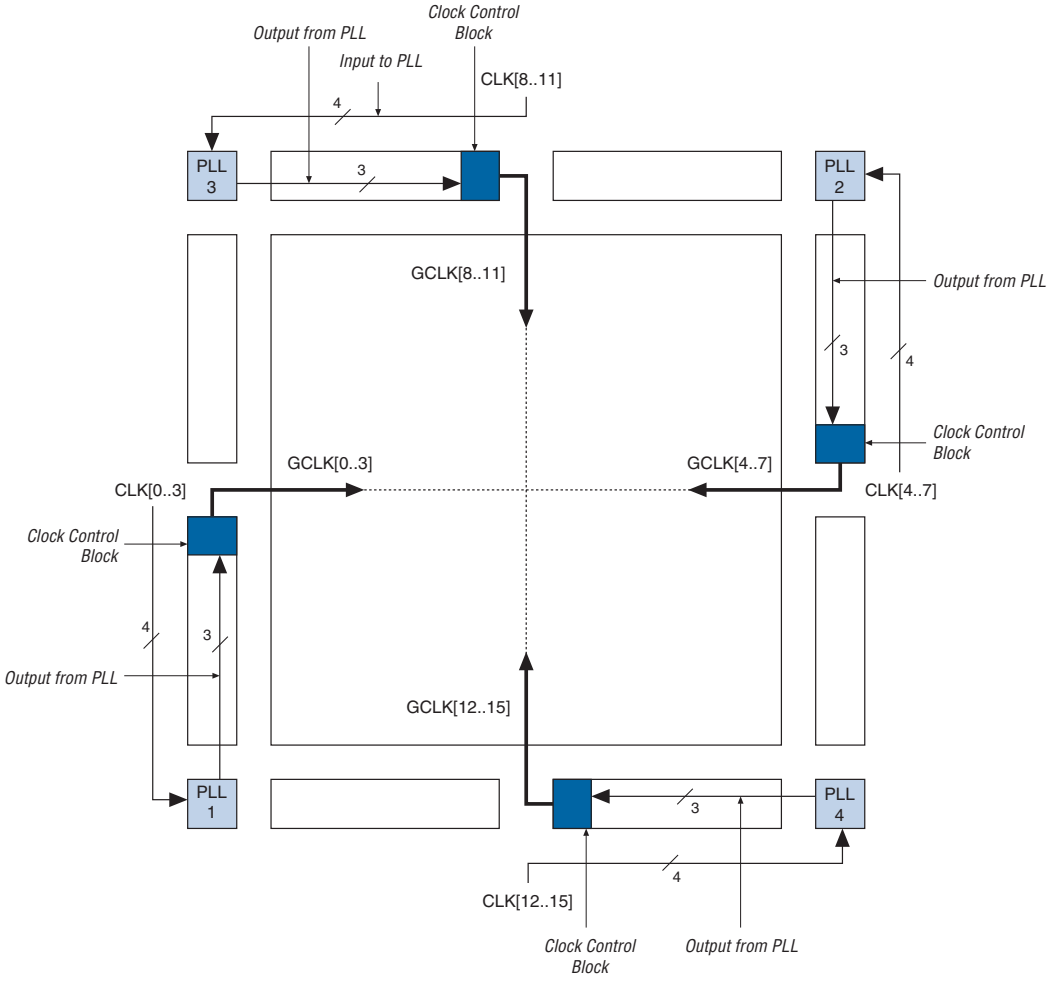
Figure 6–1 describes the ordering codes for Cyclone II devices. For more information on a specific package, contact Altera Applications.

Tables 7–4 and 7–5 describe the Cyclone II PLL input and output ports.

Table 7–4. PLL Input Signals

Port	Description	Source	Destination
inclk[1..0]	Primary and secondary clock inputs to the PLL.	Dedicated clock input pins	*n* counter
pllena	pllena is an active high signal that acts as an enable and reset signal for the PLL. It can be used for enabling or disabling each PLL. When pllena transitions low, the PLL clock output ports are driven to GND and the PLL loses lock. Once pllena transitions high again, the lock process begins and the PLL re-synchronizes to its input reference clock. The pllena port can be driven by an LE output or any general-purpose I/O pin.	Logic array or input pin	PLL control signal
areset	areset is an active high signal that resets all PLL counters to their initial values. When this signal is driven high the PLL resets its counters, clears the PLL outputs and loses lock. Once this signal is driven low again, the lock process begins and the PLL re-synchronizes to its input reference clock. The areset port can be driven by an LE output or any general-purpose I/O pin.	Logic array or input pin	PLL control signal
pfdena	pfdena is an active high signal that enables or disables the up/down output signals from the PFD. When pfdena is driven low, the PFD is disabled, while the VCO continues to operate. The PLL clock outputs continue to toggle regardless of the input clock, but may experience some long-term drift. Because the output clock frequency does not change for some time, you can use the pfdena port as a shutdown or cleanup function when a reliable input clock is no longer available. The pfdena port can be driven by an LE output or any general-purpose I/O pin.	Logic array or input pin	PFD
clkswitch	clkswitch is an active high switchover signal used to initiate manual clock switchover.	Logic array or input pin	PLL control signal

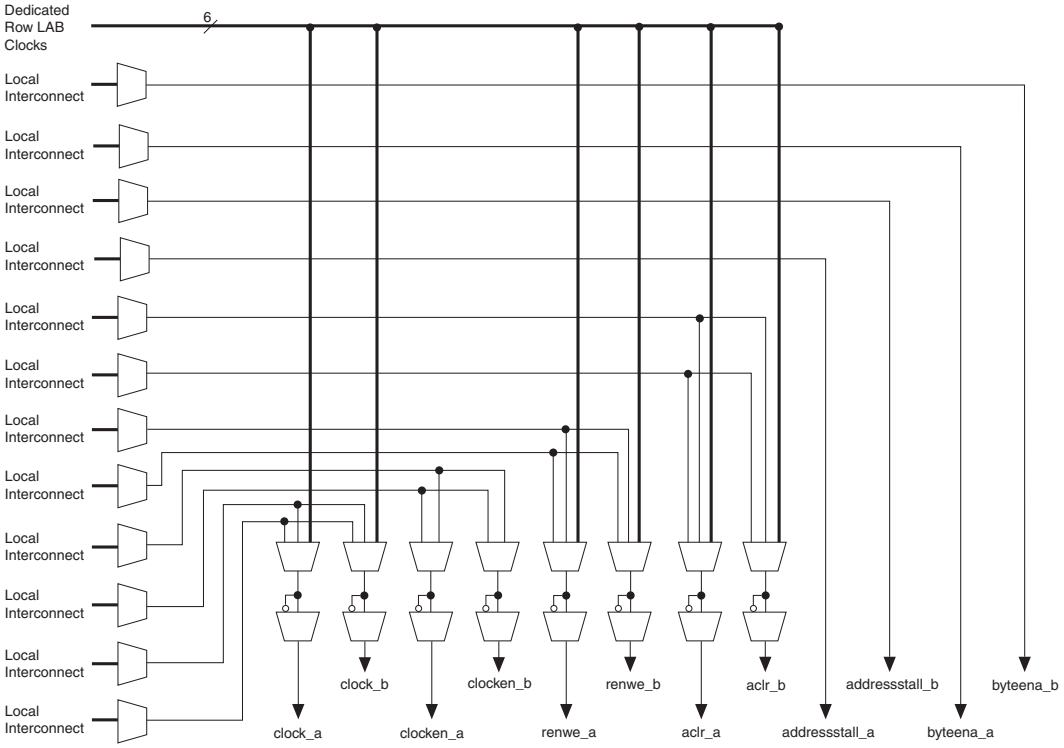
Figure 7–12. Cyclone II Clock Control Blocks Placement



The inputs to the four clock control blocks on each side are chosen from among the following clock sources:

- Four clock input pins
- Three PLL counter outputs
- Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins and two CDPCLK pins from both the top and bottom
- Four signals from internal logic

Figure 8–1. M4K Control Signal Selection



Parity Bit Support

Error detection using parity check is possible using the parity bit, with additional logic implemented in LEs to ensure data integrity. Parity-size data words can also be used for other purposes such as storing user-specified control bits.

Refer to the *Using Parity to Detect Errors White Paper* for more information.

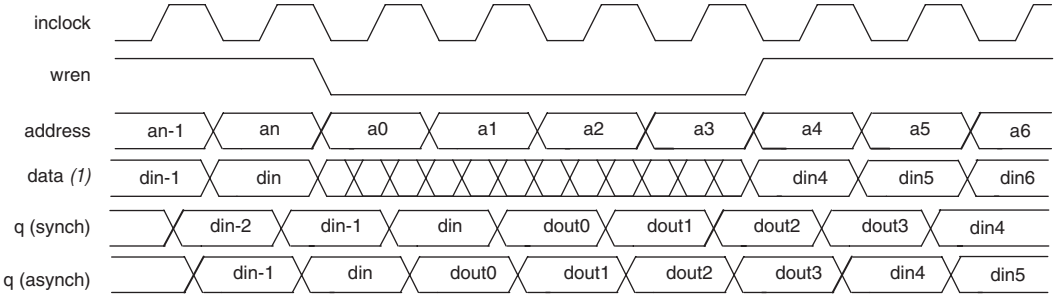
Byte Enable Support

All M4K memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable (`wren`) signals, along with the byte enable (`byteena`) signals, control the RAM block's write operations. The default value for the byte enable signals is high (enabled), in which

- 4K × 1
- 2K × 2
- 1K × 4
- 512 × 8
- 512 × 9
- 256 × 16
- 256 × 18
- 128 × 32
- 128 × 36

Figure 8–7 shows timing waveforms for read and write operations in single-port mode.

Figure 8–7. Cyclone II Single-Port Timing Waveforms

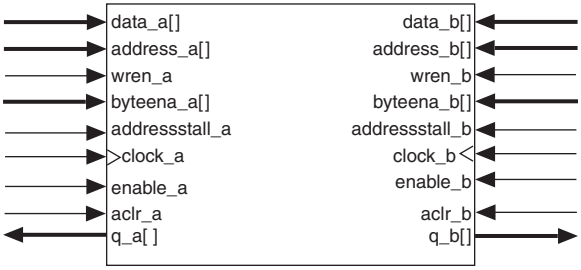


Note to Figure 8–7:
(1) The crosses in the `data` waveform during read mean "don't care."

Simple Dual-Port Mode

Simple dual-port mode supports simultaneous read and write operation. Figure 8–8 shows the simple dual-port memory configuration.

Figure 8–10. Cyclone II True Dual-Port Mode *Note (1)*



Note to Figure 8–10:
(1) True dual-port memory supports input and output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M4K blocks in true dual-port mode is 256 × 16-bit (18-bit with parity).

The 128 × 32-bit (36-bit with parity) configuration of the M4K block is unavailable because the number of output drivers is equivalent to the maximum bit width. The maximum width of the true dual-port RAM equals half of the total number of output drivers because true dual-port RAM has outputs on two ports. Table 8–6 lists the possible M4K block mixed-port width configurations.

Table 8–6. Cyclone II Memory Block Mixed-Port Width Configurations (True Dual-Port)

Read Port	Write Port						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

In true dual-port configuration, the RAM outputs are in read-during-write mode. This means that during a write operation, data being written to the A or B port of the RAM flows through to the A or B

External Memory Interface Standards

The following sections describe how to use Cyclone II device external memory interfacing features.

DDR & DDR2 SDRAM

DDR SDRAM is a memory architecture that transmits and receives data at twice the clock speed. These devices transfer data on both the rising and falling edge of the clock signal. DDR2 SDRAM is the second generation memory based on the DDR SDRAM architecture and is capable of data transfer rates of up to 533 Mbps. Cyclone II devices support DDR and DDR2 SDRAM at up to 333 Mbps.

Interface Pins

DDR and DDR2 SDRAM devices use interface pins such as data (DQ), data strobe (DQS), clock, command, and address pins to communicate with the memory controller. Data is sent and captured at twice the system clock rate by transferring data on the positive and negative edge of the clock. The commands and addresses use only one active (positive) edge of a clock.

DDR SDRAM uses single-ended data strobe DQS, while DDR2 SDRAM has the option to use differential data strobes DQS and DQS#. Cyclone II devices do not use the optional differential data strobes for DDR2 SDRAM interfaces. You can leave the DDR2 SDRAM memory DQS# pin unconnected, because only the shifted DQS signal from the clock delay control circuitry captures data. DDR and DDR2 SDRAM ×16 devices use two DQS pins, and each DQS pin is associated with eight DQ pins. However, this is not the same as the ×16/×18 mode in Cyclone II devices. You need to configure the Cyclone II devices to use two sets of pins in ×8 mode. Similarly, if your ×72 memory module uses nine DQS pins where each DQS pin is associated with eight DQ pins, configure the Cyclone II device to use nine sets of DQS/DQ groups in ×8 mode.

Connect the memory device's DQ and DQS pins to the Cyclone II DQ and DQS pins, respectively, as listed in the Cyclone II pin tables. DDR and DDR2 SDRAM also use active-high data mask (DM) pins for writes. DM pins are pre-assigned in pin outs for Cyclone II devices, and these are the preferred pins. However, you may connect the memory device's DM pins to any of the Cyclone II I/O pins in the same bank as the DQ pins of the FPGA. There is one DM pin per DQS/DQ group. If the DDR or DDR2 SDRAM device supports ECC, the design uses an extra DQS/DQ group for the ECC pins.

The DQS pins are listed in the Cyclone II pin tables as DQS[1..0]T, DQS[1..0]B, DQS[1..0]L, and DQS[1..0]R for the EP2C5 and EP2C8 devices and DQS[5..0]T, DQS[5..0]B, DQS[3..0]L, and DQS[3..0]R for the larger devices. The T denotes pins on the top of the device, the B denotes pins on the bottom of the device, the L denotes pins on the left of the device, and the R denotes pins on the right of the device. The corresponding DQ pins are marked as DQ[5..0]T[8..0], where [5..0] indicates which DQS group the pins belong to.

In the Cyclone II pinouts, the DQ groups with 9 DQ pins are also used in the ×8 mode with the corresponding DQS pins, leaving the unused DQ pin available as a regular I/O pin. The DQ groups that have 18 DQ pins are also used in the ×16 mode with the corresponding DQS pins, leaving the two unused DQ pins available as regular I/O pins. For example, DQ1T[8..0] can be used in the ×8 mode, provided it is used with DQS1T. The remaining unused DQ pin, DQ1T8, is available as a regular I/O pin.

When not used as DQ or DQS pins, these pins are available as regular I/O pins. Table 9–3 shows the number of DQS pins supported in each I/O bank in each Cyclone II device density.

Table 9–3. Available DQS Pins in Each I/O Bank & Each Device *Note (1)*

Device	Top I/O Bank	Bottom I/O Bank	Left I/O Bank	Right I/O Bank
EP2C5, EP2C8	DQS[1..0]T	DQS[1..0]B	DQS[1..0]L	DQS[1..0]R
EP2C15, EP2C20, EP2C35, EP2C50, EP2C70	DQS[5..0]B	DQS[5..0]T	DQS[3..0]L	DQS[3..0]R

Note to Table 9–3:
(1) Numbers are preliminary.

The DQ pin numbering is based on ×8/×9 mode. There are up to 8 DQS/DQ groups in ×8 mode or 4 DQS/DQ groups in ×9 mode in I/O banks for EP2C5 and EP2C8. For the larger devices, there are up to 20 DQS/DQ groups in ×8 mode or 8 DQS/DQ groups in ×9 mode. Although there are up to 20 DQS/DQ groups in the ×8 mode available in the larger Cyclone II devices, but because of the available clock resources in the Cyclone II devices, only 16 DQS/DQ groups can be utilized for the external memory interface. There is a total of 16 global clock buses available for routing DQS signals but 2 of them are needed for routing the –90° write clock and the system clock to the external memory devices. This reduces the global clock resources to 14 global clock buses for routing DQS signals. Incoming DQS signals are all routed to the clock control block, and are then routed to the global clock bus to clock the DDR LE registers. For EP2C5 and EP2C8 devices, the DQS signals are routed

Table 10–2. Cyclone II 66-MHz PCI Support (Part 2 of 2)

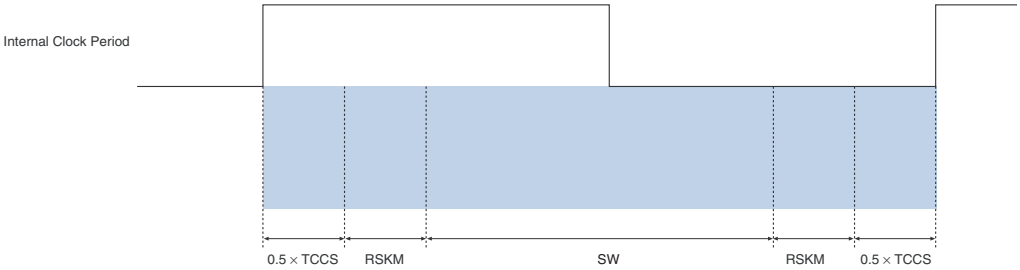
Device	Package	–6 and –7 Speed Grades	
		64 Bits	32 Bits
EP2C8	144-pin TQFP		
	208-pin PQFP		✓
	256-pin FineLine BGA		✓
EP2C15	256-pin FineLine BGA		✓
	484-pin FineLine BGA	✓	✓
EP2C20	240-pin PQFP		✓
	256-pin FineLine BGA		✓
	484-pin FineLine BGA	✓	✓
EP2C35	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C50	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C70	672-pin FineLine BGA	✓	✓
	896-pin FineLine BGA	✓	✓

Table 10–3 lists the specific Cyclone II devices that support 64-bit and 32-bit PCI at 33 MHz.

Table 10–3. Cyclone II 33-MHz PCI Support (Part 1 of 2)

Device	Package	–6, –7 and –8 Speed Grades	
		64 Bits	32 Bits
EP2C5	144-pin TQFP	—	—
	208-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
EP2C8	144-pin TQFP	—	—
	208-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
EP2C15	256-pin FineLine BGA	—	✓
	484-pin FineLine BGA	✓	✓

Figure 11–17. Cyclone II High-Speed I/O Timing Budget *Note (1)*



Note to Figure 11–17:
(1) The equation for the high-speed I/O timing budget is: Period = 0.5/TCCS + RSKM + SW + RSKM + 0.5/TCCS.

Design Guidelines

This section provides guidelines for designing with Cyclone II devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pins in relation to differential pads.

See the guidelines in the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook* for placing single-ended pads with respect to differential pads in Cyclone II devices.

Board Design Considerations

This section explains how to get the optimal performance from the Cyclone II I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. The critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques must be considered to get the best performance from the IC. The Cyclone II device generates signals that travel over the media at frequencies as high as 805 Mbps. Use the following general guidelines for improved signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.

See the *Cyclone II Memory Blocks* chapter in Volume 1 of the ***Cyclone II Device Handbook*** for more information on Cyclone II M4K memory blocks.

Refer to *AN 306: Techniques for Implementing Multipliers in FPGA Devices* for more information on soft multipliers.

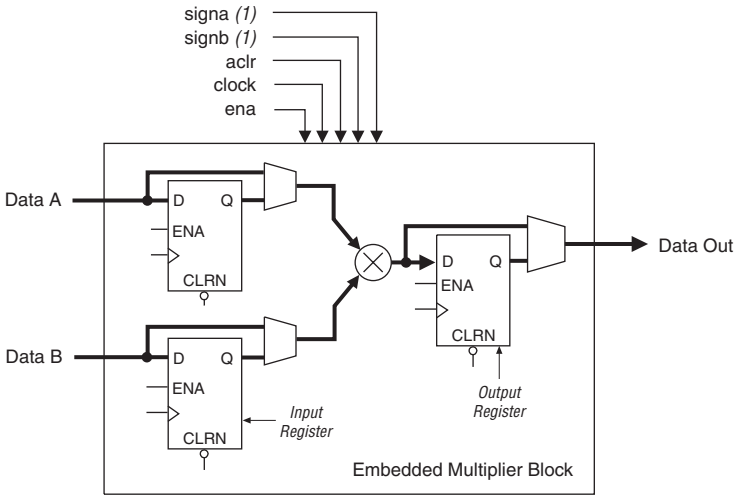
Architecture

Each embedded multiplier consists of the following elements:

- Multiplier stage
- Input and output registers
- Input and output interfaces

Figure 12–2 shows the multiplier block architecture.

Figure 12–2. Multiplier Block Architecture



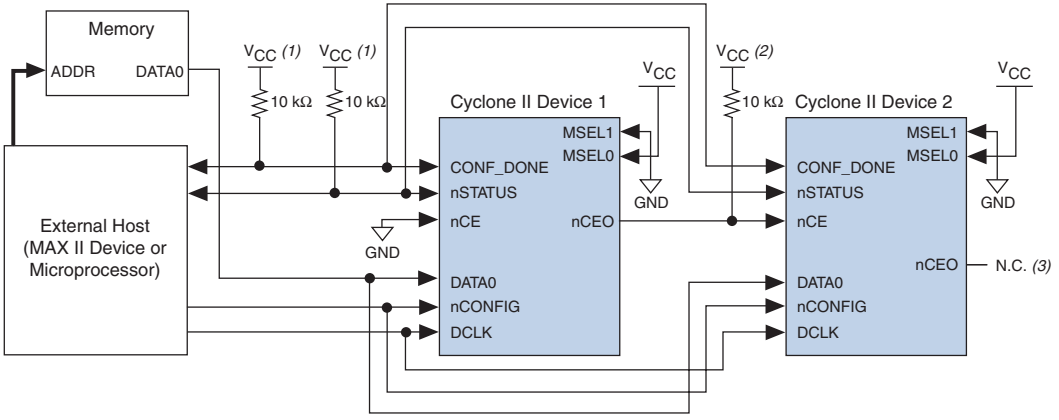
Note to Figure 12–2:

(1) If necessary, you can send these signals through one register to match the data signal path.

Input Registers

You can send each multiplier input signal into an input register or directly into the multiplier in 9- or 18-bit sections depending on the operational mode of the multiplier. You can send each multiplier input signal through a register independently of each other (e.g., you can send the multiplier's

Figure 13–10. Multiple Device PS Configuration Using an External Host



Notes to Figure 13–10:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the devices and the external host.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

In multiple device PS configuration, connect the first Cyclone II device's nCE pin to GND and connect the nCEO pin to the nCE pin of the next Cyclone II device in the chain. Use an external 10-kΩ pull-up resistor to pull the Cyclone II device's nCEO pin high to its V_{CCIO} level to help the internal weak pull-up resistor when the nCEO pin feeds next Cyclone II device's nCE pin. The input to the nCE pin of the last Cyclone II device in the chain comes from the previous Cyclone II device. After the first device completes configuration in a multiple device configuration chain, its nCEO pin transitions low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle. Therefore, the MAX II device begins to transfer data to the next Cyclone II device without interruption. The nCEO pin is a dual-purpose pin in Cyclone II devices. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in chain is a Cyclone II device.

The Quartus II software sets the Cyclone II device nCEO pin as a dedicated output by default. If the nCEO pin feeds the next device's nCE pin, you must make sure that the nCEO pin is not used as a user I/O after configuration. This software setting is in the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box in Quartus II software.

For more information on how to use the USB-Blaster, MasterBlaster, ByteBlaster II or ByteBlasterMV cables, refer to the following documents:

- *USB-Blaster USB Port Download Cable Data Sheet*
- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlaster II Parallel Port Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*

JTAG Configuration

The Joint Test Action Group (JTAG) has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture allows you to test components on PCBs with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. The JTAG circuitry can also be used to shift configuration data into the device. The Quartus II software automatically generates SOF files that can be used for JTAG configuration with a download cable in the Quartus II programmer.

For more information on JTAG boundary-scan testing, see the following documents:

- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone II Devices* chapter in Volume 2 of the *Cyclone II Device Handbook*
- Jam Programming & Testing Language Specification

Cyclone II devices are designed such that JTAG instructions have precedence over any device configuration modes. This means that JTAG configuration can take place without waiting for other configuration modes to complete. For example, if you attempt JTAG configuration of Cyclone II devices during PS configuration, PS configuration terminates and JTAG configuration begins. If the Cyclone II `MSEL` pins are set to AS or fast AS mode, the Cyclone II device does not output a `DCLK` signal when JTAG configuration takes place.

You cannot use the Cyclone II decompression feature if you are configuring your Cyclone II device when using JTAG-based configuration.