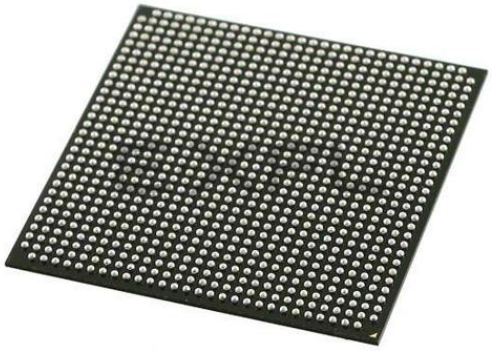

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 4276 |
| Number of Logic Elements/Cells | 68416 |
| Total RAM Bits | 1152000 |
| Number of I/O | 622 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 896-BGA |
| Supplier Device Package | 896-FBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2c70f896c6 |

There are five dynamic control input signals that feed the embedded multiplier: `signa`, `signb`, `clk`, `clkena`, and `aclr`. `signa` and `signb` can be registered to match the data signal input path. The same `clk`, `clkena`, and `aclr` signals feed all registers within a single embedded multiplier.

For more information on Cyclone II embedded multipliers, see the *Embedded Multipliers in Cyclone II Devices* chapter.

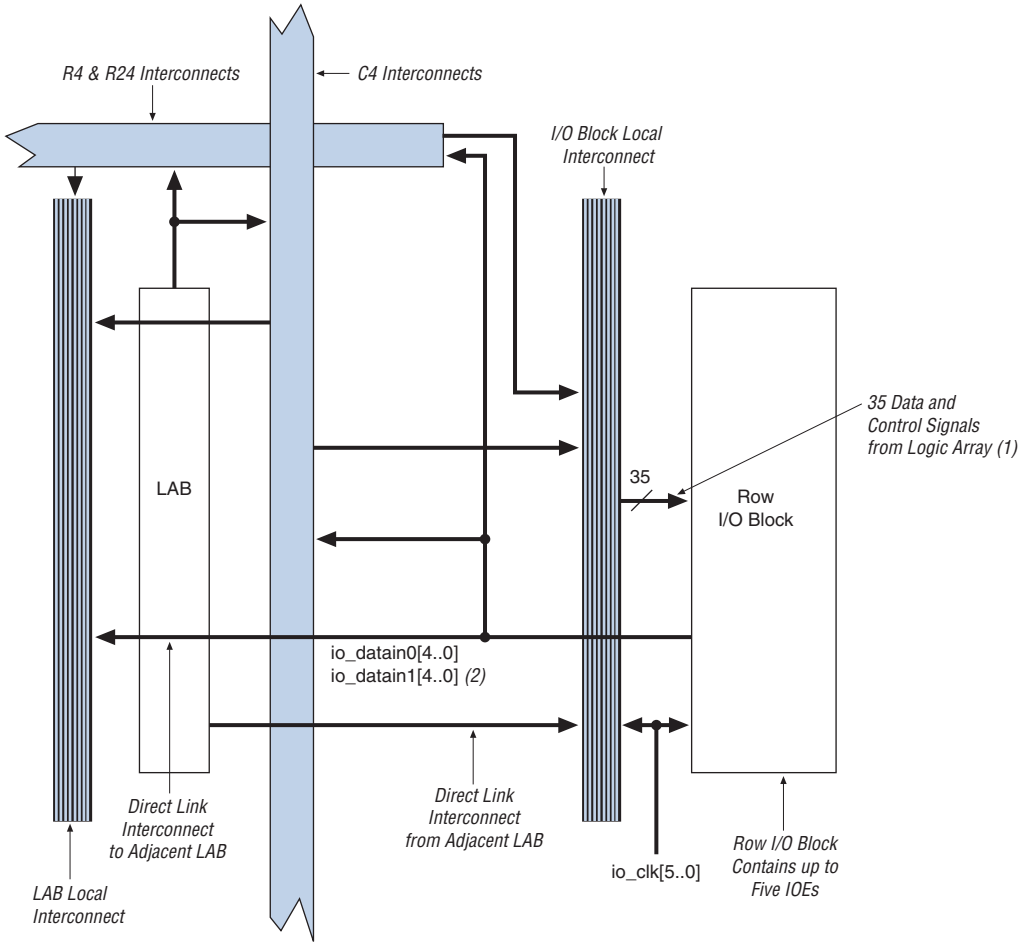
## I/O Structure & Features

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- $V_{REF}$ pins

Cyclone II device IOEs contain a bidirectional I/O buffer and three registers for complete embedded bidirectional single data rate transfer. Figure 2–20 shows the Cyclone II IOE structure. The IOE contains one input register, one output register, and one output enable register. You can use the input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. You can use IOEs as input, output, or bidirectional pins.

*Figure 2–21. Row I/O Block Connection to the Interconnect*

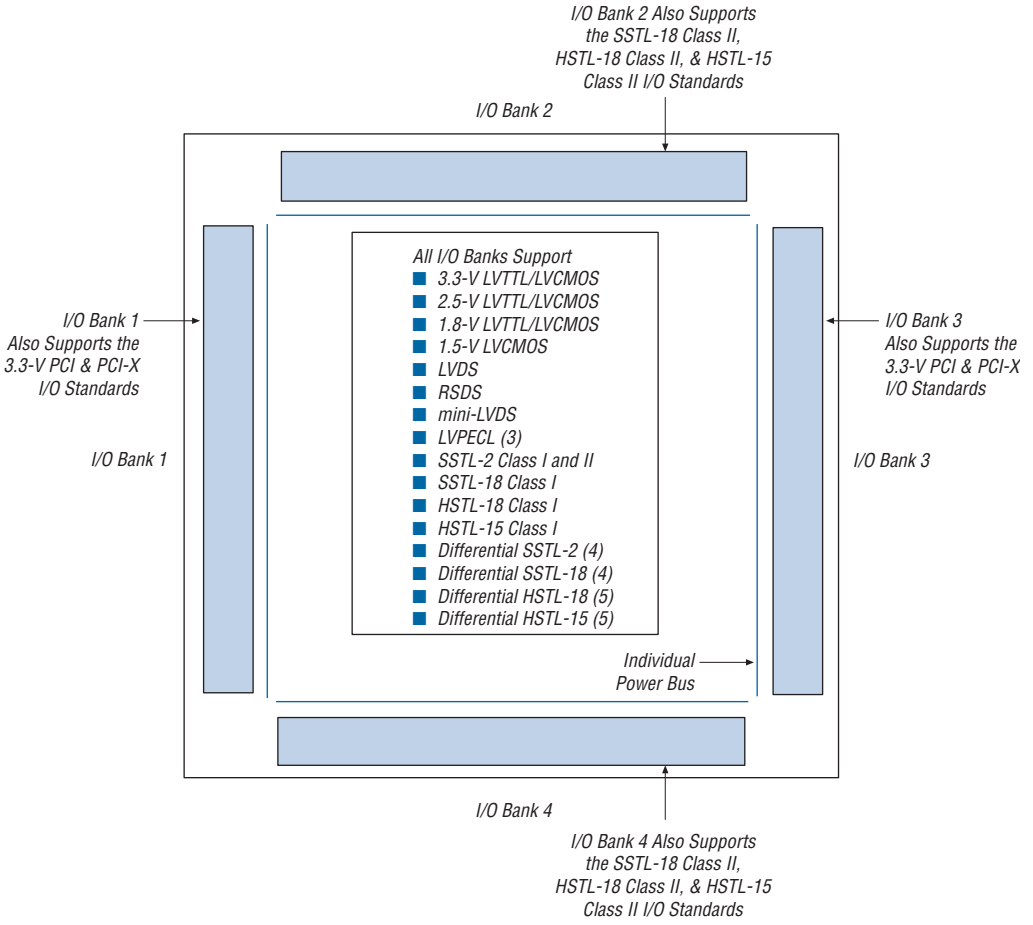



*Notes to Figure 2–21:*

(1) The 35 data and control signals consist of five data out lines, `io_dataout[4..0]`, five output enables, `io_coe[4..0]`, five input clock enables, `io_cce_in[4..0]`, five output clock enables, `io_cce_out[4..0]`, five clocks, `io_cclk[4..0]`, five asynchronous clear signals, `io_caclr[4..0]`, and five synchronous clear signals, `io_csclr[4..0]`.

(2) Each of the five IOEs in the row I/O block can have two `io_datain` (combinational or registered) inputs.

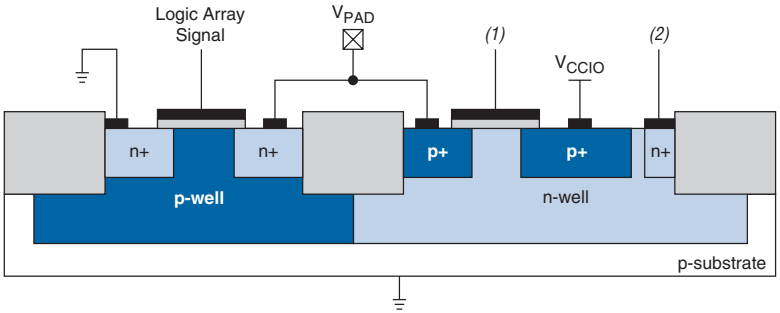
*Figure 2–28. EP2C5 & EP2C8 I/O Banks* *Notes (1), (2)*




*Notes to Figure 2–28:*

(1) This is a top view of the silicon die.
(2) This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.
(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
(4) The differential SSTL-18 and SSTL-2 I/O standards are only supported on clock input pins and PLL output clock pins.
(5) The differential 1.8-V and 1.5-V HSTL I/O standards are only supported on clock input pins and PLL output clock pins.

*Figure 4–2. Transistor Level Diagram of FPGA Device I/O Buffers*




*Notes to Figure 4–2:*
(1) This is the logic array signal or the larger of either the $V_{CCIO}$ or $V_{PAD}$ signal.
(2) This is the larger of either the $V_{CCIO}$ or $V_{PAD}$ signal.

## Power-On Reset Circuitry

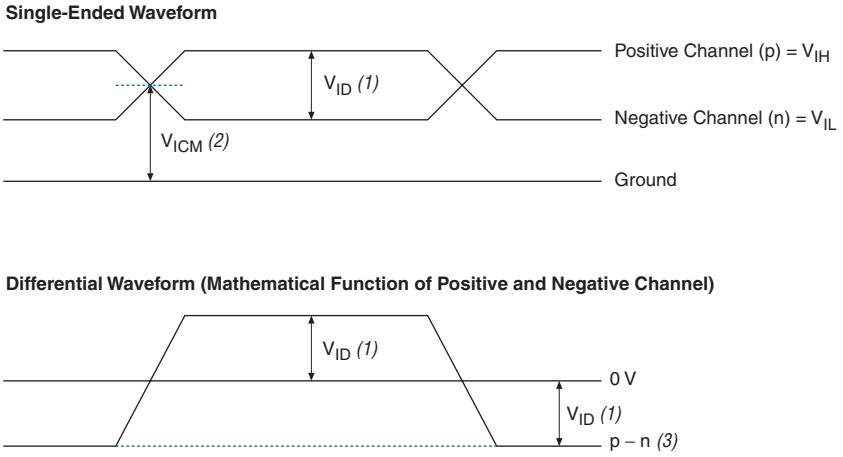
Cyclone II devices contain POR circuitry to keep the device in a reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the $V_{CCINT}$ voltage levels and tri-states all user I/O pins until the $V_{CC}$ reaches the recommended operating levels. In addition, the POR circuitry also monitors the $V_{CCIO}$ level of the two I/O banks that contains configuration pins (I/O banks 1 and 3 for EP2C5 and EP2C8, I/O banks 2 and 6 for EP2C15A, EP2C20, EP2C35, EP2C50, and EP2C70) and tri-states all user I/O pins until the $V_{CC}$ reaches the recommended operating levels.

After the Cyclone II device enters user mode, the POR circuit continues to monitor the $V_{CCINT}$ voltage level so that a brown-out condition during user mode can be detected. If the $V_{CCINT}$ voltage sags below the POR trip point during user mode, the POR circuit resets the device. If the $V_{CCIO}$ voltage sags during user mode, the POR circuit does not reset the device.

### "Wake-up" Time for Cyclone II Devices

In some applications, it may be necessary for a device to wake up very quickly in order to begin operation. The Cyclone II device family offers the Fast-On feature to support fast wake-up time applications. Devices that support the Fast-On feature are designated with an "A" in the ordering code and have stricter power up requirements compared to non-A devices.

*Figure 5–1. Receiver Input Waveforms for Differential I/O Standards*




*Notes to Figure 5–1:*

(1) $V_{ID}$ is the differential input voltage. $V_{ID} = |p - n|$.

(2) $V_{ICM}$ is the input common mode voltage. $V_{ICM} = (p + n)/2$.

(3) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

Table 5–11 specifies the bus hold parameters for general I/O pins.

*Table 5–11. Bus Hold Parameters* *Note (1)*

| Parameter | Conditions | $V_{CCIO}$ Level | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | 1.8 V | | 2.5 V | | 3.3 V | | |
| | | Min | Max | Min | Max | Min | Max | |
| Bus-hold low, sustaining current | $V_{IN} > V_{IL}$(maximum) | 30 | — | 50 | — | 70 | — | µA |
| Bus-hold high, sustaining current | $V_{IN} < V_{IL}$(minimum) | –30 | — | –50 | — | –70 | — | µA |
| Bus-hold low, overdrive current | $0 V < V_{IN} < V_{CCIO}$ | — | 200 | — | 300 | — | 500 | µA |
| Bus-hold high, overdrive current | $0 V < V_{IN} < V_{CCIO}$ | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point *(2)* | — | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2.0 | V |

*Notes to Table 5–11:*
(1) There is no specification for bus-hold at $V_{CCIO}$ = 1.5 V for the HSTL I/O standard.
(2) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

## On-Chip Termination Specifications

Table 5–12 defines the specifications for internal termination resistance tolerance when using series or differential on-chip termination.

*Table 5–12. Series On-Chip Termination Specifications*

| Symbol | Description | Conditions | Resistance Tolerance | | | |
|---|---|---|---|---|---|---|
| | | | Commercial Max | Industrial Max | Extended/ Automotive Temp Max | Unit |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.3V | ±30 | ±30 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 2.5V | ±30 | ±30 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8V | ±30 *(1)* | ±40 | ±50 | % |

*Note to Table 5–12:*
(1) For commercial –8 devices, the tolerance is ±40%.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

*Table 5–14. Cyclone II Device Timing Model Status*

| Device | Speed Grade | Preliminary | Final |
|---|---|---|---|
| EP2C5/A | Commercial/Industrial | — | ✓ |
| | Automotive | ✓ | — |
| EP2C8/A | Commercial/Industrial | — | ✓ |
| | Automotive | ✓ | — |
| EP2C15A | Commercial/Industrial | — | ✓ |
| | Automotive | ✓ | — |
| EP2C20/A | Commercial/Industrial | — | ✓ |
| | Automotive | ✓ | — |
| EP2C35 | Commercial/Industrial | — | ✓ |
| EP2C50 | Commercial/Industrial | — | ✓ |
| EP2C70 | Commercial/Industrial | — | ✓ |

## Performance

Table 5–15 shows Cyclone II performance for some common designs. All performance values were obtained with Quartus II software compilation of LPM, or MegaCore functions for the FIR and FFT designs.

*Table 5–15. Cyclone II Performance (Part 1 of 4)*

| Applications | | Resources Used | | | Performance (MHz) | | | |
|---|---|---|---|---|---|---|---|---|
| | | LEs | M4K Memory Blocks | DSP Blocks | –6 Speed Grade | –7 Speed Grade *(6)* | –7 Speed Grade *(7)* | –8 Speed Grade |
| LE | 16-to-1 multiplexer *(1)* | 21 | 0 | 0 | 385.35 | 313.97 | 270.85 | 286.04 |
| | 32-to-1 multiplexer *(1)* | 38 | 0 | 0 | 294.2 | 260.75 | 228.78 | 191.02 |
| | 16-bit counter | 16 | 0 | 0 | 401.6 | 349.4 | 310.65 | 310.65 |
| | 64-bit counter | 64 | 0 | 0 | 157.15 | 137.98 | 126.08 | 126.27 |

*Table 5–15. Cyclone II Performance (Part 2 of 4)*

| Applications | | Resources Used | | | Performance (MHz) | | | |
|---|---|---|---|---|---|---|---|---|
| | | LEs | M4K Memory Blocks | DSP Blocks | –6 Speed Grade | –7 Speed Grade *(6)* | –7 Speed Grade *(7)* | –8 Speed Grade |
| Memory M4K block | Simple dual-port RAM 128 × 36 bit *(3)*, *(5)* | 0 | 1 | 0 | 235.29 | 194.93 | 163.13 | 163.13 |
| | True dual-port RAM 128 × 18 bit *(3)*, *(5)* | 0 | 1 | 0 | 235.29 | 194.93 | 163.13 | 163.13 |
| | FIFO 128 × 16 bit *(5)* | 32 | 1 | 0 | 235.29 | 194.93 | 163.13 | 163.13 |
| | Simple dual-port RAM 128 × 36 bit *(4)*,*(5)* | 0 | 1 | 0 | 210.08 | 195.0 | 163.02 | 163.02 |
| | True dual-port RAM 128x18 bit *(4)*,*(5)* | 0 | 1 | 0 | 163.02 | 163.02 | 163.02 | 163.02 |
| DSP block | 9 × 9-bit multiplier *(2)* | 0 | 0 | 1 | 260.01 | 216.73 | 180.57 | 180.57 |
| | 18 × 18-bit multiplier *(2)* | 0 | 0 | 1 | 260.01 | 216.73 | 180.57 | 180.57 |
| | 18-bit, 4 tap FIR filter | 113 | 0 | 8 | 182.74 | 147.47 | 127.74 | 122.98 |
| Larger Designs | 8-bit, 16 tap parallel FIR filter | 52 | 0 | 4 | 153.56 | 131.25 | 110.44 | 110.57 |
| | 8-bit, 1024 pt, Streaming, 3 Mults/5 Adders FFT function | 3191 | 22 | 9 | 235.07 | 195.0 | 147.51 | 163.02 |
| | 8-bit, 1024 pt, Streaming, 4 Mults/2 Adders FFT function | 3041 | 22 | 12 | 235.07 | 195.0 | 146.3 | 163.02 |
| | 8-bit, 1024 pt, Single Output, 1 Parallel FFT Engine, Burst, 3 Mults/5 Adders FFT function | 1056 | 5 | 3 | 235.07 | 195.0 | 147.84 | 163.02 |
| | 8-bit, 1024 pt, Single Output, 1 Parallel FFT Engine, Burst, 4 Mults/2 Adders FFT function | 1006 | 5 | 4 | 235.07 | 195.0 | 149.99 | 163.02 |
| | 8-bit, 1024 pt, Single Output, 2 Parallel FFT Engines, Burst, 3 Mults/5 Adders FFT function | 1857 | 10 | 6 | 200.0 | 195.0 | 149.61 | 163.02 |
| | 8-bit, 1024 pt, Single Output, 2 Parallel FFT Engines, Burst, 4 Mults/2 Adders FFT function | 1757 | 10 | 8 | 200.0 | 195.0 | 149.34 | 163.02 |
| | 8-bit, 1024 pt, Quad Output, 1 Parallel FFT Engine, Burst, 3 Mults/5 Adders FFT function | 2550 | 10 | 9 | 235.07 | 195.0 | 148.21 | 163.02 |

*Table 5–56. Maximum DCD for SDR Output on Column I/O* Notes (1), (2) *(Part 2 of 2)*

| Column I/O Output Standard | C6 | C7 | C8 | Unit |
|---|---|---|---|---|
| 2.5-V | 140 | 140 | 155 | ps |
| 1.8-V | 115 | 115 | 165 | ps |
| 1.5-V | 745 | 745 | 770 | ps |
| SSTL-2 Class I | 60 | 60 | 75 | ps |
| SSTL-2 Class II | 60 | 60 | 80 | ps |
| SSTL-18 Class I | 60 | 130 | 130 | ps |
| SSTL-18 Class II | 60 | 135 | 135 | ps |
| HSTL-18 Class I | 60 | 115 | 115 | ps |
| HSTL-18 Class II | 75 | 75 | 100 | ps |
| HSTL-15 Class I | 150 | 150 | 150 | ps |
| HSTL-15 Class II | 135 | 135 | 155 | ps |
| Differential SSTL-2 Class I | 60 | 60 | 75 | ps |
| Differential SSTL-2 Class II | 60 | 60 | 80 | ps |
| Differential SSTL-18 Class I | 60 | 130 | 130 | ps |
| Differential SSTL-18 Class II | 60 | 135 | 135 | ps |
| Differential HSTL-18 Class I | 60 | 115 | 115 | ps |
| Differential HSTL-18 Class II | 75 | 75 | 100 | ps |
| Differential HSTL-15 Class I | 150 | 150 | 150 | ps |
| Differential HSTL-15 Class II | 135 | 135 | 155 | ps |
| LVDS | 60 | 60 | 60 | ps |
| Simple RSDS | 60 | 70 | 70 | ps |
| Mini-LVDS | 60 | 60 | 60 | ps |

*Notes to Table 5–56:*

(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.

(2) Numbers are applicable for commercial, industrial, and automotive devices.

*Table 5–57. Maximum for DDIO Output on Row Pins with PLL in the Clock Path* Notes (1), (2) *(Part 1 of 2)*

| Row Pins with PLL in the Clock Path | C6 | C7 | C8 | Unit |
|---|---|---|---|---|
| LVCMOS | 270 | 310 | 310 | ps |
| LVTTL | 285 | 305 | 335 | ps |
| 2.5-V | 180 | 180 | 220 | ps |
| 1.8-V | 165 | 175 | 205 | ps |

DQS pin to the DQ LE register does not necessarily match the delay from the DQ pin to the DQ LE register. Therefore, you must adjust the clock delay control circuitry to compensate for this difference in delays.

## DQS Postamble

For external memory interfaces that use a bidirectional read strobe, such as DDR and DDR2 SDRAM, the DQS signal is low before going to or coming from the high-impedance state (see Figure 9–1). The state where DQS is low just after high-impedance is called the preamble and the state where DQS is low just before it goes to high-impedance is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR and DDR2 SDRAM. If the Cyclone II device or the DDR/DDR2 SDRAM device does not drive the DQ and DQS pins, the signals go to a high-impedance state. Because a pull-up resistor terminates both DQ and DQS to $V_{TT}$ (1.25 V for SSTL-2 and 0.9 V for SSTL-18), the effective voltage on the high-impedance line is either 1.25 V or 0.9 V. According to the JEDEC JESD8-9 specification for SSTL-2 I/O standard and the JESD8-15A specification for SSTL-18 I/O standard, this is an indeterminate logic level, and the input buffer can interpret this as either a logic high or logic low. If there is any noise on the DQS line, the input buffer may interpret that noise as actual strobe edges.

Cyclone II devices have non-dedicated logic that can be configured to prevent a false edge trigger at the end of the DQS postamble. Each Cyclone II DQS signal is connected to postamble logic that consists of a D flip flop (see Figure 9–9). This register is clocked by the shifted DQS signal. Its input is connected to ground. The controller needs to include extra logic to tell the reset signal to release the preset signal on the falling DQS edge at the start of the postamble. This disables any glitches that happen right after the postamble. This postamble logic is automatically implemented by the Altera MegaCore DDR/DDR2 SDRAM Controller in the LE register as part of the open-source datapath.

- Cyclone II FPGA (EP2C15 or larger)
- Altera PCI Express Compiler ×1 MegaCore® function
- External PCI Express transceiver/PHY

## 2.5-V LVTTL (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVTTL.

## 2.5-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVCMOS.

## SSTL-2 Class I and II (EIA/JEDEC Standard JESD8-9A)

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operations in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of $-0.3\ V \leq V_I \leq V_{CCIO} + 0.3\ V$. SSTL-2 requires a $V_{REF}$ value of 1.25 V and a $V_{TT}$ value of 1.25 V connected to the termination resistors (refer to Figures 10–1 and 10–2).

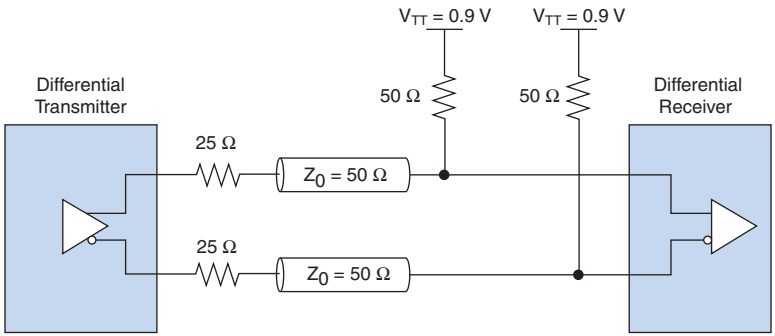
## Pseudo-Differential SSTL-18 Class I and Differential SSTL-18 Class II

The 1.8-V differential SSTL-18 standard is formulated under JEDEC Standard, JESD8-15: Stub Series Terminated Logic for 1.8V (SSTL-18).

The differential SSTL-18 I/O standard is a 1.8-V standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard supports differential signals in systems using the SSTL-18 standard and supplements the SSTL-18 standard for differential clocks. Refer to Figures 10–9 and 10–10 for details on differential SSTL-18 termination.

Cyclone II devices do not support true differential SSTL-18 standards. Cyclone II devices support pseudo-differential SSTL-18 outputs for `PLL_OUT` pins and pseudo-differential SSTL-18 inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential SSTL.

*Figure 10–9. Differential SSTL-18 Class I Termination*



transistor-to-transistor logic (TTL), and positive (or pseudo) emitter coupled logic (PECL). This low EMI makes LVDS ideal for applications with low EMI requirements or noise immunity requirements. The LVDS standard does not require an input reference voltage. However, it does require a termination resistor of 90 to 110 Ωbetween the two signals at the input buffer. Cyclone II devices support true differential LVDS inputs and outputs.

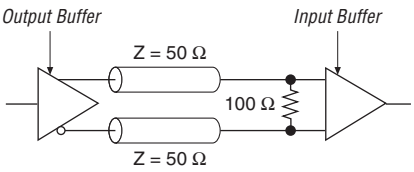
LVDS outputs on Cyclone II need external resistor network to work properly. Refer to the *High Speed Differential Interfaces in Cyclone II Devices* chapter in volume 1 of the *Cyclone II Device Handbook* for more information.

For reduced swing differential signaling (RSDS), $V_{OD}$ ranges from 100 to 600 mV. For mini-LVDS, $V_{OD}$ ranges from 300 to 600 mV. The differential termination resistor value ranges from 95 to 105 Ωfor both RSDS and mini-LVDS. Cyclone II devices support RSDS/mini-LVDS outputs only.

## Differential LVPECL

The low voltage positive (or pseudo) emitter coupled logic (LVPECL) standard is a differential interface standard recommending $V_{CCIO}$ of 3.3 V. The LVPECL standard also supports $V_{CCIO}$ of 2.5 V, 1.8 V and 1.5 V. The standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply and is similar to LVDS. However, LVPECL has a larger differential output voltage swing than LVDS. The LVPECL standard does not require an input reference voltage, but it does require an external 100-Ωtermination resistor between the two signals at the input buffer. Figures 10–17 and 10–18 show two alternate termination schemes for LVPECL. LVPECL input standard is supported at the clock input pins on Cyclone II devices. LVPECL output standard is not supported.

***Figure 10–17. LVPECL DC Coupled Termination***



device also pulls nSTATUS and CONF_DONE low and tri-states all I/O pins. Once the nCONFIG pin returns to a logic high level and the Cyclone II device releases the nSTATUS pin, the MAX II device can begin reconfiguration.

### *Error During Configuration*

If an error occurs during configuration, the Cyclone II device transitions its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin tells the MAX II device that there is an error. If you turn on the **Auto-restart configuration after error** option in the Quartus II software, the Cyclone II device releases nSTATUS after a reset time-out period (maximum of 40 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 µs) on nCONFIG to restart the configuration process.

The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The MAX II device must monitor the Cyclone II device's CONF_DONE pin to detect errors and determine when programming completes. If all configuration data is sent, but CONF_DONE or INIT_DONE do not transition high, the MAX II device must reconfigure the target device.

For more information on configuration issues, see the *Debugging Configuration Problems* chapter of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site (**www.altera.com**).

## Multiple Device PS Configuration Using a MAX II Device as an External Host

Figure 13–10 shows how to configure multiple devices using a MAX II device. This circuit is similar to the PS configuration circuit for a single device, except Cyclone II devices are cascaded for multiple device configuration.

Upon power-up, the Cyclone II device goes through a POR. During POR, the device reset, holds nSTATUS and CONF_DONE low, and tri-states all user I/O pins. After POR, which typically lasts 100 ms, the Cyclone II FPGA releases nSTATUS and enters configuration mode when this signal is pulled high by the external 10-kΩ resistor. Once the FPGA successfully exits POR, all user I/O pins continue to be tri-stated. Cyclone II devices have weak pull-up resistors on the user I/O pins which are on before and during configuration.

The configuration device also goes through a POR delay to allow the power supply to stabilize. The maximum POR time for EPC2 or EPC1 devices is 200 ms. The POR time for enhanced configuration devices can be set to 100 ms or 2 ms, depending on the enhanced configuration device's PORSEL pin setting. If the PORSEL pin is connected to ground, the POR delay is 100 ms. If the PORSEL pin is connected to $V_{CC}$, the POR delay is 2 ms. You must power the Cyclone II device before or during the enhanced configuration device POR time. During POR, the configuration device transitions its OE pin low. This low signal delays configuration because the OE pin is connected to the target device's nSTATUS pin. When the target and configuration devices complete POR, they both release the nSTATUS to OE line, which is then pulled high by a pull-up resistor.

When the power supplies have reached the appropriate operating voltages, the target FPGA senses the low-to-high transition on nCONFIG and initiates the configuration cycle. The configuration cycle consists of three stages: reset, configuration, and initialization.

The Cyclone II device does not have a PORSEL pin.

### *Reset Stage*

While nCONFIG or nSTATUS is low, the device is in reset. You can delay configuration by holding the nCONFIG or nSTATUS pin low.

$V_{CCINT}$ and $V_{CCIO}$ of the banks where the configuration and JTAG pins reside need to be fully powered to the appropriate voltage levels in order to begin the configuration process.

When the nCONFIG signal goes high, the device comes out of reset and releases the nSTATUS pin, which is pulled high by a pull-up resistor. Enhanced configuration and EPC2 devices have an optional internal pull-up resistor on the OE pin. You can turn on this option in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If this internal pull-up resistor is not used, you need to connect an external 10-kΩ pull-up resistor to the OE and nSTATUS line. Once nSTATUS is released, the FPGA is ready to receive configuration data and the configuration stage begins.

devices and to the slave configuration devices. Connect the first configuration device's nCS pin to all the Cyclone II device's CONF_DONE pins, and connect the nCASC pin to the nCS pin of the next configuration device in the chain. Leave the nCASC pin of the last configuration device floating. When the master configuration device sends all the data to the Cyclone II device, the configuration device transitions the nCASC pin low, which drives nCS on the next configuration device. Because a configuration device requires less than one clock cycle to activate a subsequent configuration device, the data stream is uninterrupted.

Enhanced configuration devices (EPC16, EPC8, and EPC4 devices) cannot be cascaded.

Since all nSTATUS and CONF_DONE pins are connected, if any device detects an error, the master configuration device stops configuration for the entire chain and the entire chain must be reconfigured. For example, if the master configuration device does not detect the Cyclone II device's CONF_DONE pin transitioning high at the end of configuration, it resets the entire chain by transitioning its OE pin low. This low signal drives the OE pin low on the slave configuration device(s) and drives nSTATUS low on all Cyclone II devices, causing them to enter a reset state. This behavior is similar to the FPGA detecting an error in the configuration data.

Figure 13–17 shows how to configure multiple devices using cascaded EPC2 or EPC1 devices.

## Combining JTAG & Active Serial Configuration Schemes

You can combine the AS configuration scheme with JTAG-based configuration. Set the MSEL[1..0] pins to 00 (AS mode) or 10 (Fast AS mode)in this setup, which uses two 10-pin download cable headers on the board. The first header programs the serial configuration device in the system via the AS programming interface, and the second header configures the Cyclone II directly via the JTAG interface.

If you try configuring the device using both schemes simultaneously, JTAG configuration takes precedence and AS configuration is terminated.

When a blank serial configuration device is attached to Cyclone II device, turn on the **Halt on-chip configuration controller** option under the Tools menu by clicking **Options**. The Options dialog box appears. In the **Category** list, select **Programmer** before starting the JTAG configuration with the Quartus II programmer. This option stops the AS reconfiguration loop from a blank serial configuration device before starting the JTAG configuration. This includes using the Serial Flash Loader IP because JTAG is used for configuring the Cyclone II device. Users do not need to recompile their Quartus II designs after turning on this Option.

## Programming Serial Configuration Devices In-System Using the JTAG Interface

Cyclone II devices in a single device chain or in a multiple device chain support in-system programming of a serial configuration device using the JTAG interface via the serial flash loader design. The board's intelligent host or download cable can use the four JTAG pins on the Cyclone II device to program the serial configuration device in system, even if the host or download cable cannot access the configuration device's configuration pins (DCLK, DATA, ASDI, and nCS pins).

The serial flash loader design is a JTAG-based in-system programming solution for Altera serial configuration devices. The serial flash loader is a bridge design for the FPGA that uses its JTAG interface to access the EPCS JIC (JTAG Indirect Configuration Device Programming) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the serial flash loader design.

In a multiple device chain, you only need to configure the master Cyclone II device which is controlling the serial configuration device. The slave devices in the multiple device chain which are configured by the serial configuration device do not need to be configured when using this

*Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 4 of 5)*

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| nCEO | N/A if option is on. I/O if option is off. | All | Output | This pin is an output that drives low when device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multiple device configuration, this pin inputs the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration.<br><br>If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the $V_{CCIO}$ voltage of its I/O bank to help the internal weak pull-up resistor.<br><br>Use the Quartus II software to make this pin a user I/O pin. |
| ASDO | N/A in AS mode I/O in PS and JTAG mode | AS | Output | This pin sends a control signal from the Cyclone II device to the serial configuration device in AS mode and is used to read out configuration data.<br><br>In AS mode, ASDO has an internal pull-up that is always active. |
| nCSO | N/A in AS mode I/O in PS and JTAG mode | AS | Output | This pin sends an output control signal from the Cyclone II device to the serial configuration device in AS mode that enables the configuration device.<br><br>In AS mode, nCSO has an internal pull-up resistor that is always active. |

# Thermal Resistance

Thermal resistance values for Cyclone II devices are provided for a board meeting JEDEC specifications and for a typical board. The values provided are as follows:

- $\theta_{JA}$ (°C/W) Still Air—Junction-to-ambient thermal resistance with no airflow when a heat sink is not being used.
- $\theta_{JA}$ (°C/W) 100 ft./minute—Junction-to-ambient thermal resistance with 100 ft./minute airflow when a heat sink is not being used.
- $\theta_{JA}$ (°C/W) 200 ft./minute—Junction-to-ambient thermal resistance with 200 ft./minute airflow when a heat sink is not being used.
- $\theta_{JA}$ (°C/W) 400 ft./minute—Junction-to-ambient thermal resistance with 400 ft./minute airflow when a heat sink is not being used.
- $\theta_{JC}$ (°C/W)—Junction-to-case thermal resistance for device.
- $\theta_{JB}$ (°C/W)—Junction-to-board thermal resistance for specific board being used.

Table 15–2 provides $\theta_{JA}$ (junction-to-ambient thermal resistance) values and $\theta_{JC}$ (junction-to-case thermal resistance) values for Cyclone II devices on a board meeting JEDEC specifications for thermal resistance calculation. The JEDEC board specifications require two signal and two power/ground planes and are available at **www.jedec.org**.

*Table 15–2. Thermal Resistance of Cyclone II Devices for Board Meeting JEDEC Specifications (Part 1 of 2)*

| Device | Pin Count | Package | $\theta_{JA}$ (°C/W) Still Air | $\theta_{JA}$ (°C/W) 100 ft./min. | $\theta_{JA}$ (°C/W) 200 ft./min. | $\theta_{JA}$ (°C/W) 400 ft./min. | $\theta_{JC}$ (°C/W) |
|---|---|---|---|---|---|---|---|
| EP2C5 | 144 | TQFP | 31 | 29.3 | 27.9 | 25.5 | 10 |
| | 208 | PQFP | 30.4 | 29.2 | 27.3 | 22.3 | 5.5 |
| | 256 | FineLine BGA | 30.2 | 26.1 | 23.6 | 21.7 | 8.7 |
| EP2C8 | 144 | TQFP | 29.8 | 28.3 | 26.9 | 24.9 | 9.9 |
| | 208 | PQFP | 30.2 | 28.8 | 26.9 | 21.7 | 5.4 |
| | 256 | FineLine BGA | 27 | 23 | 20.5 | 18.5 | 7.1 |
| EP2C15 | 256 | FineLine BGA | 24.2 | 20 | 17.8 | 16 | 5.5 |
| | 484 | FineLine BGA | 21 | 17 | 14.8 | 13.1 | 4.2 |
| EP2C20 | 240 | PQFP | 26.6 | 24 | 21.4 | 17.4 | 4.2 |
| | 256 | FineLine BGA | 24.2 | 20 | 17.8 | 16 | 5.5 |
| | 484 | FineLine BGA | 21 | 17 | 14.8 | 13.1 | 4.2 |
| EP2C35 | 484 | FineLine BGA | 19.4 | 15.4 | 13.3 | 11.7 | 3.3 |
| | 484 | Ultra FineLine BGA | 20.6 | 16.6 | 14.5 | 12.8 | 5 |
| | 672 | FineLine BGA | 18.6 | 14.6 | 12.6 | 11.1 | 3.1 |