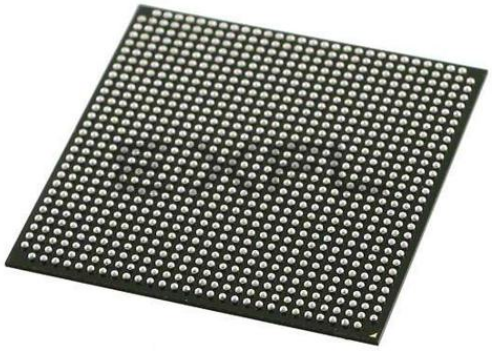

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4276
Number of Logic Elements/Cells	68416
Total RAM Bits	1152000
Number of I/O	622
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c70f896c6n

Table 1–1. Cyclone II FPGA Family Features (Part 2 of 2)

Feature	EP2C5 (2)	EP2C8 (2)	EP2C15 (1)	EP2C20 (2)	EP2C35	EP2C50	EP2C70
Maximum user I/O pins	158	182	315	315	475	450	622

Notes to Table 1–1:

(1) The EP2C15A is only available with the Fast On feature, which offers a faster POR time. This device is available in both commercial and industrial grade.

(2) The EP2C5, EP2C8, and EP2C20 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. The EP2C8A and EP2C20A devices are only available in industrial grade.

(3) This is the total number of 18 × 18 multipliers. For the total number of 9 × 9 multipliers per device, multiply the total number of 18 × 18 multipliers by 2.

This gives a maximum of seven control signals at a time. When using the LAB-wide synchronous load, the `clkena` of `labclk1` is not available. Additionally, register packing and synchronous load cannot be used simultaneously.

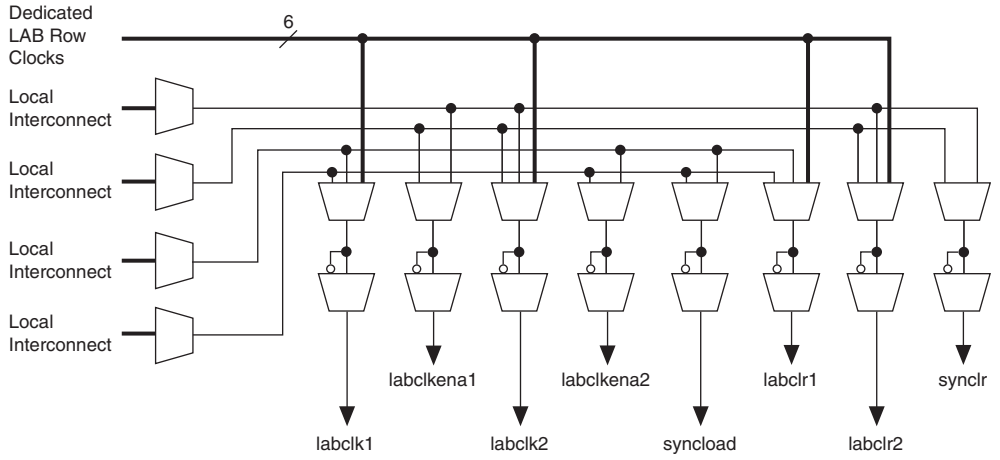
Each LAB can have up to four non-global control signals. Additional LAB control signals can be used as long as they are global signals.

Synchronous clear and load signals are useful for implementing counters and other functions. The synchronous clear and synchronous load signals are LAB-wide signals that affect all registers in the LAB.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal turns off the LAB-wide clock.

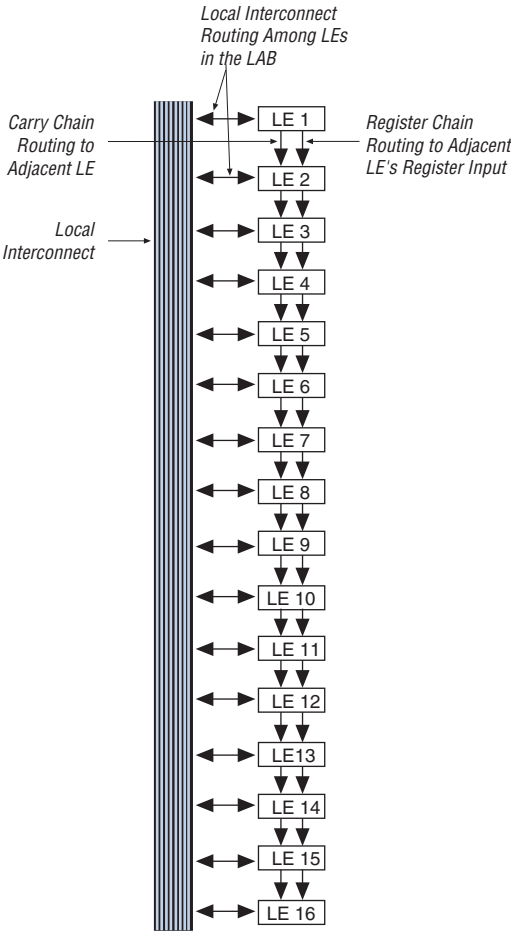
The LAB row clocks [5..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–7 shows the LAB control signal generation circuit.

Figure 2–7. LAB-Wide Control Signals



LAB-wide signals control the logic for the register's clear signal. The LE directly supports an asynchronous clear function. Each LAB supports up to two asynchronous clear signals (`labclr1` and `labclr2`).

Figure 2–9. Register Chain Interconnects



The C4 interconnects span four LABs, M4K blocks, or embedded multipliers up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–10 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including PLLs, M4K memory blocks, embedded multiplier blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor (see Figure 2–10) can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

SignalTap II Embedded Logic Analyzer

Cyclone II devices support the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA® packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

For more information on the SignalTap II, see the *Signal Tap* chapter of the *Quartus II Handbook, Volume 3*.

Configuration

The logic, circuitry, and interconnects in the Cyclone II architecture are configured with CMOS SRAM elements. Altera FPGA devices are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Cyclone II devices are configured at system power-up with data stored in an Altera configuration device or provided by a system controller. The Cyclone II device's optimized interface allows the device to act as controller in an active serial configuration scheme with EPCS serial configuration devices. The serial configuration device can be programmed via SRunner, the ByteBlaster II or USB Blaster download cable, the Altera Programming Unit (APU), or third-party programmers.

In addition to EPCS serial configuration devices, Altera offers in-system programmability (ISP)-capable configuration devices that can configure Cyclone II devices via a serial data stream using the Passive serial (PS) configuration mode. The PS interface also enables microprocessors to treat Cyclone II devices as memory and configure them by writing to a virtual memory location, simplifying reconfiguration. After a Cyclone II device has been configured, it can be reconfigured in-circuit by resetting the device and loading new configuration data. Real-time changes can be made during system operation, enabling innovative reconfigurable applications.

Operating Modes

The Cyclone II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. You can use the 10MHz internal oscillator or the optional `CLKUSR` pin during the initialization. The 10 MHz internal oscillator is disabled in user mode. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
1.2V_DIFFERENTIAL_HSTL	t_{PI}	570	597	1263	1324	1385	1385	ps
	t_{PCOUT}	356	373	801	879	957	957	ps

Notes to Table 5–40 :
(1) These numbers are for commercial devices.
(2) These numbers are for automotive devices.

Table 5–41. Cyclone II I/O Input Delay for Row Pins (Part 1 of 2)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
LVTTL	t_{PI}	583	611	1129	1160	1240	1240	ps
	t_{PCOUT}	366	384	762	784	855	855	ps
2.5V	t_{PI}	629	659	1099	1171	1244	1244	ps
	t_{PCOUT}	412	432	732	795	859	859	ps
1.8V	t_{PI}	729	764	1278	1360	1443	1443	ps
	t_{PCOUT}	512	537	911	984	1058	1058	ps
1.5V	t_{PI}	794	832	1345	1429	1513	1513	ps
	t_{PCOUT}	577	605	978	1053	1128	1128	ps
LVCMOS	t_{PI}	583	611	1129	1160	1240	1240	ps
	t_{PCOUT}	366	384	762	784	855	855	ps
SSTL_2_CLASS_I	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
SSTL_2_CLASS_II	t_{PI}	536	561	896	947	998	998	ps
	t_{PCOUT}	319	334	529	571	613	613	ps
SSTL_18_CLASS_I	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
SSTL_18_CLASS_II	t_{PI}	581	609	933	967	1004	1004	ps
	t_{PCOUT}	364	382	566	591	619	619	ps
1.5V_HSTL_CLASS_I	t_{PI}	593	621	1051	1109	1167	1167	ps
	t_{PCOUT}	376	394	684	733	782	782	ps

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 4 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_2_CLASS_I	OCT_50 _OHMS	67	69	70	25	42	60	25	42	60
SSTL_18_CLASS_I	OCT_50 _OHMS	30	33	36	47	49	51	47	49	51

High Speed I/O Timing Specifications

The timing analysis for LVDS, mini-LVDS, and RSDS is different compared to other I/O standards because the data communication is source-synchronous.

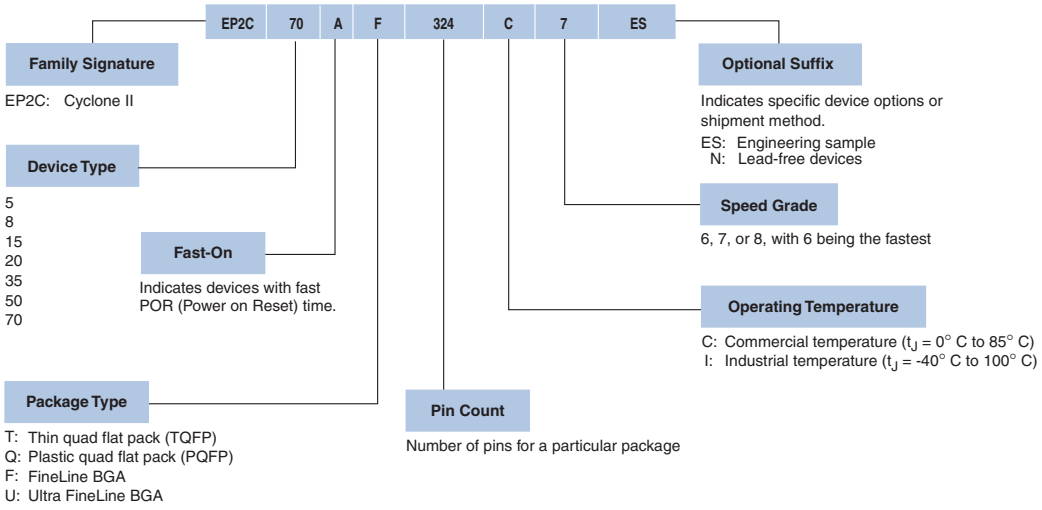
You should also consider board skew, cable skew, and clock jitter in your calculation. This section provides details on the timing parameters for high-speed I/O standards in Cyclone II devices.

Table 5–47 defines the parameters of the timing diagram shown in Figure 5–3.

Table 5–47. High-Speed I/O Timing Definitions (Part 1 of 2)

Parameter	Symbol	Description
High-speed clock	f_{HSCKLK}	High-speed receiver and transmitter input and output clock frequency.
Duty cycle	t_{DUTY}	Duty cycle on high-speed transmitter output clock.
High-speed I/O data rate	HSIODR	High-speed receiver and transmitter input and output data rate.
Time unit interval	TUI	TUI = 1/HSIODR.
Channel-to-channel skew	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement. TCCS = TUI – SW – (2 × RSKM)

Figure 6–1. Cyclone II Device Packaging Ordering Information



Document Revision History

Table 6–1 shows the revision history for this document.

Table 6–1. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v1.5	• Added document revision history. • Updated Figure 6–1.	• Added Ultra FineLine BGA detail in UBGA Package information in Figure 6–1.
November 2005 v1.2	Updated software introduction.	
November 2004 v1.1	Updated Figure 6–1.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	

Each output port has a unique post-scale counter to divide down the high-frequency VCO. There are three post-scale counters (c0, c1, and c2), which range from 1 to 32. The following equations show the frequencies for the three post-scale counters:

$$f_{C0} = \frac{f_{VCO}}{C0} = f_{IN} \frac{m}{n \times C0}$$

$$f_{C1} = \frac{f_{VCO}}{C1} = f_{IN} \frac{m}{n \times C1}$$

$$f_{C2} = \frac{f_{VCO}}{C2} = f_{IN} \frac{m}{n \times C2}$$

All three output counters can drive the global clock network. The c2 output counter can also drive a dedicated external I/O pin (single ended or differential). This counter output can drive a dedicated external clock output pin (`PLL<#>_OUT`) and the global clock network at the same time.

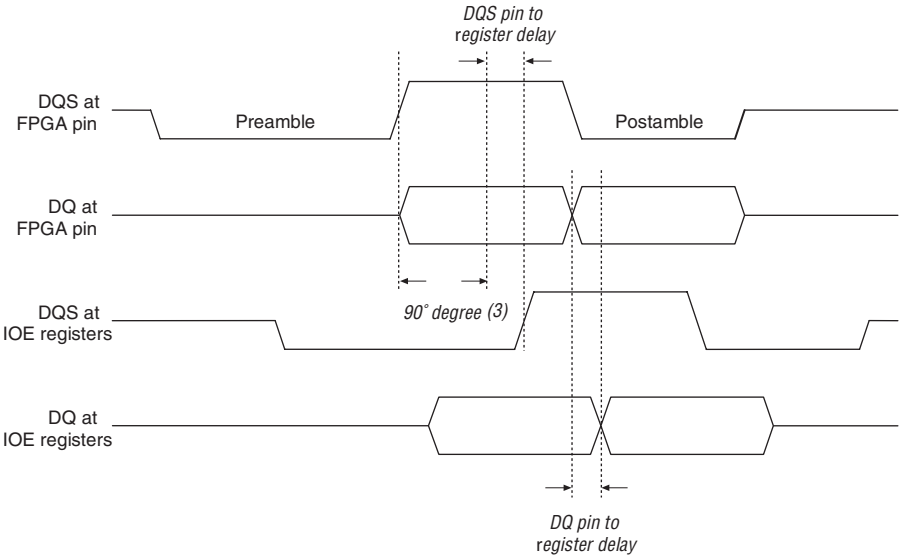
For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets the VCO frequency specifications. Then, the post-scale counters scale down the VCO frequency for each PLL clock output port. For example, if clock output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least common multiple in the VCO's range).

Programmable Duty Cycle

The programmable duty cycle feature allows you to set the PLL clock output duty cycles. The duty cycle is the ratio of the clock output high and low time to the total clock cycle time, expressed as a percentage of high time. This feature is supported on all three PLL post-scale counters, c0, c1, and c2, and when using all clock feedback modes.

The duty cycle is set by using a low- and high-time count setting for the post-scale counters. The Quartus II software uses the input frequency and target multiply/divide ratio to select the post-scale counter. The granularity of the duty cycle is determined by the post-scale counter value chosen on a PLL clock output and is defined as 50% ÷ post-scale counter value. For example, if the post-scale counter value is 3, then the allowable duty cycle precision would be 50% ÷ 3 = 16.67%. Because the `altpll` megafunction does not accept non-integer values for the duty cycle values, the allowable duty cycles are 17% 33% 50% and 67%. For example, if the c0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

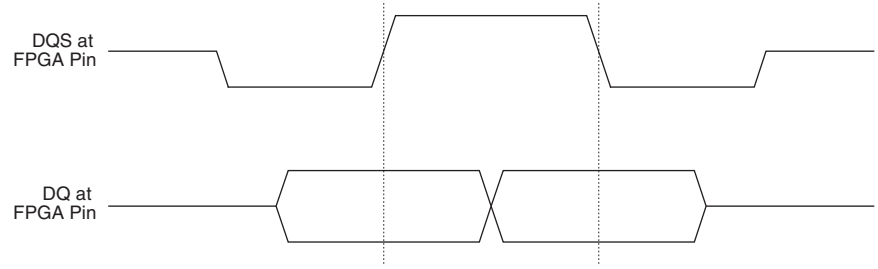
Figure 9–1. Example of a 90° Shift on the DQS Signal *Notes (1), (2)*



Notes to Figure 9–1:
(1) RLDRAM II and QDRII SRAM memory interfaces do not have preamble and postamble specifications.
(2) DDR2 SDRAM does not support a burst length of two.
(3) The phase shift required for your system should be based on your timing analysis and may not be 90°.

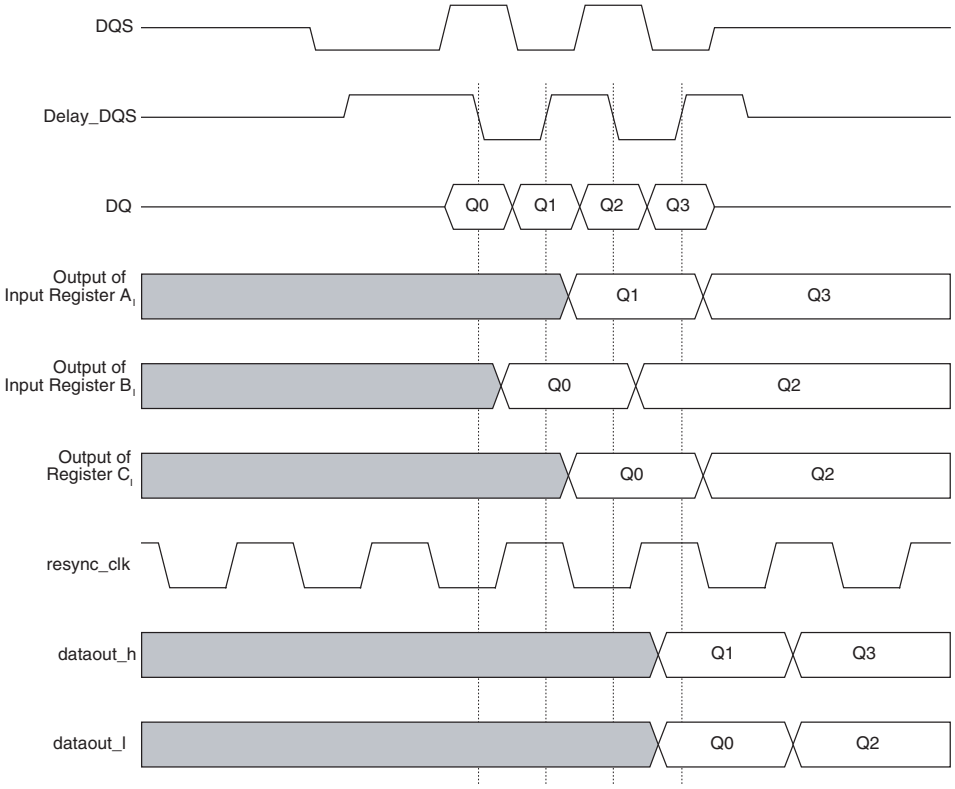
During write operations to a DDR or DDR2 SDRAM device, the FPGA must send the data strobe to the memory device center-aligned relative to the data. Cyclone II devices use a PLL to center-align the data strobe by generating a 0° phase-shifted system clock for the write data strobes and a –90° phase-shifted write clock for the write data pins for the DDR and DDR2 SDRAM. Figure 9–2 shows an example of the relationship between the data and data strobe during a burst-of-two write.

Figure 9–2. DQ & DQS Relationship During a DDR & DDR2 SDRAM Write



Registers sync_reg_h and sync_reg_l synchronize the two data streams to the rising edge of the resynchronization clock. Figure 9–12 shows examples of functional waveforms from a double data rate input implementation.

Figure 9–12. DDR Input Functional Waveforms



The Cyclone II DDR input registers require you to invert the incoming DQS signal to ensure proper data transfer. The altdq megafunction automatically adds the inverter on the clock port of the DQ signals. As shown in Figure 9–11, the inverted DQS signal's rising edge clocks register A_I, its falling edge clocks register B_I, and register C_I aligns the data clocked by register B_I with register A_I on the inverted DQS signal's rising edge. In a DDR memory read operation, the last data coincides with the falling edge of DQS signal. If you do not invert the DQS pin, you do not get this last data because the register does not latch until the next rising edge of the DQS signal.

10. Selectable I/O Standards in Cyclone II Devices

CII51010-2.4

Introduction

The proliferation of I/O standards and the need for improved I/O performance have made it critical that low-cost devices have flexible I/O capabilities. Selectable I/O capabilities such as SSTL-18, SSTL-2, and LVDS compatibility allow Cyclone® II devices to connect to other devices on the same printed circuit board (PCB) that may require different operating and I/O voltages. With these aspects of implementation easily manipulated using the Altera® Quartus® II software, the Cyclone II device family allows you to use low cost FPGAs while keeping pace with increasing design complexity.

This chapter is a guide to understanding the input and output capabilities of the Cyclone II devices, including:

- Supported I/O standards
- Cyclone II I/O banks
- Programmable current drive strength
- I/O termination
- Pad placement and DC guidelines

For information on hot socketing, refer to the *Hot Socketing & Power-On Reset* chapter in volume 1 of the *Cyclone II Device Handbook*.

For information on ESD specifications, refer to the *Altera Reliability Report*.

Supported I/O Standards

Cyclone II devices support the I/O standards shown in Table 10–1.

For more details on the I/O standards discussed in this section, including target data rates and voltage values for each I/O standard, refer to the *DC Characteristics and Timing Specifications* chapter in volume 1 of the *Cyclone II Device Handbook*.

Table 10–2. Cyclone II 66-MHz PCI Support (Part 2 of 2)

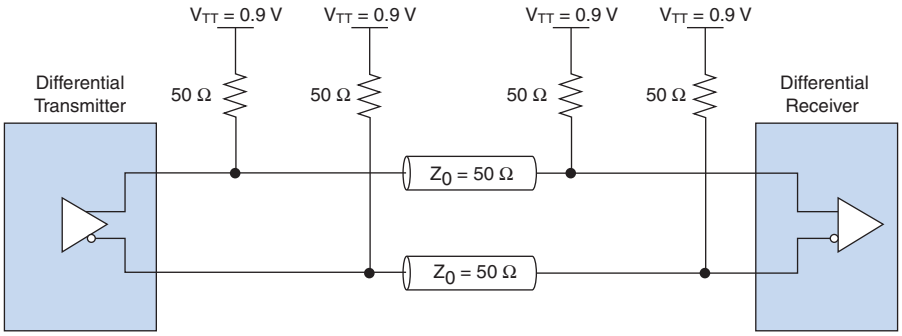
Device	Package	–6 and –7 Speed Grades	
		64 Bits	32 Bits
EP2C8	144-pin TQFP		
	208-pin PQFP		✓
	256-pin FineLine BGA		✓
EP2C15	256-pin FineLine BGA		✓
	484-pin FineLine BGA	✓	✓
EP2C20	240-pin PQFP		✓
	256-pin FineLine BGA		✓
	484-pin FineLine BGA	✓	✓
EP2C35	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C50	484-pin FineLine BGA	✓	✓
	672-pin FineLine BGA	✓	✓
EP2C70	672-pin FineLine BGA	✓	✓
	896-pin FineLine BGA	✓	✓

Table 10–3 lists the specific Cyclone II devices that support 64-bit and 32-bit PCI at 33 MHz.

Table 10–3. Cyclone II 33-MHz PCI Support (Part 1 of 2)

Device	Package	–6, –7 and –8 Speed Grades	
		64 Bits	32 Bits
EP2C5	144-pin TQFP	—	—
	208-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
EP2C8	144-pin TQFP	—	—
	208-pin PQFP	—	✓
	256-pin FineLine BGA	—	✓
EP2C15	256-pin FineLine BGA	—	✓
	484-pin FineLine BGA	✓	✓

Figure 10–12. 1.8-V Differential HSTL Class II Termination



1.5-V LVCMOS (EIA/JEDEC Standard JESD8-11)

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices.

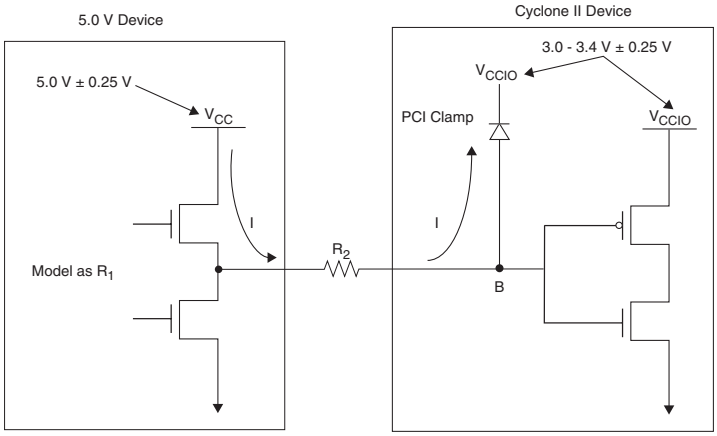
The 1.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.5-V LVCMOS.

1.5-V HSTL Class I and II

The 1.5-V HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic nominal switching range. This standard defines single-ended input and output specifications for all HSTL-compliant digital integrated circuits. The 1.5-V HSTL I/O standard in Cyclone II devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE, APEX 20KC, Stratix® II, Stratix GX, Stratix, and in Cyclone II devices themselves because the input and output voltage thresholds are compatible. Refer to Figures 10–13 and 10–14. Cyclone II devices support both input and output levels with V_{REF} and V_{TT}.

Figure 10–21. Driving a Cyclone II Device with a 5.0-Volt Device



If V_{CCIO} is between 3.0 V and 3.6 V and the PCI clamping diode is enabled, the voltage at point B in Figure 10–21 is 4.3 V or less. To limit large current draw from the 5.0-V device, R_2 should be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (I_{OH}) specifications of the devices driving the trace. The PCI clamping diode in the Cyclone II device can support 25 mA of current.

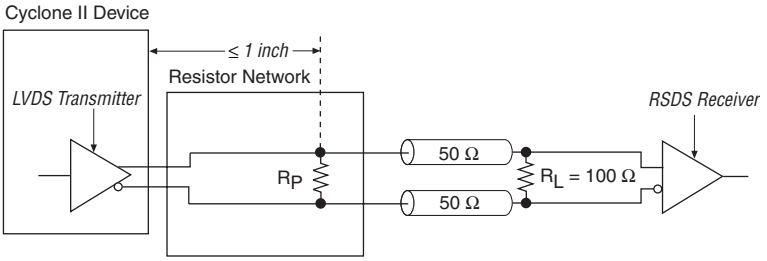
To compute the required value of R_2, first calculate the model of the pull-up transistors on the 5.0-V device. This output resistor (R_1) can be modeled by dividing the 5.0-V device supply voltage (V_{CC}) by the I_{OH}: $R_1 = V_{CC}/I_{OH}$.

Figure 10–22 shows an example of typical output drive characteristics of a 5.0-V device.

Designing with RSDS

Cyclone II devices support the RSDS output standard using the LVDS I/O buffer types. For transmitters, the LVDS output buffer can be used with the external resistor network shown in Figure 11–7.

Figure 11–7. RSDS Resistor Network *Note (1)*



Note to Figure 11–7:
(1) R_S = 120 Ω and R_P = 170 Ω

For more information on the RSDS I/O standard, see the RSDS specification from the National Semiconductor web site **(www.national.com)**.

A resistor network is required to attenuate the LVDS output voltage swing to meet the RSDS specifications. The resistor network values can be modified to reduce power or improve the noise margin. The resistor values chosen should satisfy the following equation:

$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\,\Omega$$

Additional simulations using the IBIS models should be performed to validate that custom resistor values meet the RSDS requirements.

Single Resistor RSDS Solution

The external single resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. To transmit the RSDS signal, an external resistor (R_P) is connected in parallel between the two adjacent I/O pins on the board as shown in Figure 11–8. The recommended value of the resistor R_P is 100 Ω

Figures 11–14 and 11–15 show differential HSTL class I and II interfaces, respectively.

Figure 11–14. Differential HSTL Class I Interface

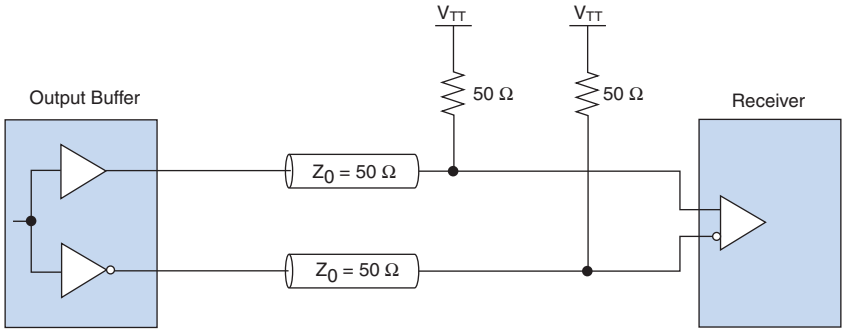
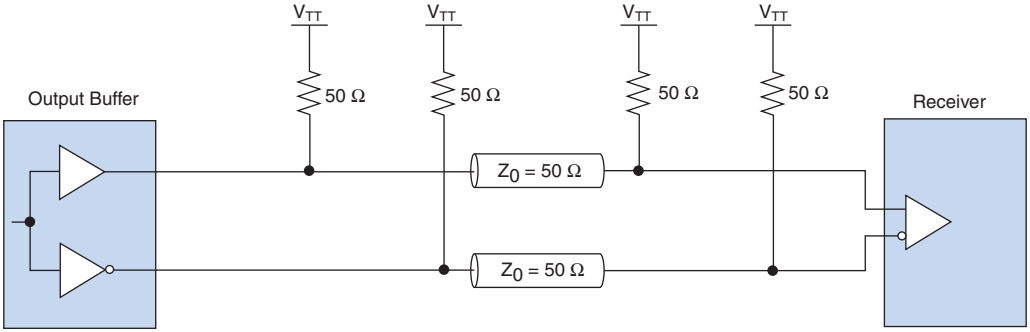


Figure 11–15. Differential HSTL Class II Interface



High-Speed I/O Timing in Cyclone II Devices

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Cyclone II devices. LVDS, LVPECL, RSDS, and mini-LVDS I/O standards enable high-speed data transmission. Timing for these high-speed signals is based on skew between the data and the clock signals.

High-speed differential data transmission requires timing parameters provided by integrated circuit (IC) vendors and requires consideration of board skew, cable skew, and clock jitter. This section provides details on high-speed I/O standards timing parameters in Cyclone II devices.

Table 13–7 defines the timing parameters for Cyclone II devices for PS configuration.

Table 13–7. PS Timing Parameters for Cyclone II Devices

Symbol	Parameter	Minimum	Maximum	Units
t_{POR}	POR delay *(1)*	100		ms
t_{CF2CD}	nCONFIG low to CONF_DONE low		800	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low		800	ns
t_{CFG}	nCONFIG low pulse width	2		µs
t_{STATUS}	nSTATUS low pulse width	10	40 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high		40 *(2)*	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	40		µs
t_{ST2CK}	nSTATUS high to first rising edge on DCLK	1		µs
t_{DSU}	Data setup time before rising edge on DCLK	7		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CH}	DCLK high time	4		ns
t_{CL}	DCLK low time	4		ns
t_{CLK}	DCLK period	10		ns
f_{MAX}	DCLK frequency		100	MHz
t_{CD2UM}	CONF_DONE high to user mode *(3)*	18	40	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period		
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (299 × CLKUSR period)		

Notes to Table 13–7:

(1) The POR delay minimum of 100 ms only applies for non "A" devices.

(2) This value is applicable if users do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting the device.

Device configuration options and how to create configuration files are discussed further in the *Software Settings* section in Volume 2 of the *Configuration Handbook*.

PS Configuration Using a Microprocessor

In the PS configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone II device.

Table 13–11. Dedicated Configuration Pins on the Cyclone II Device (Part 3 of 5)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bidirectional open-drain	This pin is a status output and input. The target Cyclone II device drives the CONF_DONE pin low before and during configuration. Once the Cyclone II device receives all the configuration data without error and the initialization cycle starts, it releases CONF_DONE. Driving CONF_DONE low during user mode does not affect the configured device. Do not drive CONF_DONE low before the device enters user mode. After the Cyclone II device receives all the data, the CONF_DONE pin transitions high, and the device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device. The enhanced configuration devices' and EPC2 devices' OE and nCS pins are connected to the Cyclone II device's nSTATUS and CONF_DONE pins, respectively, and have optional internal programmable pull-up resistors. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on these pins. When using EPC2 devices, you should only use external 10-kΩ pull-up resistors. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.
nCE	N/A	All	Input	This pin is an active-low chip enable. The nCE pin activates the device with a low signal to allow configuration. The nCE pin must be held low during configuration, initialization, and user mode. In single device configuration, it should be tied low. In multiple device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. The nCE pin must also be held low for successful JTAG programming of the FPGA. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.

Table 14–2 describes the capture and update register capabilities of all types of boundary-scan cells within Cyclone II devices.

Table 14–2. Cyclone II Device Boundary Scan Cell Descriptions *Note (1)*

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Dedicated clock input	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to clock network or logic array
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to control logic
Dedicated bidirectional (open drain) *(4)*	0	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to configuration control
Dedicated bidirectional *(5)*	OUTJ	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	OUTJ drives to output buffer

Notes to Table 14–2:

(1) TDI, TDO, TMS, TCK, all V_{CC} and GND pin types do not have BSCs.
(2) N.C.: no connect.
(3) This includes nCONFIG, MSEL0, MSEL1, DATA0, and nCE pins and DCLK (when not used in Active Serial mode).
(4) This includes CONF_DONE and nSTATUS pins.
(5) This includes DCLK (when not used in Active Serial mode).

IEEE Std. 1149.1 BST Operation Control

Cyclone II devices implement the following IEEE Std. 1149.1 BST instructions: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE, USERCODE, CLAMP, and HIGHZ. The BST instruction length is 10 bits. These instructions are described later in this chapter.

For summaries of the BST instructions and their instruction codes, see the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

The IEEE Std. 1149.1 test access port (TAP) controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 14–5 shows the TAP controller state machine.

Table 15–8. 208-Pin PQFP Package Outline Dimensions (Part 2 of 2)			
Symbol	Millimeter		
	Min.	Nom.	Max.
e	0.50 BSC		
q	0°	3.5°	8°

Figure 15–2 shows a 208-pin PQFP package outline.

Figure 15–2. 208-pin PQFP Package Outline