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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4276
Number of Logic Elements/Cells	68416
Total RAM Bits	1152000
Number of I/O	622
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c70f896c7n

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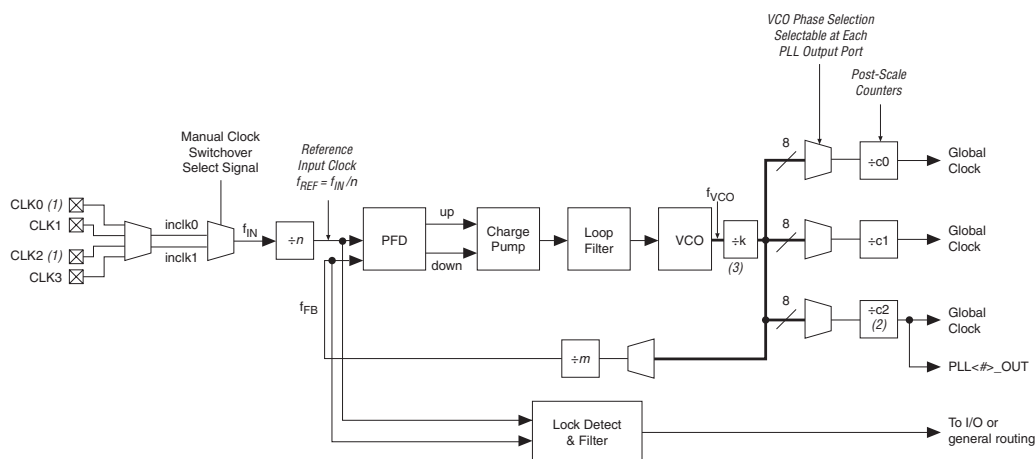
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Figure 2–16 shows a block diagram of the Cyclone II PLL.

Figure 2–16. Cyclone II PLL *Note (1)*



Notes to Figure 2–16:

- (1) This input can be single-ended or differential. If you are using a differential I/O standard, then two CLK pins are used. LVDS input is supported via the secondary function of the dedicated CLK pins. For example, the CLK0 pin's secondary function is LVDSCLK1p and the CLK1 pin's secondary function is LVDSCLK1n. If a differential I/O standard is assigned to the PLL clock input pin, the corresponding CLK (n) pin is also completely used. The Figure 2–16 shows the possible clock input connections (CLK0/CLK1) to PLL1.
- (2) This counter output is shared between a dedicated external clock output I/O and the global clock network.



For more information on Cyclone II PLLs, see the PLLs in the *Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

Embedded Memory

The Cyclone II embedded memory consists of columns of M4K memory blocks. The M4K memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. The output registers can be bypassed, but input registers cannot.

Clock Modes

Table 2–8 summarizes the different clock modes supported by the M4K memory.

Table 2–8. M4K Clock Modes	
Clock Mode	Description
Independent	In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side.
Input/output	On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, <i>wren</i> , and address. The other clock controls the block's data output registers.
Read/write	Up to two clocks are available in this mode. The write clock controls the block's data inputs, <i>wraddress</i> , and <i>wren</i> . The read clock controls the data output, <i>rdaddress</i> , and <i>rden</i> .
Single	In this mode, a single clock, together with clock enable, is used to control all registers of the memory block. Asynchronous clear signals for the registers are not supported.

Table 2–9 shows which clock modes are supported by all M4K blocks when configured in the different memory modes.

Table 2–9. Cyclone II M4K Memory Clock Modes			
Clocking Modes	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode
Independent	✓		
Input/output	✓	✓	✓
Read/write		✓	
Single clock	✓	✓	✓

M4K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K block local interconnect. The M4K blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. M4K block outputs can also connect to left and right LABs through each 16 direct link interconnects. Figure 2–17 shows the M4K block to logic array interface.

Operating Conditions

Cyclone® II devices are offered in commercial, industrial, automotive, and extended temperature grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the parameter values in this chapter apply to all Cyclone II devices. AC and DC characteristics are specified using the same numbers for commercial, industrial, and automotive grades. All parameters representing voltages are measured with respect to ground.

Tables 5–1 through 5–4 provide information on absolute maximum ratings.

Table 5–1. Cyclone II Device Absolute Maximum Ratings <i>Notes (1), (2)</i>					
Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Output supply voltage		–0.5	4.6	V
$V_{CCA-PLL}$ [1..4]	PLL supply voltage		–0.5	1.8	V
V_{IN}	DC input voltage (3)	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias	—	125	°C

Notes to Table 5–1:

- (1) Conditions beyond those listed in this table cause permanent damage to a device. These are stress ratings only. Functional operation at these levels or any other conditions beyond those specified in this chapter is not implied. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effect on the device reliability.
- (2) Refer to the *Operating Requirements for Altera Devices Data Sheet* for more information.
- (3) During transitions, the inputs may overshoot to the voltage shown in Table 5–4 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transition, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The VCO frequency is a critical parameter that must be between 300 and 1,000 MHz to ensure proper operation of the PLL. The Quartus II software automatically sets the VCO frequency within the recommended range based on the clock output and phase-shift requirements in your design.

PLL Reference Clock Generation

In Cyclone II devices, up to four clock pins can drive the PLL, as shown in [Figure 7-11 on page 7-26](#). The multiplexer output feeds the PLL reference clock input. The PLL has internal delay elements that compensate for the clock delay from the input pin to the clock input port of the PLL.

[Table 7-3](#) shows the clock input pin connections to the PLLs in the Cyclone II device.

Table 7-3. PLL Clock Input Pin Connections								
Device	PLL 1		PLL 2		PLL 3		PLL 4	
	CLK0 CLK1	CLK2 CLK3	CLK4 CLK5	CLK6 CLK7	CLK8 CLK9	CLK10 CLK11	CLK12 CLK13	CLK14 CLK15
EP2C5	✓	✓	✓	✓				
EP2C8	✓	✓	✓	✓				
EP2C15	✓	✓	✓	✓	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓	✓	✓	✓	✓

Each PLL can be fed by one of four single-ended or two differential clock input pins. For example, PLL 1 can be fed by CLK[3..0] when using a single-ended I/O standard. When your design uses a differential I/O standard, these same clock pins have a secondary function as LVDSCLK[2..1]p and LVDSCLK[2..1]n pins. When using differential clocks, the CLK0 pin's secondary function is LVDSCLK1p, the CLK1 pin's secondary function is LVDSCLK1n, etc.

VCCA & GNDA

Each Cyclone II PLL uses separate VCC and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called `VCCA_PLL<PLL number>` and `GNDA_PLL<PLL number>`. Connect the VCCA power pin to a 1.2-V power supply, even if you do not use the PLL. Isolate the power connected to VCCA from the power to the rest of the Cyclone II device or any other digital device on the board. You can use one of three different methods of isolating the VCCA pin:

- Use separate VCCA power planes
- Use a partitioned VCCA island within the VCCINT plane
- Use thick VCCA traces

Separate VCCA Power Plane

A mixed signal system is already partitioned into analog and digital sections, each with its own power planes on the board. To isolate the VCCA pin using a separate VCCA power plane, connect the VCCA pin to the analog 1.2-V power plane.

Partitioned VCCA Island Within the VCCINT Plane

Fully digital systems do not have a separate analog power plane on the board. Since it is expensive to add new planes to the board, you can create islands for `VCCA_PLL`. [Figure 7–16](#) shows an example board layout with an analog power island. The dielectric boundary that creates the island should be 25 mils thick. [Figure 7–16](#) shows a partitioned plane within `VCCINT` for VCCA.

applications require local data storage, traditionally implemented with standard flip-flops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources.

The size of a $(w \times m \times n)$ shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n), and must be less than or equal to the maximum number of memory bits, which is 4,608 bits. In addition, the size of $(w \times n)$ must be less than or equal to the maximum width of the block, which is 36 bits. If a larger shift register is required, the memory blocks can be cascaded.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 8–12 shows the Cyclone II memory block in the shift register mode.

Figure 8–12. Cyclone II Shift Register Mode Configuration

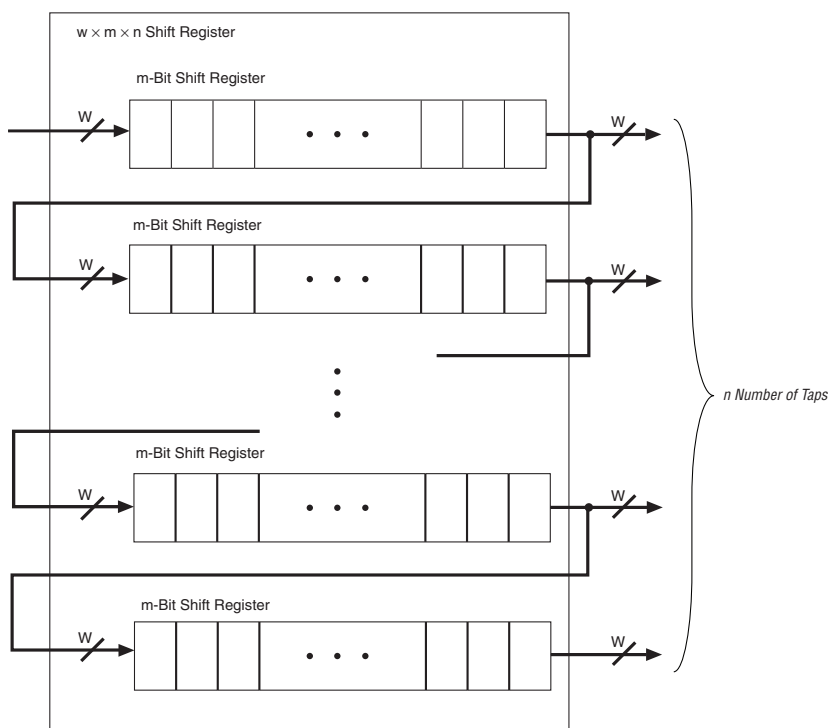
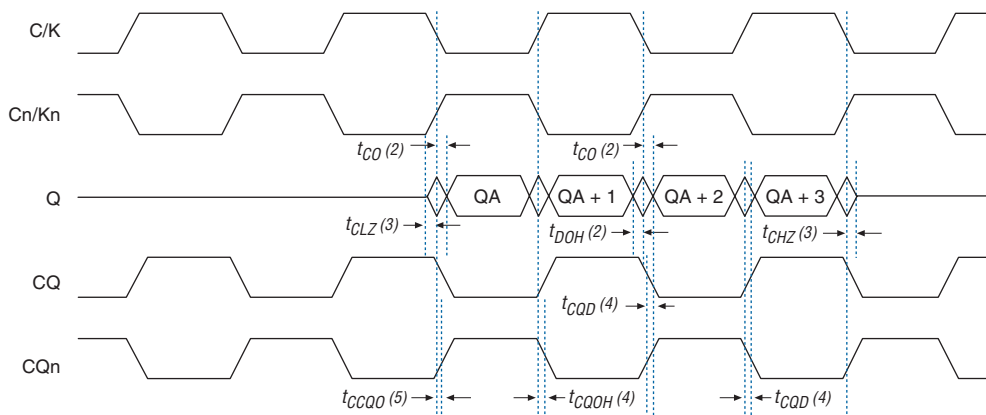


Figure 9–5. Data & Clock Relationship During a QDRII SRAM Report



Notes to Figure 9–5:

- (1) The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
- (2) t_{CO} is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
- (3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times, respectively.
- (4) t_{CQD} is the skew between CQn and data edges.
- (5) t_{CCQO} and t_{CQOH} are skew measurements between the C or C# clocks (or the K or K# clocks in single-clock mode) and the CQ or CQn clocks.

When writing to QDRII SRAM devices, the write clock generates the data while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

DQS pin to the DQ LE register does not necessarily match the delay from the DQ pin to the DQ LE register. Therefore, you must adjust the clock delay control circuitry to compensate for this difference in delays.

DQS Postamble

For external memory interfaces that use a bidirectional read strobe, such as DDR and DDR2 SDRAM, the DQS signal is low before going to or coming from the high-impedance state (see [Figure 9–1](#)). The state where DQS is low just after high-impedance is called the preamble and the state where DQS is low just before it goes to high-impedance is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR and DDR2 SDRAM. If the Cyclone II device or the DDR/DDR2 SDRAM device does not drive the DQ and DQS pins, the signals go to a high-impedance state. Because a pull-up resistor terminates both DQ and DQS to V_{TT} (1.25 V for SSTL-2 and 0.9 V for SSTL-18), the effective voltage on the high-impedance line is either 1.25 V or 0.9 V. According to the JEDEC JESD8-9 specification for SSTL-2 I/O standard and the JESD8-15A specification for SSTL-18 I/O standard, this is an indeterminate logic level, and the input buffer can interpret this as either a logic high or logic low. If there is any noise on the DQS line, the input buffer may interpret that noise as actual strobe edges.

Cyclone II devices have non-dedicated logic that can be configured to prevent a false edge trigger at the end of the DQS postamble. Each Cyclone II DQS signal is connected to postamble logic that consists of a D flip flop (see [Figure 9–9](#)). This register is clocked by the shifted DQS signal. Its input is connected to ground. The controller needs to include extra logic to tell the reset signal to release the preset signal on the falling DQS edge at the start of the postamble. This disables any glitches that happen right after the postamble. This postamble logic is automatically implemented by the Altera MegaCore DDR/DDR2 SDRAM Controller in the LE register as part of the open-source datapath.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pads in relation to differential pads in the same I/O bank. Use the following guidelines for placing single-ended pads with respect to differential pads and for differential output pads placement in Cyclone II devices.

For the LVDS I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVDS I/O pad.
- Single-ended outputs can be no closer than five pads away from an LVDS I/O pad.
- Maximum of four 155-MHz (or greater) LVDS output channels per V_{CCIO} and ground pair.
- Maximum of three 311-MHz (or greater) LVDS output channels per V_{CCIO} and ground pair.



For optimal signal integrity at the LVDS input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVDS input pad.

The Quartus II software only checks the first two cases.

For the RSDS and mini-LVDS I/O standards:

- Single-ended inputs can be no closer than four pads away from an RSDS and mini-LVDS output pad.
- Single-ended outputs can be no closer than five pads away from an RSDS and mini-LVDS output pad.
- Maximum of three 85-MHz (or greater) RSDS and mini-LVDS output channels per V_{CCIO} and ground pair.

The Quartus II software only checks the first two cases.

For the LVPECL I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVPECL input pad.
- Single-ended outputs can be no closer than five pads away from an LVPECL input pad.



For optimal signal integrity at the LVPECL input pad, Altera recommends the LVDS, RSDS and mini-LVDS outputs are placed five or more pads away from an LVPECL input pad.

If the bidirectional pads are all controlled by the same output enable (OE) and there are no other outputs or voltage referenced inputs in the bank, then there is no case where there is a voltage referenced input is active at the same time as an output. Therefore, the output limitation does not apply. However, since the bidirectional pads are linked to the same OE, all the bidirectional pads act as inputs at the same time. Therefore, the input limitation of 30 input pads (15 on each side of the V_{REF} pad) for FineLine BGA packages and 20 input pads (10 on each side of the V_{REF} pad) for QFP packages applies.

If the bidirectional pads are all controlled by different OEs, and there are no other outputs or voltage referenced inputs in the bank, then there may be a case where one group of bidirectional pads is acting as inputs while another group is acting as outputs. In such cases, apply the formulas shown in [Table 10–8](#).

Table 10–8. Input-Only Bidirectional Pad Limitation Formulas	
Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤ 9 (per V_{CCIO} and ground pair)
QFP	(Total number of bidirectional pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤ 5 (per V_{CCIO} and ground pair).

Consider a FineLine BGA package with four bidirectional pads controlled by the first OE, four bidirectional pads controlled by the second OE, and two bidirectional pads controlled by the third OE. If the first and second OEs are active and the third OE is inactive, there are 10 bidirectional pads, but it is safely allowable because there would be 8 or fewer outputs per V_{CCIO}/GND pair.

When at least one additional voltage referenced input and no other outputs exist in the same V_{REF} bank, the bidirectional pad limitation applies in addition to the input and output limitations. See the following equations:

Total number of bidirectional pads + total number of input pads ≤ 30
(15 on each side of your V_{REF} pad) for Fineline BGA packages

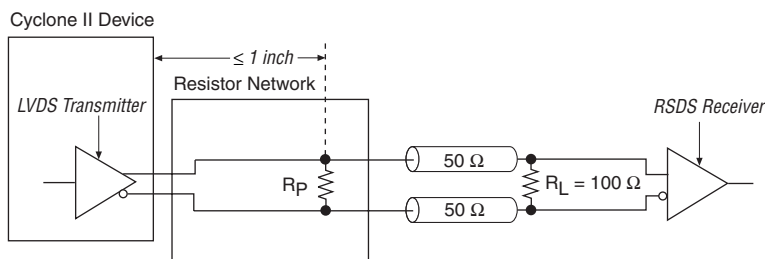
Total number of bidirectional pads + total number of input pads ≤ 20
(10 on each side of your V_{REF} pad) for QFP packages

November 2005 v2.1	<ul style="list-style-type: none"> • Updated Tables 10–2 and 10–3. • Added PCI Express information. • Updated Table 10–6. 	—
July 2005 v2.0	Updated Table 10–1 .	—
November 2004 v1.1	Updated Table 10–7 .	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

Designing with RSDS

Cyclone II devices support the RSDS output standard using the LVDS I/O buffer types. For transmitters, the LVDS output buffer can be used with the external resistor network shown in Figure 11-7.

Figure 11-7. RSDS Resistor Network Note (1)



Note to Figure 11-7:

(1) $R_S = 120\ \Omega$ and $R_P = 170\ \Omega$



For more information on the RSDS I/O standard, see the RSDS specification from the National Semiconductor web site (www.national.com).

A resistor network is required to attenuate the LVDS output voltage swing to meet the RSDS specifications. The resistor network values can be modified to reduce power or improve the noise margin. The resistor values chosen should satisfy the following equation:

$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\ \Omega$$

Additional simulations using the IBIS models should be performed to validate that custom resistor values meet the RSDS requirements.

Single Resistor RSDS Solution

The external single resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. To transmit the RSDS signal, an external resistor (R_P) is connected in parallel between the two adjacent I/O pins on the board as shown in Figure 11-8. The recommended value of the resistor R_P is $100\ \Omega$.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Cyclone II devices read configuration data via the serial interface, decompress data if necessary, and configure their SRAM cells. The FPGA controls the configuration interface in the AS configuration scheme, while the external host (e.g., the configuration device or microprocessor) controls the interface in the PS configuration scheme.



The Cyclone II decompression feature is available when configuring your Cyclone II device using AS mode.

Table 13–4 shows the MSEL pin settings when using the AS configuration scheme.

Table 13–4. Cyclone II Configuration Schemes		
Configuration Scheme	MSEL1	MSEL0
AS (20 MHz)	0	0
Fast AS (40 MHz) (1)	1	0

Note to Table 13–4:

- (1) Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz. Refer to the *Serial Configuration Devices Data Sheet* for more information.

Single Device AS Configuration

Serial configuration devices have a four-pin interface: serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select ($\overline{\text{nCS}}$). This four-pin interface connects to Cyclone II device pins, as shown in Figure 13–3.

device releases its `nSTATUS` pin after a reset time-out period (maximum of 40 μ s). When the `nSTATUS` pin is released and pulled high by a pull-up resistor, the configuration device reconfigures the chain. If this option is turned off, the external system must monitor `nSTATUS` for errors and then pulse `nCONFIG` low for at least 2 μ s to restart configuration. The external system can pulse the `nCONFIG` pin if the pin is under system control rather than tied to V_{CC} .

Additionally, if the configuration device sends all of its data and then detects that the `CONF_DONE` pin has not transitioned high, it recognizes that the FPGA has not configured successfully. Enhanced configuration devices wait for 64 `DCLK` cycles after the last configuration bit was sent for the `CONF_DONE` pin to transition high. EPC2 devices wait for 16 `DCLK` cycles. After that, the configuration device pulls its OE pin low, which in turn drives the target device's `nSTATUS` pin low. If you turn on the **Auto-restart configuration after error** option in the Quartus II software, the target device resets and then releases its `nSTATUS` pin after a reset time-out period (maximum of 40 μ s). When `nSTATUS` transitions high again, the configuration device reconfigures the FPGA.



For more information on configuration issues, see the *Debugging Configuration Problems* chapter of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site (www.altera.com).

Multiple Device PS Configuration Using a Configuration Device

You can use Altera enhanced configuration devices (EPC16, EPC8, and EPC4 devices) or EPC2 and EPC1 configuration devices to configure multiple Cyclone II devices in a PS configuration chain.

Figure 13–14 shows how to configure multiple devices with an enhanced configuration device. This circuit is similar to the configuration device circuit for a single device, except Cyclone II devices are cascaded for multiple device configuration.

DATA3, you can leave the corresponding bit 3 line blank in the Quartus II software. On the printed circuit board (PCB), leave the DATA3 line from the enhanced configuration device unconnected. Use the Quartus II **Convert Programming Files** window (Tools menu) setup for this scheme.

You can also connect two FPGAs to one of the configuration device's DATA pins while the other DATA pins drive one device each. For example, you could use the 2-bit PS mode to drive two FPGAs with DATA bit 0 (two EP2C5 devices) and the third device (an EP2C8 device) with DATA bit 1. In this example, the memory space required for DATA bit 0 is the sum of the SOF file size for the two EP2C5 devices.

$$1,223,980 \text{ bits} + 1,223,980 \text{ bits} = 2,447,960 \text{ bits}$$

The memory space required for DATA bit 1 is the SOF file size for on EP2C8 device (1,983,792 bits). Since the memory space required for DATA bit 0 is larger than the memory space required for DATA bit 1, the size of the POF file is $2 \times 2,447,960 = 4,895,920$.



For more information on using n -bit PS modes with enhanced configuration devices, see the *Using Altera Enhanced Configuration Devices* in the *Configuration Handbook*.

When configuring SRAM-based devices using n -bit PS modes, use [Table 13–8](#) to select the appropriate configuration mode for the fastest configuration times.

Table 13–8. Recommended Configuration Using n-Bit PS Modes	
Number of Devices (1)	Recommended Configuration Mode
1	1-bit PS
2	2-bit PS
3	4-bit PS
4	4-bit PS
5	8-bit PS
6	8-bit PS
7	8-bit PS
8	8-bit PS

Note to Table 13–8:

- (1) Assume that each DATA line is only configuring one device, not a daisy chain of devices.

Table 13–13 describes the dedicated JTAG pins. JTAG pins must be kept stable before and during configuration to prevent accidental loading of JTAG instructions. The TCK pin has a weak internal pull-down resistor and the TDI and TMS JTAG input pins have weak internal pull-up resistors.

Table 13–13. Dedicated JTAG Pins			
Pin Name	User Mode	Pin Type	Description
TDI	N/A	Input	<p>Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK.</p> <p>If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.</p> <p>The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.</p>
TDO	N/A	Output	<p>Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.</p> <p>If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.</p>
TMS	N/A	Input	<p>Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK.</p> <p>If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.</p> <p>The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.</p>
TCK	N/A	Input	<p>The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.</p> <p>If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to GND.</p> <p>The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.</p>

Conclusion

Cyclone II devices can be configured in AS, PS or JTAG configuration schemes to fit your system's need. The AS configuration scheme supported by Cyclone II devices can now operate at a higher DCLK

Table 15–2. Thermal Resistance of Cyclone II Devices for Board Meeting JEDEC Specifications (Part 2 of 2)

Device	Pin Count	Package	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.	θ_{JC} (° C/W)
EP2C50	484	FineLine BGA	18.4	14.4	12.4	10.9	2.8
	484	Ultra FineLine BGA	19.6	15.6	13.6	11.9	4.4
	672	FineLine BGA	17.7	13.7	11.8	10.2	2.6
EP2C70	672	FineLine BGA	16.9	13	11.1	9.7	2.2
	896	FineLine BGA	16.3	11.9	10.5	9.1	2.1

Table 15–3 provides board dimension information for each package.

Table 15–3. PCB Dimensions *Notes (1), (2)*

2.5 mm Thick	Signal Layers	Power/Ground Layers	Package Dimension (mm)	Board Dimension (mm)
F896	10	10	31	91
F672	8	8	27	87
F672	7	7	27	87
F484	7	7	23	83
F484	6	6	23	83
U484	7	7	19	79
U484	6	6	19	79
F256	6	6	17	77

Notes to Table 15–3:

- (1) Power layer Cu thickness 35 μ m, Cu 90%
- (2) Signal layer Cu thickness 17 μ m, Cu 15%