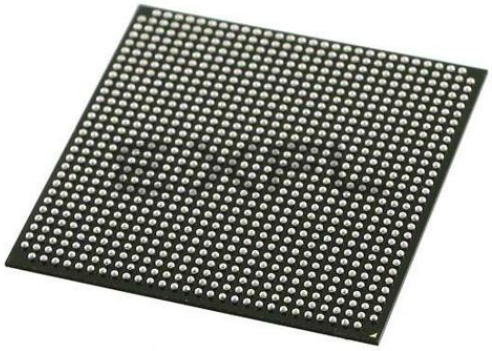

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

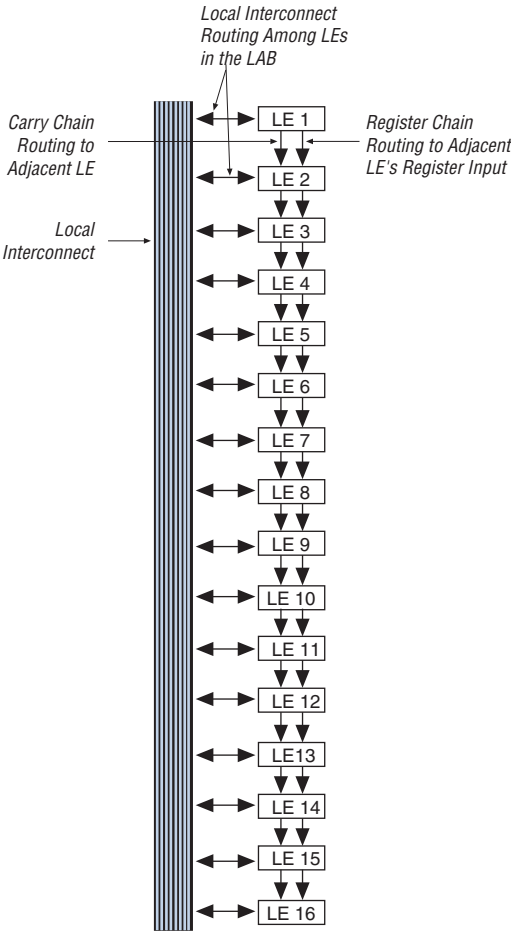
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4276
Number of Logic Elements/Cells	68416
Total RAM Bits	1152000
Number of I/O	622
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c70f896c8

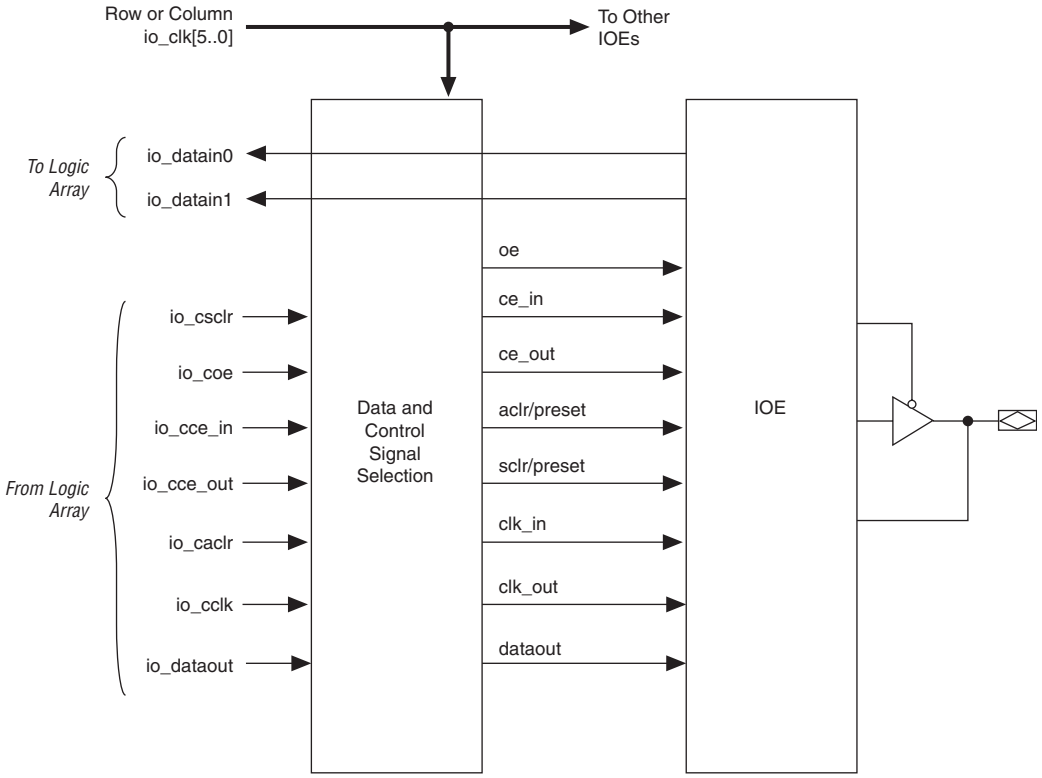
Figure 2–9. Register Chain Interconnects



The C4 interconnects span four LABs, M4K blocks, or embedded multipliers up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–10 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including PLLs, M4K memory blocks, embedded multiplier blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor (see Figure 2–10) can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

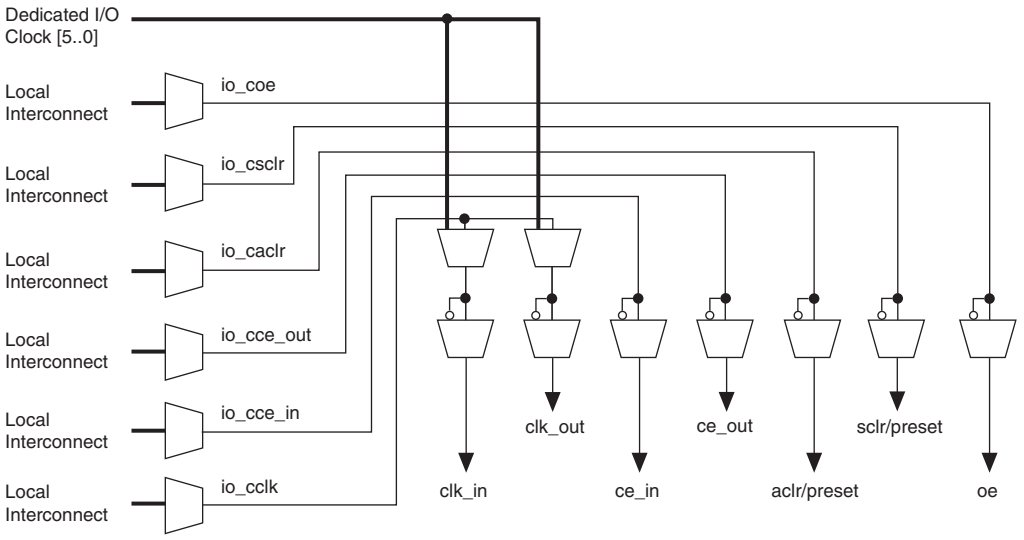
The pin's datain signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks, io_clk[5..0], provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions (see "Global Clock Network & Phase-Locked Loops" on page 2–16). Figure 2–23 illustrates the signal paths through the I/O block.

Figure 2–23. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: oe, ce_in, ce_out, aclr/preset, sclr/preset, clk_in, and clk_out. Figure 2–24 illustrates the control signal selection.

Figure 2–24. Control Signal Selection per IOE



In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. You can use the output register for data requiring fast clock-to-output performance. The OE register is available for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from the local interconnect in the associated LAB, dedicated I/O clocks, or the column and row interconnects. All registers share sclr and aclr, but each register can individually disable sclr and aclr. Figure 2–25 shows the IOE in bidirectional configuration.

Table 2–17. Cyclone II Supported I/O Standards & Constraints (Part 2 of 2)

I/O Standard	Type	V_{CCIO} Level		Top & Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
Differential HSTL-15 class I or class II	Pseudo differential *(4)*	*(5)*	1.5 V				✓ *(7)*	
		1.5 V	*(5)*	✓ *(6)*		✓ *(6)*		
Differential HSTL-18 class I or class II	Pseudo differential *(4)*	*(5)*	1.8 V				✓ *(7)*	
		1.8 V	*(5)*	✓ *(6)*		✓ *(6)*		
LVDS	Differential	2.5 V	2.5 V	✓	✓	✓	✓	✓
RSDS and mini-LVDS *(8)*	Differential	*(5)*	2.5 V		✓		✓	✓
LVPECL *(9)*	Differential	3.3 V/ 2.5 V/ 1.8 V/ 1.5 V	*(5)*	✓		✓		

Notes to Table 2–17:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and turn on the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.
(2) These pins support SSTL-18 class II and 1.8- and 1.5-V HSTL class II inputs.
(3) PCI-X does not meet the IV curve requirement at the linear region. PCI-clamp diode is not available on top and bottom I/O pins.
(4) Pseudo-differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Pseudo-differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them.
(5) This I/O standard is not supported on these I/O pins.
(6) This I/O standard is only supported on the dedicated clock pins.
(7) `PLL_OUT` does not support differential SSTL-18 class II and differential 1.8 and 1.5-V HSTL class II.
(8) mini-LVDS and RSDS are only supported on output pins.
(9) LVPECL is only supported on clock inputs.

For more information on Cyclone II supported I/O standards, see the *Selectable I/O Standards in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

High-Speed Differential Interfaces

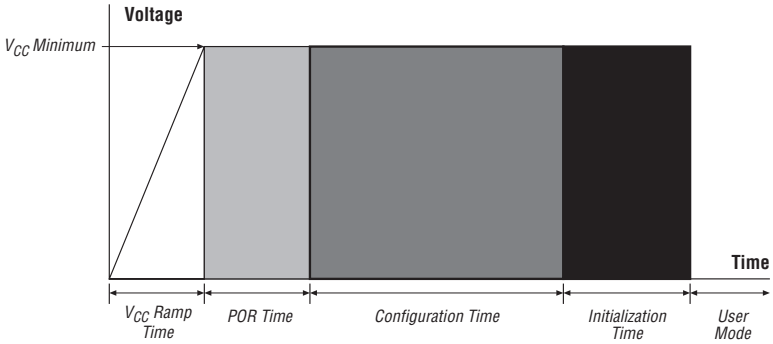
Cyclone II devices can transmit and receive data through LVDS signals at a data rate of up to 640 Mbps and 805 Mbps, respectively. For the LVDS transmitter and receiver, the Cyclone II device's input and output pins support serialization and deserialization through internal logic.

For Cyclone II devices, wake-up time consists of power-up, POR, configuration, and initialization. The device must properly go through all four stages to configure correctly and begin operation. You can calculate wake-up time using the following equation:

Wake-Up Time = V_{CC} Ramp Time + POR Time + Configuration Time + Initialization Time

Figure 4–3 illustrates the components of wake up time.

Figure 4–3. Cyclone II Wake-Up Time



Note to Figure 4–3:
(1) V_{CC} ramp must be monotonic.

The V_{CC} ramp time and POR time will depend on the device characteristics and the power supply used in your system. The fast-on devices require a maximum V_{CC} ramp time of 2 ms and have a maximum POR time of 12 ms.

Configuration time will depend on the configuration mode chosen and the configuration file size. You can calculate configuration time by multiplying the number of bits in the configuration file with the period of the configuration clock. For fast configuration times, you should use Passive Serial (PS) configuration mode with maximum DCLK frequency of 100 MHz. In addition, you can use compression to reduce the configuration file size and speed up the configuration time. The t_{CD2UM} or t_{CD2UMC} parameters will determine the initialization time.

For more information on the t_{CD2UM} or t_{CD2UMC} parameters, refer to the *Configuring Cyclone II Devices* chapter in the *Cyclone II Device Handbook*.

Table 5–19. M4K Block Internal Timing Microparameters (Part 3 of 3)

Parameter	–6 Speed Grade (1)		–7 Speed Grade (2)		–8 Speed Grade (3)		Unit
	Min	Max	Min	Max	Min	Max	
TM4KCLR	191	—	244	—	244	—	ps
	—	—	217	—	244	—	ps

Notes to Table 5–19:

(1) For the –6 speed grades, the minimum timing is for the commercial temperature grade. The –7 speed grade devices offer the automotive temperature grade. The –8 speed grade devices offer the industrial temperature grade.

(2) For each parameter of the –7 speed grade columns, the value in the first row represents the minimum timing parameter for automotive devices. The second row represents the minimum timing parameter for commercial devices.

(3) For each parameter of the –8 speed grade columns, the value in the first row represents the minimum timing parameter for industrial devices. The second row represents the minimum timing parameter for commercial devices.

Cyclone II Clock Timing Parameters

Refer to Tables 5–20 through 5–34 for Cyclone II clock timing parameters.

Table 5–20. Cyclone II Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP2C5/A Clock Timing Parameters

Tables 5–21 and 5–22 show the clock timing parameters for EP2C5/A devices.

Table 5–21. EP2C5/A Column Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
	Industrial/ Automotive	Commercial					
t_{CIN}	1.283	1.343	2.329	2.484	2.688	2.688	ns
t_{COUT}	1.297	1.358	2.363	2.516	2.717	2.717	ns
t_{PLLCIN}	–0.188	–0.201	0.076	0.038	0.042	0.052	ns

I/O Delays

Refer to Tables 5–39 through 5–43 for I/O delays.

Table 5–39. I/O Delay Parameters

Symbol	Parameter
t_{DIP}	Delay from I/O datain to output pad
t_{OP}	Delay from I/O output register to output pad
t_{PCOUT}	Delay from input pad to I/O dataout to core
t_{PI}	Delay from input pad to I/O input register

Table 5–40. Cyclone II I/O Input Delay for Column Pins (Part 1 of 3)

I/O Standard	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (1)	–7 Speed Grade (2)	–8 Speed Grade	Unit
		Industrial/ Automotive	Commer -cial					
LVTTL	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
2.5V	t_{PI}	624	654	1192	1238	1283	1283	ps
	t_{PCOUT}	410	430	730	793	855	855	ps
1.8V	t_{PI}	725	760	1372	1428	1484	1484	ps
	t_{PCOUT}	511	536	910	983	1056	1056	ps
1.5V	t_{PI}	790	828	1439	1497	1556	1556	ps
	t_{PCOUT}	576	604	977	1052	1128	1128	ps
LVCMOS	t_{PI}	581	609	1222	1228	1282	1282	ps
	t_{PCOUT}	367	385	760	783	854	854	ps
SSTL_2_CLASS_I	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_2_CLASS_II	t_{PI}	533	558	990	1015	1040	1040	ps
	t_{PCOUT}	319	334	528	570	612	612	ps
SSTL_18_CLASS_I	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps
SSTL_18_CLASS_II	t_{PI}	577	605	1027	1035	1045	1045	ps
	t_{PCOUT}	363	381	565	590	617	617	ps

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 5 of 6)

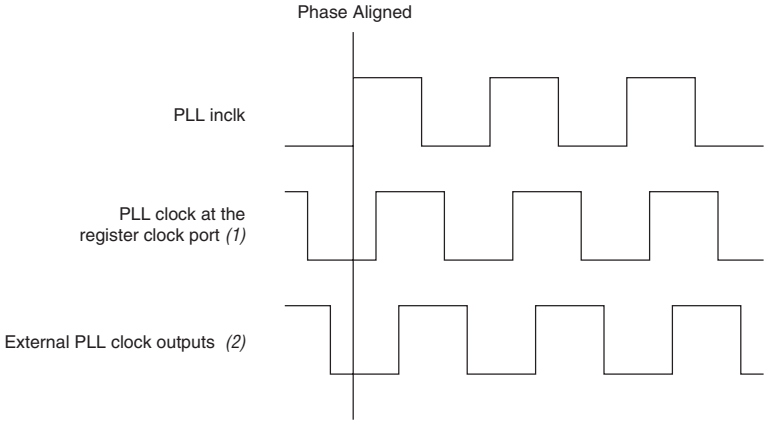
I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
DIFFERENTIAL_ SSTL_18_CLASS_I	6 mA	t_{OP}	1472	1544	3140	3345	3542	3549	ps
		t_{DIP}	1604	1683	3310	3539	3768	3768	ps
	8 mA	t_{OP}	1469	1541	3086	3287	3482	3489	ps
		t_{DIP}	1601	1680	3256	3481	3708	3708	ps
	10 mA	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
	12 mA (1)	t_{OP}	1466	1538	2980	3171	3354	3361	ps
		t_{DIP}	1598	1677	3150	3365	3580	3580	ps
DIFFERENTIAL_ SSTL_18_CLASS_II	16 mA	t_{OP}	1454	1525	2905	3088	3263	3270	ps
		t_{DIP}	1586	1664	3075	3282	3489	3489	ps
	18 mA (1)	t_{OP}	1453	1524	2900	3082	3257	3264	ps
		t_{DIP}	1585	1663	3070	3276	3483	3483	ps
1.8V_DIFFERENTIAL _HSTL_CLASS_I	8 mA	t_{OP}	1460	1531	3222	3424	3618	3625	ps
		t_{DIP}	1592	1670	3392	3618	3844	3844	ps
	10 mA	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
	12 mA (1)	t_{OP}	1462	1534	3090	3279	3462	3469	ps
		t_{DIP}	1594	1673	3260	3473	3688	3688	ps
1.8V_DIFFERENTIAL _HSTL_CLASS_II	16 mA	t_{OP}	1449	1520	2936	3107	3271	3278	ps
		t_{DIP}	1581	1659	3106	3301	3497	3497	ps
	18 mA	t_{OP}	1450	1521	2924	3101	3272	3279	ps
		t_{DIP}	1582	1660	3094	3295	3498	3498	ps
	20 mA (1)	t_{OP}	1452	1523	2926	3096	3259	3266	ps
		t_{DIP}	1584	1662	3096	3290	3485	3485	ps
1.5V_DIFFERENTIAL _HSTL_CLASS_I	8 mA	t_{OP}	1779	1866	4292	4637	4974	4981	ps
		t_{DIP}	1911	2005	4462	4831	5200	5200	ps
	10 mA	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps
	12 mA (1)	t_{OP}	1784	1872	4031	4355	4673	4680	ps
		t_{DIP}	1916	2011	4201	4549	4899	4899	ps

Tables 5–50 and 5–51 show the LVDS timing budget for Cyclone II devices. Cyclone II devices support LVDS receivers at data rates up to 805 Mbps, and LVDS transmitters at data rates up to 640 Mbps.

Table 5–50. LVDS Transmitter Timing Specification (Part 1 of 2)

Symbol	Conditions	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
		Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	Min	Typ	Max (1)	Max (2)	
f_{HSCLK} (input clock frequency)	×10	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×8	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×7	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×4	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×2	10	—	320	320	10	—	275	320	10	—	155.5 (4)	320 (6)	MHz
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (8)	402.5 (8)	MHz
HSIODR	×10	100	—	640	640	100	—	550	640	100	—	311 (5)	550 (7)	Mbps
	×8	80	—	640	640	80	—	550	640	80	—	311 (5)	550 (7)	Mbps
	×7	70	—	640	640	70	—	550	640	70	—	311 (5)	550 (7)	Mbps
	×4	40	—	640	640	40	—	550	640	40	—	311 (5)	550 (7)	Mbps
	×2	20	—	640	640	20	—	550	640	20	—	311 (5)	550 (7)	Mbps
	×1	10	—	402.5	402.5	10	—	402.5	402.5	10	—	402.5 (9)	402.5 (9)	Mbps
t_{DUTY}	—	45	—	55	—	45	—	55	—	45	—	55	—	%
	—	—	—	—	160	—	—	—	312.5	—	—	—	363.6	ps
TCCS (3)	—	—	—	200		—	—	200		—	—	200		ps
Output jitter (peak to peak)	—	—	—	500		—	—	500		—	—	550 (10)		ps
t_{RISE}	20–80%	150	200	250		150	200	250		150	200	250 (11)		ps

Figure 7–6. Phase Relationship between Cyclone II PLL Clocks in No Compensation Mode

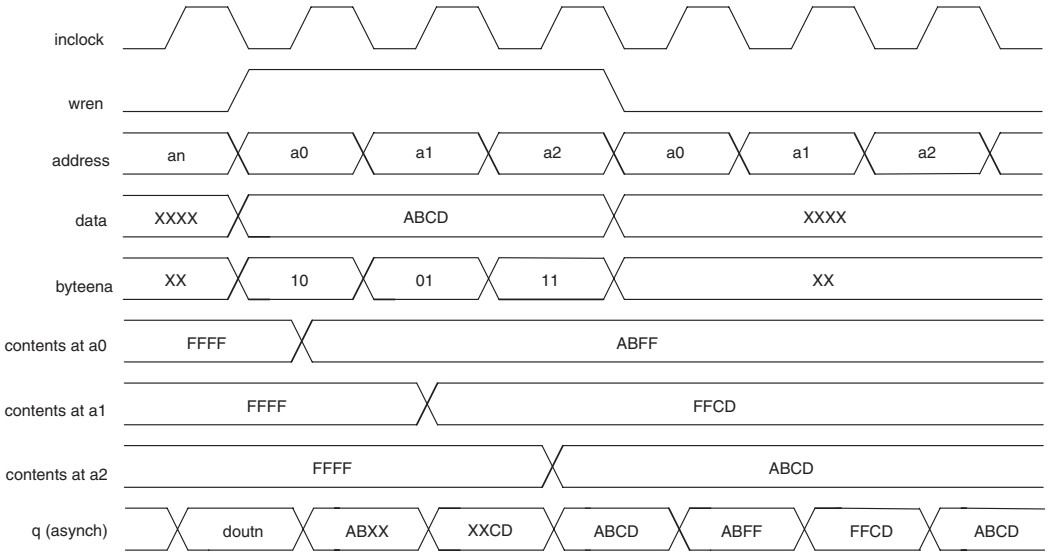


Notes to Figure 7–6:
(1) Internal clocks fed by the PLL are in phase with each other.
(2) The external clock outputs can lead or lag the PLL internal clocks.

Source-Synchronous Mode

If data and clock arrive at the same time at the input pins, they are guaranteed to keep the same phase relationship at the clock and data ports of any IOE input register. Figure 7–7 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfer. Data and clock signals at the IOE experience similar buffer delays as long as the same I/O standard is used.

Figure 8–2. Cyclone II Byte Enable Functional Waveform



Packed Mode Support

Cyclone II M4K memory blocks support packed mode. You can implement two single-port memory blocks in a single block under the following conditions:

- Each of the two independent block sizes is less than or equal to half of the M4K block size. The maximum data width for each independent block is 18 bits wide.
- Each of the single-port memory blocks is configured in single-clock mode.

See "Single-Port Mode" on page 8–9 and "Single-Clock Mode" on page 8–24 for more information.

Address Clock Enable

Cyclone II M4K memory blocks support address clock enables, which holds the previous address value until needed. When the memory blocks are configured in dual-port mode, each port has its own independent address clock enable.

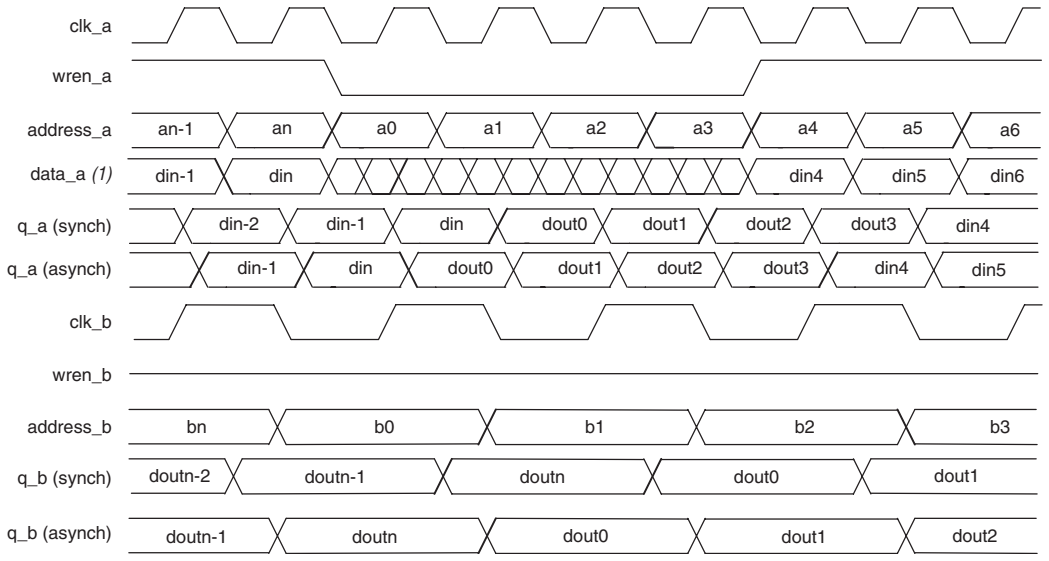
outputs, respectively. When the output registers are bypassed, the new data is available on the rising edge of the same clock cycle on which it was written. See "Read-During- Write Operation at the Same Address" on page 8–28 for waveforms and information on mixed-port read-during-write mode.

Potential write contentions must be resolved external to the RAM because writing to the same address location at both ports results in unknown data storage at that location.

For the maximum synchronous write cycle time, refer to the *Cyclone II Device Family Data Sheet* in volume 1 of the *Cyclone II Device Handbook*.

Figure 8–11 shows true dual-port timing waveforms for the write operation at port A and the read operation at port B.

Figure 8–11. Cyclone II True Dual-Port Timing Waveforms

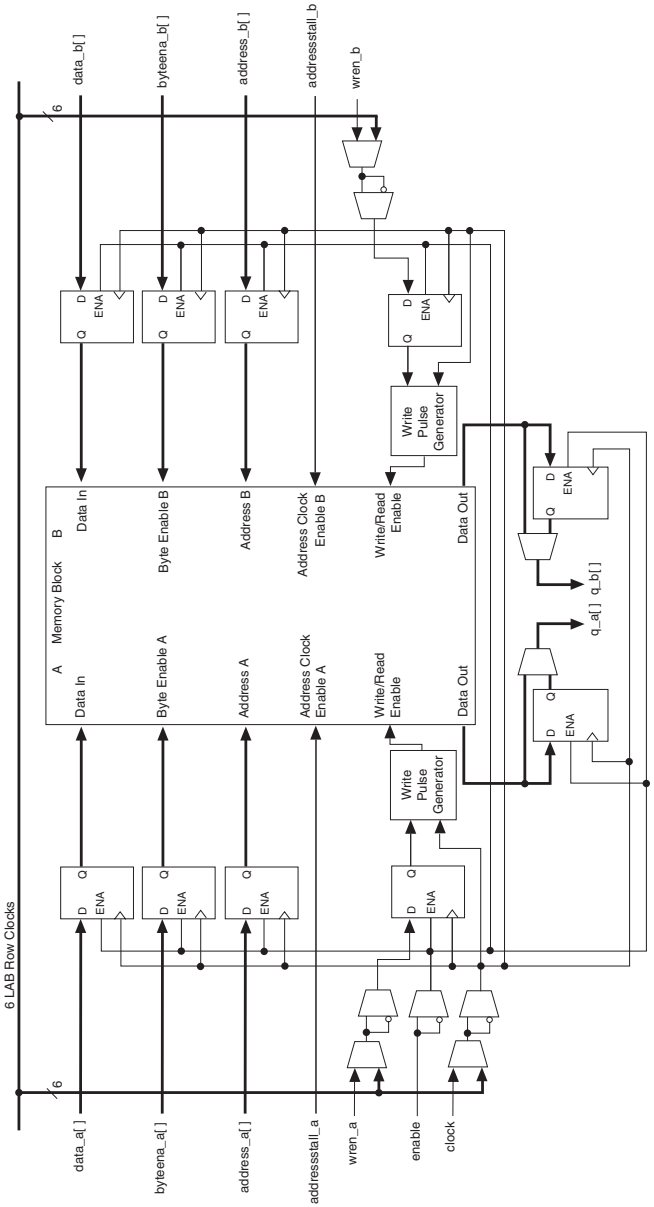


Note to Figure 8–11:
(1) The crosses in the `data_a` waveform during write indicate "don't care."

Shift Register Mode

Cyclone II memory blocks can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto-correlation and cross-correlation functions. These and other DSP

Figure 8–18. Cyclone II Single-Clock Mode in True Dual-Port Mode *Note (1)*



Note to Figure 8–18:

(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Document Revision History

Table 8–8 shows the revision history for this document.

Table 8–8. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v2.4	Corrected Figure 8–12.	—
February 2007 v2.3	• Added document revision history. • Updated "Packed Mode Support" section. • Updated "Mixed-Port Read-During-Write Mode" section and added new Figure 8–24.	• In packed mode support, the maximum data width for each of the two memory block is 18 bits wide. • Added don't care mode information to mixed-port read-during-write mode section.
November 2005 v2.1	Updated Figures 8–13 through 8–20.	—
July 2005 v2.0	Added Clear Signals section.	—
February 2005 v1.1	Added a note to Figures 8-13 through 8-20 regarding violating the setup and hold time on address registers.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

- Cyclone II FPGA (EP2C15 or larger)
- Altera PCI Express Compiler ×1 MegaCore® function
- External PCI Express transceiver/PHY

2.5-V LVTTL (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVTTL applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V devices.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVTTL.

2.5-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-5)

The 2.5-V I/O standard is used for 2.5-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 2.5-V parts.

The 2.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 2.5-V LVCMOS.

SSTL-2 Class I and II (EIA/JEDEC Standard JESD8-9A)

The SSTL-2 I/O standard is a 2.5-V memory bus standard used for applications such as high-speed double data rate (DDR) SDRAM interfaces. This standard defines the input and output specifications for devices that operate in the SSTL-2 logic switching range of 0.0 to 2.5 V. This standard improves operations in conditions where a bus must be isolated from large stubs. The SSTL-2 standard specifies an input voltage range of $-0.3\ V \leq V_I \leq V_{CCIO} + 0.3\ V$. SSTL-2 requires a V_{REF} value of 1.25 V and a V_{TT} value of 1.25 V connected to the termination resistors (refer to Figures 10–1 and 10–2).

RSDS I/O Standard Support in Cyclone II Devices

The RSDS specification is used in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the National Semiconductor Corporation RSDS Interface Specification and support the RSDS output standard. Table 11–2 shows the RSDS electrical characteristics for Cyclone II devices.

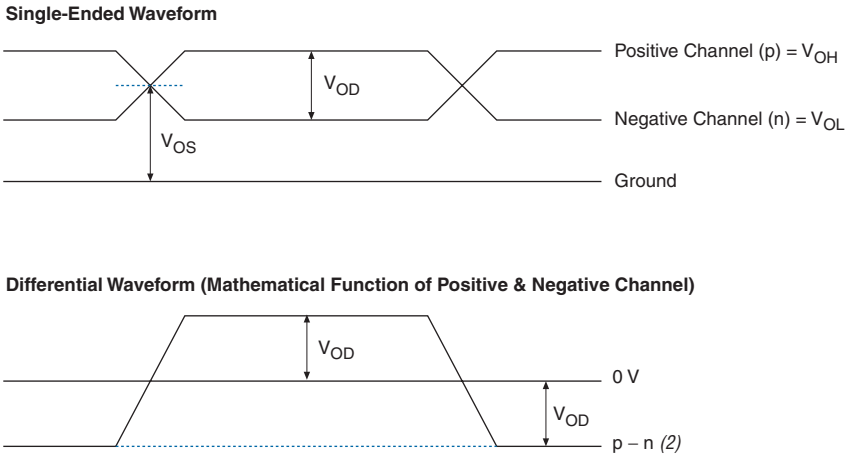
Table 11–2. RSDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	100		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
T_r/T_f	Transition time	20% to 80%		500		ps

Notes to Table 11–2:
(1) The specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

Figure 11–6 shows the RSDS transmitter output signal waveforms.

Figure 11–6. Transmitter Output Signal Level Waveforms for RSDS *Note (1)*

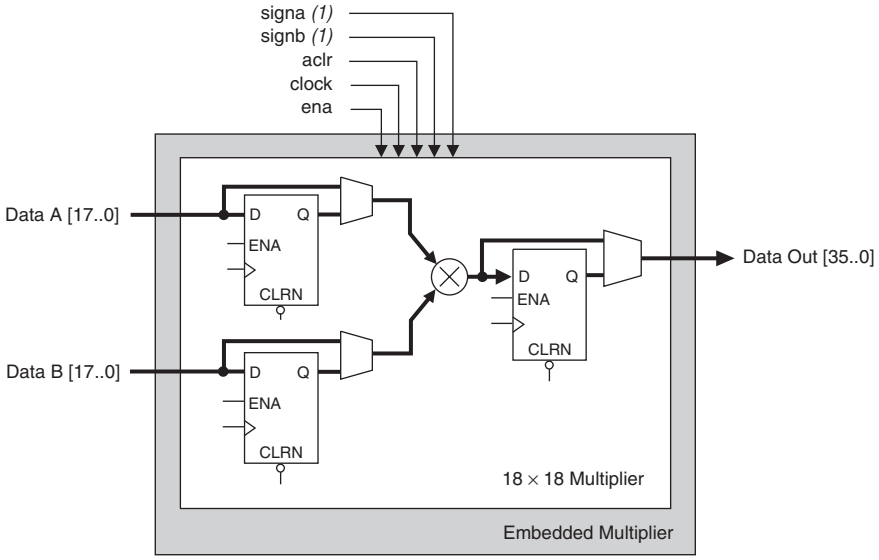


Notes to Figure 11–6:
(1) The V_{OD} specifications apply at the resistor network output.
(2) The p – n waveform is a function of the positive channel (p) and the negative channel (n).

18-Bit Multipliers

Each embedded multiplier can be configured to support a single 18 × 18 multiplier for input widths from 10- to 18-bits. Figure 12–3 shows the embedded multiplier configured to support an 18-bit multiplier.

Figure 12–3. 18-Bit Multiplier Mode



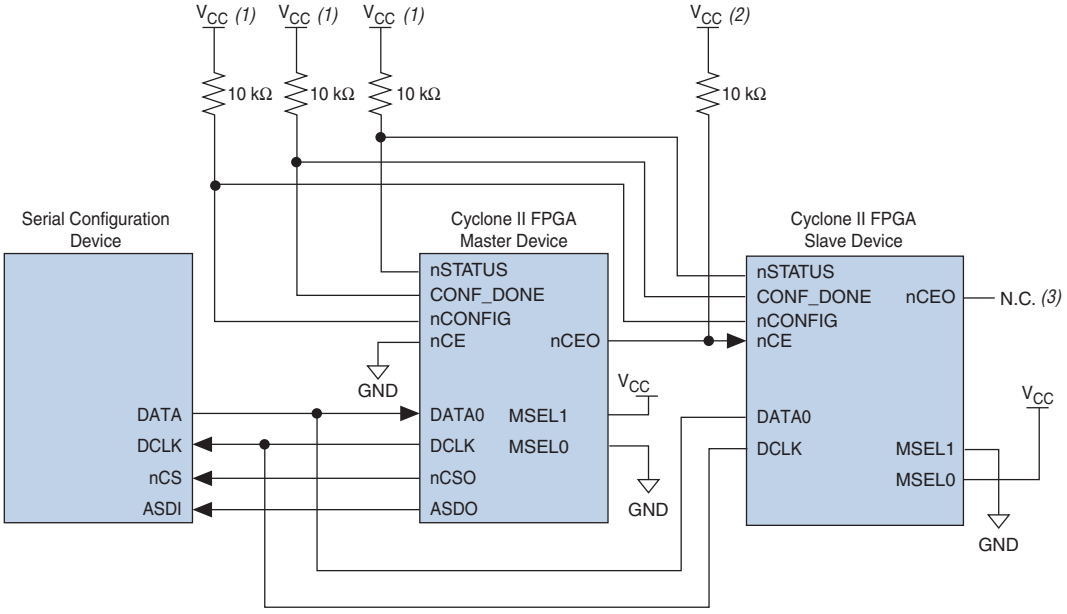
Note to Figure 12–3:
(1) If necessary, you can send these signals through one register to match the data signal path.

All 18-bit multiplier inputs and results can be independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers or a combination of both. Additionally, you can change the `signa` and `signb` signals dynamically and can send these signals through dedicated input registers.

9-Bit Multipliers

Each embedded multiplier can also be configured to support two 9 × 9 independent multipliers for input widths up to 9-bits. Figure 12–4 shows the embedded multiplier configured to support two 9-bit multipliers.

Figure 13–4. Multiple Device AS Configuration



Notes to Figure 13–4:

(1) Connect the pull-up resistors to a 3.3-V supply.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank that the nCEO pin resides in.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

As shown in Figure 13–4, the nSTATUS and CONF_DONE pins on all target FPGAs are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the FPGAs. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep the CONF_DONE signal low until they receive their configuration data. When all the target FPGAs in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor pulls this signal high, and all devices simultaneously enter initialization mode.

The Quartus II software sets the Cyclone II device nCEO pin as an output pin driving to ground by default. If the nCEO pin inputs to the next device's nCE pin, make sure that the nCEO pin is not used as a user I/O pin after configuration.

Other Altera devices that have JTAG support can be placed in the same JTAG chain for device programming and configuration.

For more information on configuring multiple Altera devices in the same configuration chain, see the *Configuring Mixed Altera FPGA Chains* chapter in the *Configuration Handbook*.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP). Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information on JTAG and Jam STAPL in embedded environments, see *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*. To download the Jam player, go to the Altera web site (**www.altera.com**).

Configuring Cyclone II FPGAs with JRunner

JRunner is a software driver that allows you to configure Cyclone II devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in **.rbf** format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

The RBF file used by the JRunner software driver can not be a compressed RBF file because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

For more information on the JRunner software driver, see *JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site.