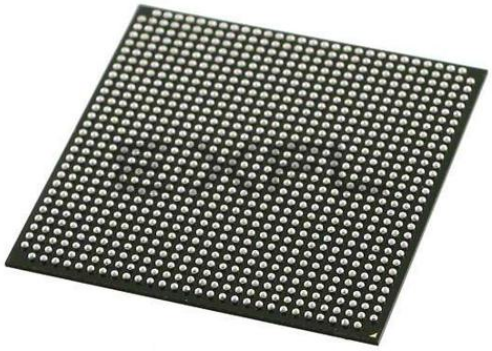

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

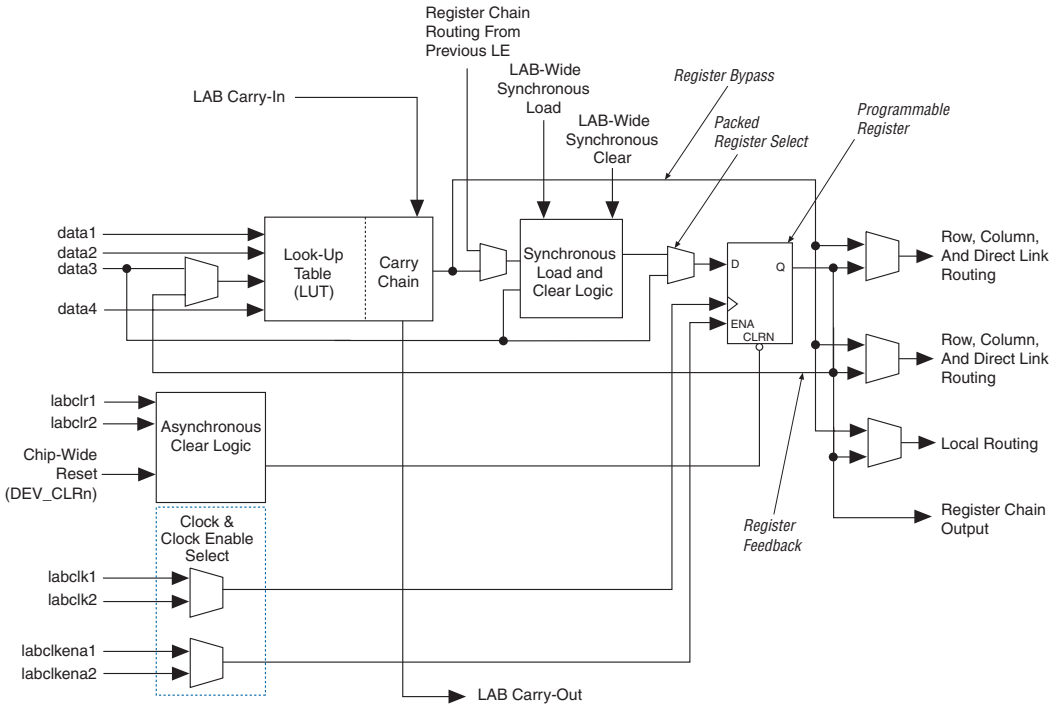
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4276
Number of Logic Elements/Cells	68416
Total RAM Bits	1152000
Number of I/O	622
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2c70f896i8

Figure 2–2 shows a Cyclone II LE.

Figure 2–2. Cyclone II LE



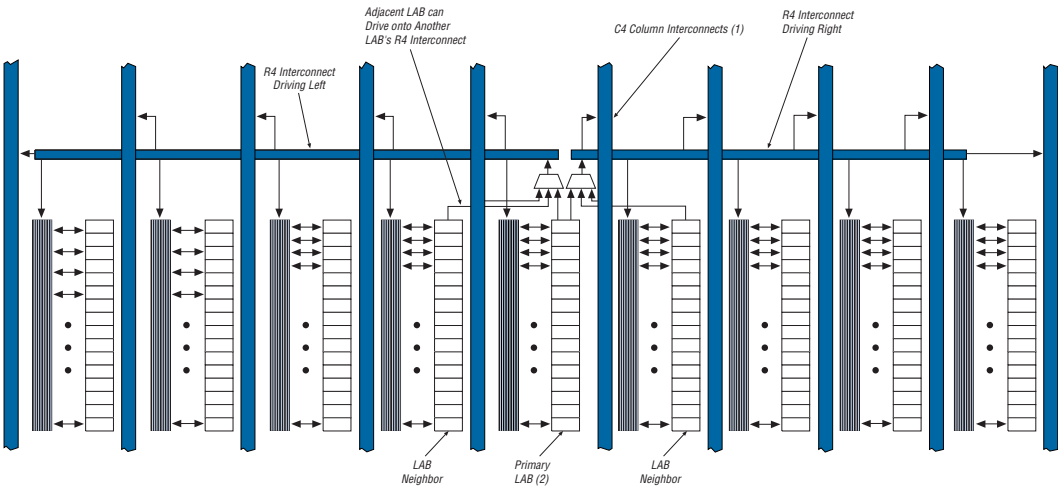
Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, clock, clock enable, and clear inputs. Signals that use the global clock network, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources, allowing the LUT to drive one output while the register drives another output. This feature, register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. When using register packing, the LAB-wide synchronous load control signal is not available. See "LAB Control Signals" on page 2–8 for more information.

The direct link interconnect allows an LAB, M4K memory block, or embedded multiplier block to drive into the local interconnect of its left and right neighbors. Only one side of a PLL block interfaces with direct link and row interconnects. The direct link interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M4K memory block, or three LABs and one embedded multiplier to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–8 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by LABs, M4K memory blocks, embedded multipliers, PLLs, and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor (see Figure 2–8) can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. Additionally, R4 interconnects can drive R24 interconnects, C4, and C16 interconnects for connections from one row to another.

Figure 2–8. R4 Interconnect Connections



Notes to Figure 2–8:

(1) C4 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, M4K memory blocks, embedded multipliers, and IOEs. C16 column interconnects drive to other row and column interconnects at every fourth LAB. C16 column interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. C16 interconnects can drive R24, R4, C16, and C4 interconnects.

Device Routing

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (for example, M4K memory, embedded multiplier, or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

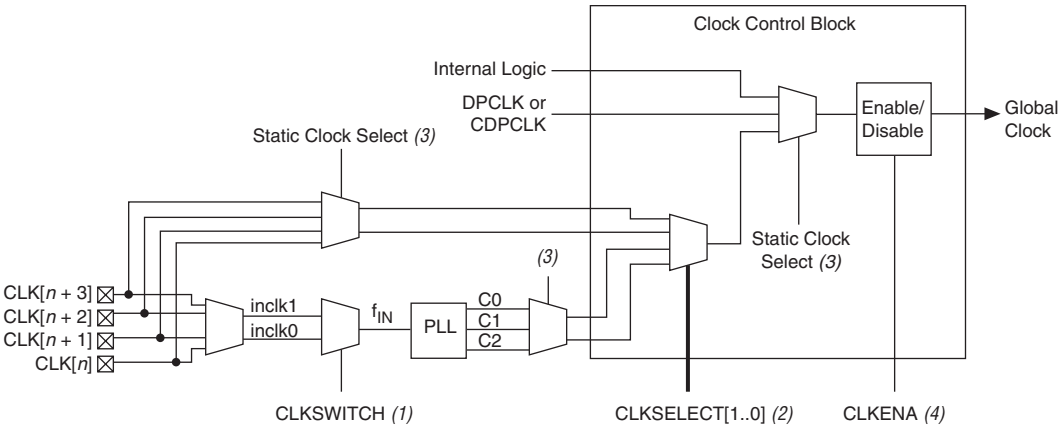
Table 2–1 shows the Cyclone II device's routing scheme.

Table 2–1. Cyclone II Device Routing Scheme (Part 1 of 2)

Source	Destination												
	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	LE	M4K RAM Block	Embedded Multiplier	PLL	Column IOE	Row IOE
Register Chain								✓					
Local Interconnect								✓	✓	✓	✓	✓	✓
Direct Link Interconnect		✓											
R4 Interconnect		✓		✓	✓	✓	✓						
R24 Interconnect				✓	✓	✓	✓						
C4 Interconnect		✓		✓	✓	✓	✓						
C16 Interconnect				✓	✓	✓	✓						

Of the sources listed, only two clock pins, two PLL clock outputs, one DPCLK pin, and one internally-generated signal are chosen to drive into a clock control block. Figure 2–13 shows a more detailed diagram of the clock control block. Out of these six inputs, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of DPCLK and the signal from internal logic.

Figure 2–13. Clock Control Block



Notes to Figure 2–13:

(1) The CLKSWITCH signal can either be set through the configuration file or it can be dynamically set when using the manual PLL switchover feature. The output of the multiplexer is the input reference clock (f_{IN}) for the PLL.

(2) The CLKSELECT[1..0] signals are fed by internal logic and can be used to dynamically select the clock source for the global clock network when the device is in user mode.

(3) The static clock select signals are set in the configuration file and cannot be dynamically controlled when the device is in user mode.

(4) Internal logic can be used to enabled or disabled the global clock network in user mode.

Table 2–4 describes the PLL features in Cyclone II devices.

Table 2–4. Cyclone II PLL Features

Feature	Description
Clock multiplication and division	*m* / (*n* × post-scale counter) *m* and post-scale counter values (C0 to C2) range from 1 to 32. *n* ranges from 1 to 4.
Phase shift	Cyclone II PLLs have an advanced clock shift capability that enables programmable phase shifts in increments of at least 45°. The finest resolution of phase shifting is determined by the voltage control oscillator (VCO) period divided by 8 (for example, 1/1000 MHz/8 = down to 125-ps increments).
Programmable duty cycle	The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each PLL post-scale counter (C0-C2).
Number of internal clock outputs	The Cyclone II PLL has three outputs which can drive the global clock network. One of these outputs (C2) can also drive a dedicated PLL<#>_OUT pin (single ended or differential).
Number of external clock outputs	The C2 output drives a dedicated PLL<#>_OUT pin. If the C2 output is not used to drive an external clock output, it can be used to drive the internal global clock network. The C2 output can concurrently drive the external clock output and internal global clock network.
Manual clock switchover	The Cyclone II PLLs support manual switchover of the reference clock through internal logic. This enables you to switch between two reference input clocks during user mode for applications that may require clock redundancy or support for clocks with two different frequencies.
Gated lock signal	The lock output indicates that there is a stable clock output signal in phase with the reference clock. Cyclone II PLLs include a programmable counter that holds the lock signal low for a user-selected number of input clock transitions, allowing the PLL to lock before enabling the locked signal. Either a gated locked signal or an ungated locked signal from the locked port can drive internal logic or an output pin.
Clock feedback modes	In zero delay buffer mode, the external clock output pin is phase-aligned with the clock input pin for zero delay. In normal mode, the PLL compensates for the internal global clock network delay from the input clock pin to the clock port of the IOE output registers or registers in the logic array. In no compensation mode, the PLL does not compensate for any clock networks.
Control signals	The pllenable signal enables and disables the PLLs. The areset signal resets/resynchronizes the inputs for each PLL. The pfdena signal controls the phase frequency detector (PFD) output with a programmable gate.

the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

Altera has ensured by design of the I/O buffers and hot-socketing circuitry, that Cyclone II devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone II Devices

The hot-socketing feature turns off the output buffer during power up (either V_{CCINT} or V_{CCIO} supplies) or power down. The hot-socket circuit generates an internal HOTSCKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. Designs cannot use the HOTSCKT signal for other purposes. The HOTSCKT signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When V_{CC} ramps up slowly, V_{CC} is still relatively low even after the internal POR signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tristated at this low V_{CC} voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are able to operate during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 4–1.

Table 5–42. Cyclone II I/O Output Delay for Column Pins (Part 6 of 6)

I/O Standard	Drive Strength	Parameter	Fast Corner		–6 Speed Grade	–7 Speed Grade (2)	–7 Speed Grade (3)	–8 Speed Grade	Unit
			Industrial/ Automotive	Commer -cial					
1.5V_DIFFERENTIAL _HSTL_CLASS_II	16 mA (1)	t_{OP}	1750	1836	3844	4125	4399	4406	ps
		t_{DIP}	1882	1975	4014	4319	4625	4625	ps
LVDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
RSDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
MINI_LVDS	—	t_{OP}	1258	1319	2243	2344	2438	2445	ps
		t_{DIP}	1390	1458	2413	2538	2664	2664	ps
SIMPLE_RSDS	—	t_{OP}	1221	1280	2258	2435	2605	2612	ps
		t_{DIP}	1353	1419	2428	2629	2831	2831	ps
1.2V_HSTL	—	t_{OP}	2403	2522	4635	5344	6046	6053	ps
		t_{DIP}	2535	2661	4805	5538	6272	6272	ps
1.2V_DIFFERENTIAL _HSTL	—	t_{OP}	2403	2522	4635	5344	6046	6053	ps
		t_{DIP}	2535	2661	4805	5538	6272	6272	ps

Notes to Table 5–42:

(1) This is the default setting in the Quartus II software.
(2) These numbers are for commercial devices.
(3) These numbers are for automotive devices.

Table 5–45. Maximum Output Clock Toggle Rate on Cyclone II Devices (Part 2 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate on Cyclone II Devices (MHz)								
		Column I/O Pins *(1)*			Row I/O Pins *(1)*			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
LVCMOS	4 mA	250	210	170	250	210	170	250	210	170
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	310	260	210	310	260	210	310	260	210
	16 mA	320	270	220	—	—	—	—	—	—
	20 mA	350	290	240	—	—	—	—	—	—
	24 mA	370	310	250	—	—	—	—	—	—
2.5V	4 mA	180	150	120	180	150	120	180	150	120
	8 mA	280	230	190	280	230	190	280	230	190
	12 mA	440	370	300	—	—	—	—	—	—
	16 mA	450	405	350	—	—	—	—	—	—
1.8V	2 mA	120	100	80	120	100	80	120	100	80
	4 mA	180	150	120	180	150	120	180	150	120
	6 mA	220	180	150	220	180	150	220	180	150
	8 mA	240	200	160	240	200	160	240	200	160
	10 mA	300	250	210	300	250	210	300	250	210
	12 mA	350	290	240	350	290	240	350	290	240
1.5V	2 mA	80	60	50	80	60	50	80	60	50
	4 mA	130	110	90	130	110	90	130	110	90
	6 mA	180	150	120	180	150	120	180	150	120
	8 mA	230	190	160	—	—	—	—	—	—
SSTL_2_CLASS_I	8 mA	400	340	280	400	340	280	400	340	280
	12 mA	400	340	280	400	340	280	400	340	280
SSTL_2_CLASS_II	16 mA	350	290	240	350	290	240	350	290	240
	20 mA	400	340	280	—	—	—	—	—	—
	24 mA	400	340	280	—	—	—	—	—	—
SSTL_18_CLASS_I	6 mA	260	220	180	260	220	180	260	220	180
	8 mA	260	220	180	260	220	180	260	220	180
	10 mA	270	220	180	270	220	180	270	220	180
	12 mA	280	230	190	—	—	—	—	—	—

Table 5–46. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 4)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
SSTL_2_CLASS_II	16 mA	42	43	45	15	29	42	15	29	42
	20 mA	41	42	44	—	—	—	—	—	—
	24 mA	40	42	43	—	—	—	—	—	—
SSTL_18_ CLASS_I	6 mA	20	22	24	46	47	49	46	47	49
	8 mA	20	22	24	47	49	51	47	49	51
	10 mA	20	22	25	23	25	27	23	25	27
	12 mA	19	23	26	—	—	—	—	—	—
SSTL_18_ CLASS_II	16 mA	30	33	36	—	—	—	—	—	—
	18 mA	29	29	29	—	—	—	—	—	—
1.8V_HSTL_ CLASS_I	8 mA	26	28	29	59	61	63	59	61	63
	10 mA	46	47	48	65	66	68	65	66	68
	12 mA	67	67	67	71	71	72	71	71	72
1.8V_HSTL_ CLASS_II	16 mA	62	65	68	—	—	—	—	—	—
	18 mA	59	62	65	—	—	—	—	—	—
	20 mA	57	59	62	—	—	—	—	—	—
1.5V_HSTL_ CLASS_I	8 mA	40	40	41	28	32	36	28	32	36
	10 mA	41	42	42	—	—	—	—	—	—
	12 mA	43	43	43	—	—	—	—	—	—
1.5V_HSTL_ CLASS_II	16 mA	18	20	21	—	—	—	—	—	—
DIFFERENTIAL_SSTL_2 _CLASS_I	8 mA	46	47	49	25	40	56	25	40	56
	12 mA	67	69	70	23	42	60	23	42	60
DIFFERENTIAL_SSTL_2 _CLASS_II	16 mA	42	43	45	15	29	42	15	29	42
	20 mA	41	42	44	—	—	—	—	—	—
	24 mA	40	42	43	—	—	—	—	—	—
DIFFERENTIAL_SSTL_ 18_CLASS_I	6 mA	20	22	24	46	47	49	46	47	49
	8 mA	20	22	24	47	49	51	47	49	51
	10 mA	20	22	25	23	25	27	23	25	27
	12 mA	19	23	26	—	—	—	—	—	—

Table 5–55. Maximum DCD for Single Data Outputs (SDR) on Row I/O Pins *Notes (1), (2)* *(Part 2 of 2)*

Row I/O Output Standard	C6	C7	C8	Unit
Differential SSTL-2 Class I	60	90	90	ps
Differential SSTL-2 Class II	65	75	75	ps
Differential SSTL-18 Class I	90	165	165	ps
Differential HSTL-18 Class I	85	155	155	ps
Differential HSTL-15 Class I	145	145	205	ps
LVDS	60	60	60	ps
Simple RSDS	60	60	60	ps
Mini LVDS	60	60	60	ps
PCI	195	255	255	ps
PCI-X	195	255	255	ps

Notes to Table 5–55:
(1) The DCD specification is characterized using the maximum drive strength available for each I/O standard.
(2) Numbers are applicable for commercial, industrial, and automotive devices.

Here is an example for calculating the DCD as a percentage for an SDR output on a row I/O on a –6 device:

If the SDR output I/O standard is SSTL-2 Class II, the maximum DCD is 65 ps (refer to Table 5–55). If the clock frequency is 167 MHz, the clock period T is:

$$T = 1/f = 1 / 167\ \text{MHz} = 6\ \text{ns} = 6000\ \text{ps}$$

To calculate the DCD as a percentage:

$(T/2 - DCD) / T = (6000\ \text{ps}/2 - 65\ \text{ps}) / 6000\ \text{ps} = 48.91\%$ (for low boundary)

$(T/2 + DCD) / T = (6000\ \text{ps}/2 + 65\ \text{ps}) / 6000\text{ps} = 51.08\%$ (for high boundary

Table 5–56. Maximum DCD for SDR Output on Column I/O *Notes (1), (2)* *(Part 1 of 2)*

Column I/O Output Standard	C6	C7	C8	Unit
LVCMOS	195	285	285	ps
LVTTL	210	305	305	ps

9. External Memory Interfaces

CII51009-3.1

Introduction

Improving data bandwidth is an important design consideration when trying to enhance system performance without complicating board design. Traditionally, doubling the data bandwidth of a system required either doubling the system frequency or doubling the number of data I/O pins. Both methods are undesirable because they complicate the overall system design and increase the number of I/O pins. Using double data rate (DDR) I/O pins to transmit and receive data doubles the data bandwidth while keeping I/O counts low. The DDR architecture uses both edges of a clock to transmit data, which facilitates data transmission at twice the rate of a single data rate (SDR) architecture using the same clock speed while maintaining the same number of I/O pins. DDR transmission should be used where fast data transmission is required for a broad range of applications such as networking, communications, storage, and image processing.

Cyclone® II devices support a broad range of external memory interfaces, such as SDR SDRAM, DDR SDRAM, DDR2 SDRAM, and QDRII SRAM. Dedicated clock delay control circuitry allows Cyclone II devices to interface with an external memory device at clock speeds up to 167 MHz/333 Mbps for DDR and DDR2 SDRAM devices and 167 MHz/667 Mbps for QDRII SRAM devices. Although Cyclone II devices also support SDR SDRAM, this chapter focuses on the implementations of a double data rate I/O interface using the hardware features available in Cyclone II devices and explains briefly how each memory standard uses the Cyclone II features.

The easiest way to interface to external memory devices is by using one of the Altera® external memory IP cores listed below.

- DDR2 SDRAM Controller MegaCore® Function
- DDR SDRAM Controller MegaCore Function
- QDRII SRAM Controller MegaCore Function

OpenCore® Plus evaluations of these cores are available for free to Quartus® II Web Edition software users. In addition, Altera software subscription customers now receive full licenses to these MegaCore functions as part of the IP-BASE suite.

External Memory Interface Standards

The following sections describe how to use Cyclone II device external memory interfacing features.

DDR & DDR2 SDRAM

DDR SDRAM is a memory architecture that transmits and receives data at twice the clock speed. These devices transfer data on both the rising and falling edge of the clock signal. DDR2 SDRAM is the second generation memory based on the DDR SDRAM architecture and is capable of data transfer rates of up to 533 Mbps. Cyclone II devices support DDR and DDR2 SDRAM at up to 333 Mbps.

Interface Pins

DDR and DDR2 SDRAM devices use interface pins such as data (DQ), data strobe (DQS), clock, command, and address pins to communicate with the memory controller. Data is sent and captured at twice the system clock rate by transferring data on the positive and negative edge of the clock. The commands and addresses use only one active (positive) edge of a clock.

DDR SDRAM uses single-ended data strobe DQS, while DDR2 SDRAM has the option to use differential data strobes DQS and DQS#. Cyclone II devices do not use the optional differential data strobes for DDR2 SDRAM interfaces. You can leave the DDR2 SDRAM memory DQS# pin unconnected, because only the shifted DQS signal from the clock delay control circuitry captures data. DDR and DDR2 SDRAM ×16 devices use two DQS pins, and each DQS pin is associated with eight DQ pins. However, this is not the same as the ×16/×18 mode in Cyclone II devices. You need to configure the Cyclone II devices to use two sets of pins in ×8 mode. Similarly, if your ×72 memory module uses nine DQS pins where each DQS pin is associated with eight DQ pins, configure the Cyclone II device to use nine sets of DQS/DQ groups in ×8 mode.

Connect the memory device's DQ and DQS pins to the Cyclone II DQ and DQS pins, respectively, as listed in the Cyclone II pin tables. DDR and DDR2 SDRAM also use active-high data mask (DM) pins for writes. DM pins are pre-assigned in pin outs for Cyclone II devices, and these are the preferred pins. However, you may connect the memory device's DM pins to any of the Cyclone II I/O pins in the same bank as the DQ pins of the FPGA. There is one DM pin per DQS/DQ group. If the DDR or DDR2 SDRAM device supports ECC, the design uses an extra DQS/DQ group for the ECC pins.

For information about the I/O standards supported for external memory applications, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone II Device Handbook*.

Table 10–1. Cyclone II Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	V_{CCIO} Level		Top and Bottom I/O Pins		Side I/O Pins		
		Input	Output	CLK, DQS	User I/O Pins	CLK, DQS	PLL_OUT	User I/O Pins
3.3-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	3.3 V	✓	✓	✓	✓	✓
2.5-V LVTTL and LVCMOS	Single ended	3.3 V/ 2.5 V	2.5 V	✓	✓	✓	✓	✓
1.8-V LVTTL and LVCMOS	Single ended	1.8 V/ 1.5 V	1.8 V	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single ended	1.8 V/ 1.5 V	1.5 V	✓	✓	✓	✓	✓
SSTL-2 class I	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-2 class II	Voltage referenced	2.5 V	2.5 V	✓	✓	✓	✓	✓
SSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
SSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-18 class I	Voltage referenced	1.8 V	1.8 V	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	1.8 V	1.8 V	✓	✓	*(1)*	*(1)*	*(1)*
HSTL-15 class I	Voltage referenced	1.5 V	1.5 V	✓	✓	✓	✓	✓
HSTL-15 class II	Voltage referenced	1.5 V	1.5 V	✓	✓	*(1)*	*(1)*	*(1)*
PCI and PCI-X *(2)*	Single ended	3.3 V	3.3 V	—	—	✓	✓	✓
Differential SSTL-2 class I or class II	Pseudo differential *(3)*	*(4)*	2.5 V	—	—	—	✓	—
		2.5 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—
Differential SSTL-18 class I or class II	Pseudo differential *(3)*	*(4)*	1.8 V	—	—		✓ *(6)*	—
		1.8 V	*(4)*	✓ *(5)*	—	✓ *(5)*	—	—

1.8-V LVCMOS (EIA/JEDEC Standard EIA/JESD8-7)

The 1.8-V I/O standard is used for 1.8-V LVCMOS applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.8-V parts.

The 1.8-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.8-V LVCMOS.

SSTL-18 Class I and II

The 1.8-V SSTL-18 standard is formulated under JEDEC Standard, JESD815: Stub Series Terminated Logic for 1.8V (SSTL-18).

The SSTL-18 I/O standard is a 1.8-V memory bus standard used for applications such as high-speed DDR2 SDRAM interfaces. This standard is similar to SSTL-2 and defines input and output specifications for devices that are designed to operate in the SSTL-18 logic switching range 0.0 to 1.8 V. SSTL-18 requires a 0.9-V V_{REF} and a 0.9-V V_{TT}, with the termination resistors connected to both. There are no class definitions for the SSTL-18 standard in the JEDEC specification. The specification of this I/O standard is based on an environment that consists of both series and parallel terminating resistors. Altera provides solutions to two derived applications in JEDEC specification and names them class I and class II to be consistent with other SSTL standards. Figures 10–5 and 10–6 show SSTL-18 class I and II termination, respectively. Cyclone II devices support both input and output levels.

Figure 10–5. 1.8-V SSTL Class I Termination

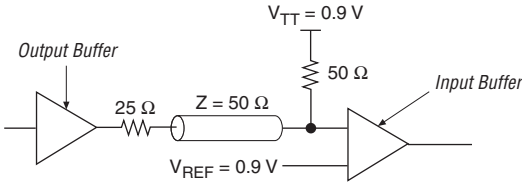
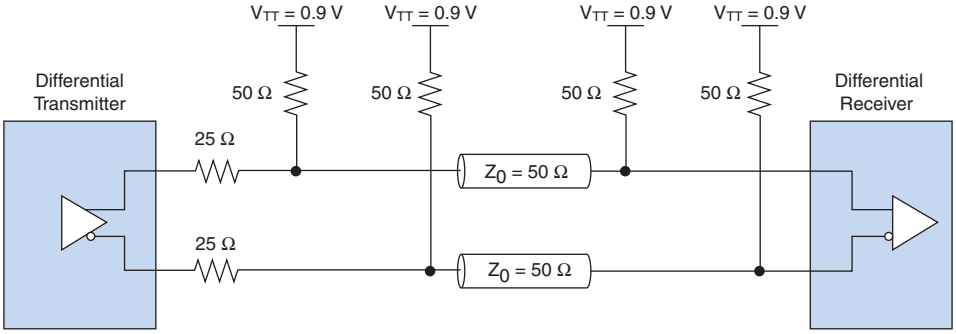


Figure 10–10. Differential SSTL-18 Class II Termination



1.8-V Pseudo-Differential HSTL Class I and II

The 1.8-V differential HSTL specification is the same as the 1.8-V single-ended HSTL specification. It is used for applications designed to operate in the 0.0 to 1.8-V HSTL logic switching range such as QDR memory clock interfaces. Cyclone II devices support both input and output levels. Refer to Figures 10–11 and 10–12 for details on 1.8-V differential HSTL termination.

Cyclone II devices do not support true 1.8-V differential HSTL standards. Cyclone II devices support pseudo-differential HSTL outputs for `PLL_OUT` pins and pseudo-differential HSTL inputs for clock pins. Pseudo-differential inputs require an input reference voltage as opposed to the true differential inputs. Refer to Table 10–1 on page 10–2 for information about pseudo-differential HSTL.

Figure 10–11. 1.8-V Differential HSTL Class I Termination

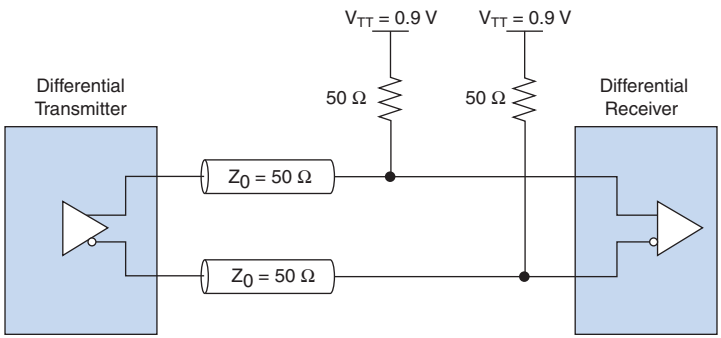
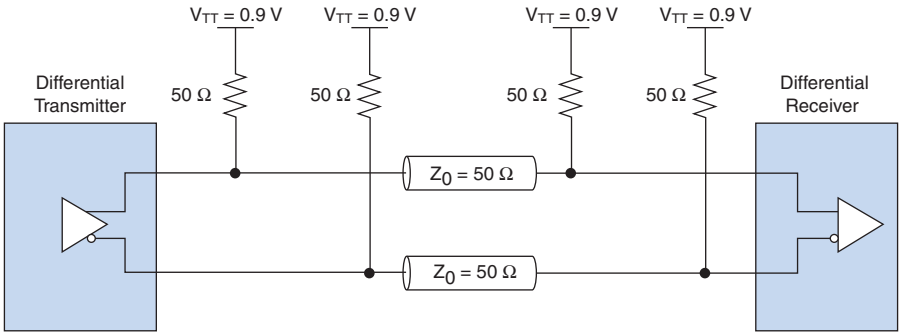


Figure 10–12. 1.8-V Differential HSTL Class II Termination



1.5-V LVCMOS (EIA/JEDEC Standard JESD8-11)

The 1.5-V I/O standard is used for 1.5-V applications. This standard defines the DC interface parameters for high-speed, low-voltage, non-terminated digital circuits driving or being driven by other 1.5-V devices.

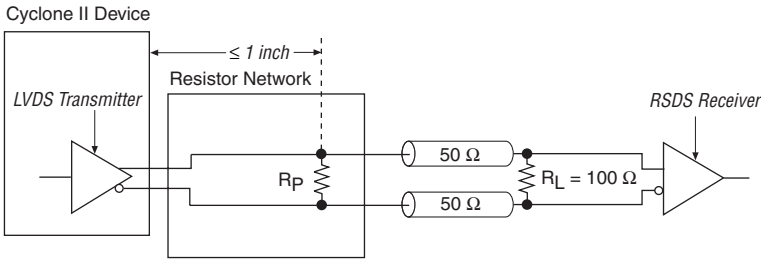
The 1.5-V standard does not require input reference voltages or board terminations. Cyclone II devices support input and output levels for 1.5-V LVCMOS.

1.5-V HSTL Class I and II

The 1.5-V HSTL standard is formulated under EIA/JEDEC Standard, EIA/JESD8-6: A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.

The 1.5-V HSTL I/O standard is used for applications designed to operate in the 0.0- to 1.5-V HSTL logic nominal switching range. This standard defines single-ended input and output specifications for all HSTL-compliant digital integrated circuits. The 1.5-V HSTL I/O standard in Cyclone II devices is compatible with the 1.8-V HSTL I/O standard in APEX™ 20KE, APEX 20KC, Stratix® II, Stratix GX, Stratix, and in Cyclone II devices themselves because the input and output voltage thresholds are compatible. Refer to Figures 10–13 and 10–14. Cyclone II devices support both input and output levels with V_{REF} and V_{TT}.

Figure 11–8. RSDS Single Resistor Network *Note (1)*



Note to Figure 11–8:
(1) R_p = 100 Ω

RSDS Software Support

When designing for the RSDS I/O standard, assign the RSDS I/O standard to the I/O pins intended for RSDS in the Quartus® II software. Contact Altera Applications for reference designs.

mini-LVDS Standard Support in Cyclone II Devices

The mini-LVDS specification defines its use in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone II devices meet the Texas Instruments mini-LVDS Interface Specification and support the mini-LVDS output standard. Table 11–3 shows the mini-LVDS electrical characteristics for Cyclone II devices.

Table 11–3. mini-LVDS Electrical Characteristics for Cyclone II Devices *Note (1)*

Symbol	Parameters	Condition	Min	Typ	Max	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{OD} *(2)*	Differential output voltage	R_L = 100 Ω	300		600	mV
V_{OS} *(3)*	Output offset voltage	R_L = 100 Ω	1125	1250	1375	mV
T_r / T_f	Transition time	20% to 80%			500	ps

Notes to Table 11–3:
(1) The V_{OD} specifications apply at the resistor network output.
(2) $V_{OD} = V_{OH} - V_{OL}$.
(3) $V_{OS} = (V_{OH} + V_{OL}) / 2$.

12. Embedded Multipliers in Cyclone II Devices

CII51012-1.2

Introduction

Use Cyclone® II FPGAs alone or as digital signal processing (DSP) co-processors to improve price-to-performance ratios for DSP applications. You can implement high-performance yet low-cost DSP systems with the following Cyclone II device features and design support:

- Up to 150 18 x 18 multipliers
- Up to 1.1 Mbit of on-chip embedded memory
- High-speed interface to external memory
- DSP Intellectual Property (IP) cores
- DSP Builder interface to the Mathworks Simulink and Matlab design environment
- DSP Development Kit, Cyclone II Edition

This chapter focuses on the Cyclone II embedded multiplier blocks.

Cyclone II devices have embedded multiplier blocks optimized for multiplier-intensive low-cost DSP applications. These embedded multipliers combined with the flexibility of programmable logic devices (PLDs), provide you with the ability to efficiently implement various cost sensitive DSP functions easily. Consumer-based application systems such as digital television (DTV) and home entertainment systems typically require a cost effective solution for implementing multipliers to perform signal processing functions like finite impulse response (FIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

Along with the embedded multipliers, the M4K memory blocks in Cyclone II devices also support various soft multiplier implementations. These, in combination with the embedded multipliers increase the available number of multipliers in Cyclone II devices and provide the user with a wide variety of implementation options and flexibility when designing their systems.

See the Cyclone II Device Family Data Sheet section in Volume 1 of the ***Cyclone II Device Handbook*** for more information on Cyclone II devices.

Configuration File Format

Table 13–3 shows the approximate uncompressed configuration file sizes for Cyclone II devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

Table 13–3. Cyclone II Raw Binary File (.rbf) Sizes *Note (1)*

Device	Data Size (Bits)	Data Size (Bytes)
EP2C5	1,265,792	152,998
EP2C8	1,983,536	247,974
EP2C15	3,892,496	486,562
EP2C20	3,892,496	486,562
EP2C35	6,858,656	857,332
EP2C50	9,963,392	1,245,424
EP2C70	14,319,216	1,789,902

Note to Table 13–3:
(1) These values are preliminary.

Use the data in Table 13–3 only to estimate the file size before design compilation. Different configuration file formats, such as a Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) format, have different file sizes. However, for any specific version of the Quartus® II software, any design targeted for the same device has the same uncompressed configuration file size. If compression is used, the file size can vary after each compilation since the compression ratio is dependent on the design.

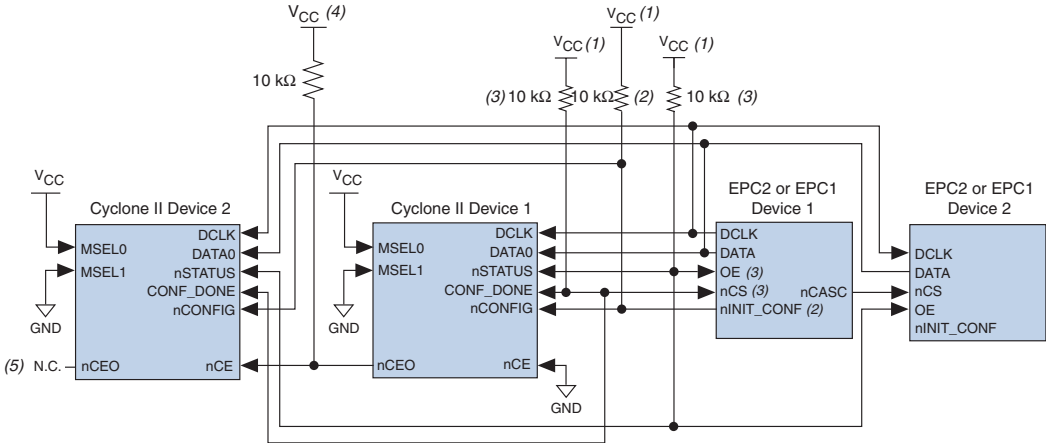
Configuration Data Compression

Cyclone II devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Cyclone II devices. During configuration, the Cyclone II device decompresses the bitstream in real time and programs its SRAM cells.

Preliminary data indicates that compression reduces configuration bitstream size by 35 to 55%.

Cyclone II devices support decompression in the AS and PS configuration schemes. Decompression is not supported in JTAG-based configuration.

Figure 13–17. Multiple Device PS Configuration Using Cascaded EPC2 or EPC1 Devices



Notes to Figure 13–17:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin (available on enhanced configuration devices and EPC2 devices only) has an internal pull-up resistor that is always active, meaning an external pull-up resistor should not be used on the nINIT_CONF to nCONFIG line. The nINIT_CONF pin does not need to be connected if its functionality is not used. If nINIT_CONF is not used or not available (e.g., on EPC1 devices), nCONFIG must be pulled to V_{CC} either directly or through a resistor (if reconfiguration is required, a resistor is necessary).

(3) The enhanced configuration devices' and EPC2 devices' OE and nCS pins have internal programmable pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device option** when generating programming files.

(4) Use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the I/O bank V_{CCIO} level to help the internal weak pull-up when it feeds next device's nCE pin.

(5) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

When using enhanced configuration devices or EPC2 devices, you can connect the Cyclone II device's nCONFIG pin to the configuration device's nINIT_CONF pin, which allows the INIT_CONF JTAG instruction to initiate FPGA configuration. You do not need to connect the nINIT_CONF pin if it is not used. If the nINIT_CONF pin is not used or not available (for example, on EPC1 devices), pull the nCONFIG pin to V_{CC} levels either directly or through a resistor (if reconfiguration is required, a resistor is necessary). An internal pull-up resistor on the nINIT_CONF pin is always active in the enhanced configuration devices and the EPC2 devices. Therefore, do not use an external pull-up resistor if you connect the nCONFIG pin to nINIT_CONF. If you use multiple EPC2 devices to configure a Cyclone II device(s), only connect the first EPC2 device's nINIT_CONF pin to the device's nCONFIG pin.